IKONAS GRAPHICS SYSTEMS INC
403 GLENWOOD AVE — RALEIGH NC 27603 — 919/833-5401

FBPR 64/8 Graphics Processor System

The FBPR 64/8 system contains an 8-bit 512x512 resolution frame buffer along with a powerful graphics display processor.

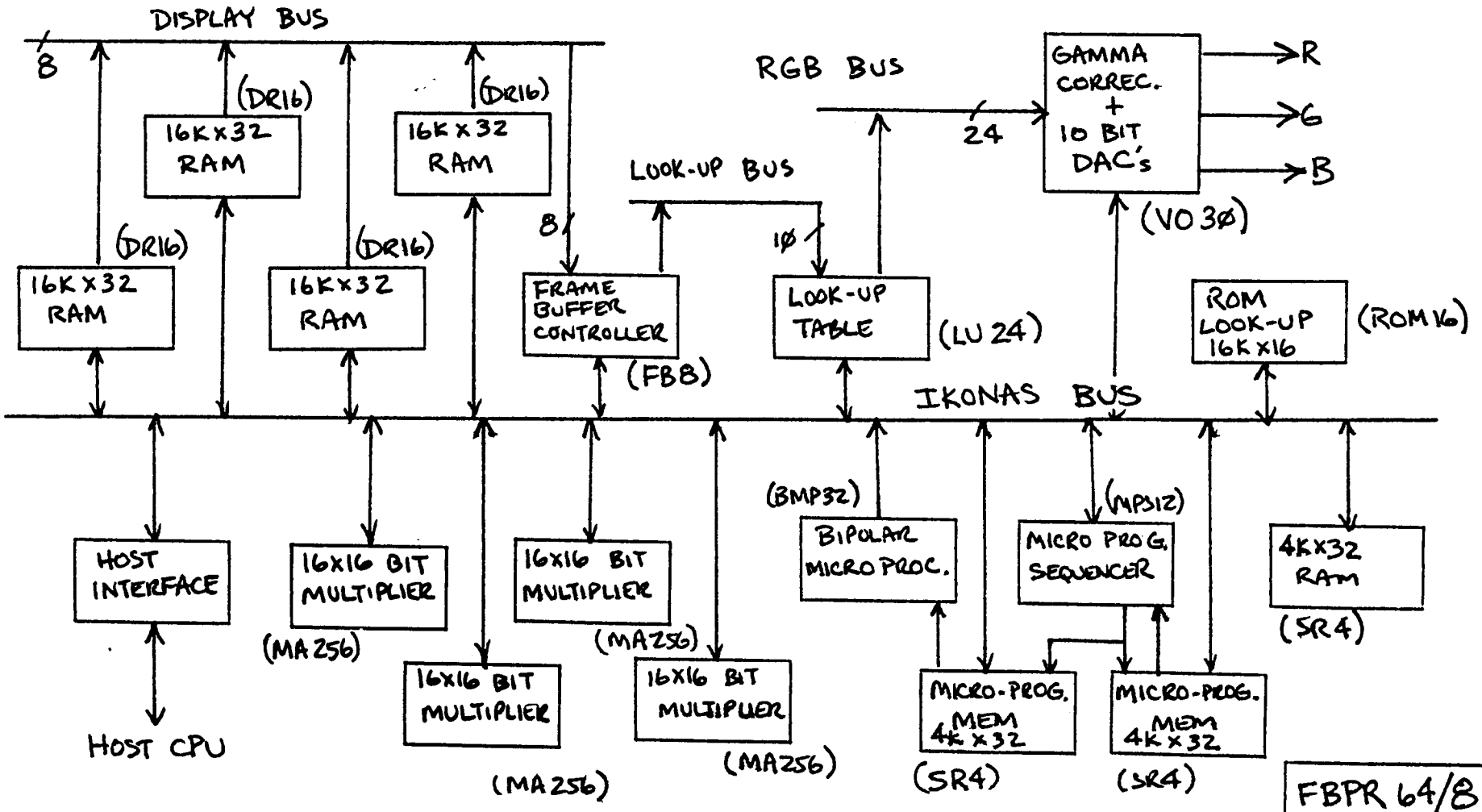
Physically, the system consists of two card cages (9 cards each) connected by a common IKONAS bus system and power supplies, all housed with a six foot rack with ample room for other equipment.

The 512x512x8 frame buffer consists of four DR16 16Kx32 dynamic RAM cards, an FB8 frame buffer controller, LU24 1Kx24 color look-up table and VO30 video output card.

The processor section is composed of up to 10 other cards. Typically, this would include:

```
 one BMP 32 bipolar microprocessor
 one MPS 32 microprogram sequencer
 two SR 4   4Kx32 microprogram memories
four MA 256 multiplier-accumulators
 one ROM 16 16Kx32 ROM look-up memory
 one SR 4   4Kx32 static memory
```

A high performance host interface card is included with the system.



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FBPR 64/8

GRAPHICS PROCESSOR SYSTEM

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THE IKONAS PROCESSOR AND SEQUENCER

The IKONAS processor is implemented using the Advanced Micro Devices Am2903 bipolar bit slice processor and the Am2911 bit slice microprogram sequencer. A familiarity with these two components will ease understanding of the IKONAS processor, BMP 32, and the microprogram sequencer, MPS 16. A bibliography of introductory literature about bit slice processors and microprogramming is attached. The Applications Notes and Microprogramming Handbook available from AMD are particularly helpful.

The IKONAS processor operates on 32 bit wide words. The processor is controlled by a sequence of microcode words (microprogram) that are 64 bits wide and are stored in static RAM microcode memory. Microprograms are downloaded from the host processor before execution. Programs may be stored in ROM memory. Each microinstruction executes in 200 nsec. Next address selection (program flow control) uses 32 bits of each microcode word. The remianing 32 bits of microcode control ALU function and operand selection. The IKONAS processor and sequencer operation will be discussed in terms of the 64 bit microcode word. Important features of the processor and sequencer will be emphasized as they effect the microcode.

MICROPROGRAM SEQUENCER CONTROL

Figure 1 is a block diagram of the MPS 16. Note the DATA FIELD REGISTER and the path from it to the LOOP COUNTER and the BMP 32. The CONTROL PROM, CONDITION CODE MULTIPLEXER, and the path from the MICROCODE LATCH to the IKONAS FUNCTION BUS are other important features. The sequencer, through the Am2911 and its related circuitry, uses the information in the microcode word and from the condition code lines to generate the 16 bit next address in the microprogram memory. Maximum size of the microprogram memory is 64K words, each 64 bits wide.

The lower 32 bits of a microcode word are inputs to the sequencer for next address selection. The bits are divided into the following fields:

DATA FIELD
OP CODE
CONDITION CODE SELECT
CONDITION CODE PARITY SELECT
LOAD CONTROL
IKONAS BUS FUNCTION CODE

DATA FIELD: Depending on the OP CODE and LOAD CONTROL bits, the 16 bit data field may be used as a pipeline address (D input to the 2911), ALU immediate data, or loop count.

OP CODE: The OP CODE determines what type of program control instruction is to be executed--that is, it addresses the CONTROL PROM which determines the next microcode address depending on the result of the condition code test. The Am2911 sequencer can output next microprogram address from one of four inputs: the data field (D), the 4 word on chip stack for subroutines and loops (F), the microprogram counter (PC), or an on chip latch which is loaded with the D data from the previous instruction (R). Features of the 2911 allow loops and subroutines to be executed with no overhead cycles. The CONTROL PROM has essentially the same instruction set as the Am29811A. Since the instruction set is in firmware, it can be changed or expanded.

CONDITION CODE SELECT: Condition codes are used to control conditional execution of the OP CODES. The condition code select bits choose 1 of 16 conditions to be tested. Presently implemented conditions are: counter=Ø, Host Request Line High, IKONAS BUS busy, IKONAS BUS or IMAGE MEMORY busy, Video Blanked, ALU overflow, ALU negative, ALU zero, and ALU carry out. Other specific condition codes can be easily added.

CONDITION CODE PARITY SELECT: This bit determines whether the conditional operation takes place on condition TRUE or condition FALSE.

LOAD CONTROL: Load Control determines whether the data field will be latched into the loop counter on the MPS 16 or into the immediate data register on the BMP 32.

IKONAS BUS FUNCTION CODE: This field controls read and write operations in Static RAM (32 bit parallel format), Dynamic RAM (512x512 or 1Ø24x1Ø24 format), or other special purpose devices (matrix multiplier, disk controller, etc.).

PROCESSOR CONTROL

In the processor block diagram, Figure 2, the important features are the 16 GENERAL PURPOSE REGISTERS, SELECTORS, and SHIFTERS within the 29Ø3, the R BUS SELECTOR and its sources, the Y BUS, the MDR, MAR, and IMMEDIATE DATA REGISTER and their paths to the IKONAS DATA and ADDRESS busses. The 16 general purpose registers are dual ported RAM with two independent address ports (A and B) and two independent output latches. Data may be written into the registers only using the B address port.

The 32 bits of microcode which are input to the processor are divided into the following fields:

R OPERAND SELECT
S OPERAND SELECT
ALU INSTRUCTION
ALU CARRY CONTROL
ALU SHIFT CONTROL
Y BUS SOURCE/DESTINATION
DR BUS DATA SOURCE
IKONAS BUS ADDRESS SOURCE
IKONAS BUS ENABLE

R OPERAND SELECT: This field selects one of the general purpose registers (Ø-15) or the R bus as the R operand. The field contains bits for A address and R bus select control. The R BUS data may be selected from the data registers (DR), lower 16 bits of DR, Memory Address Register (MAR), lower 16 bits of MAR, or the B register data in several forms: right rotated 8 or 16 bits, right shifted 8 or 16 bits.

S OPERAND SELECT: This field selects one of the general purpose registers (Ø-15) or the Q register as S operand. The B address bits within this field are also used to specify one of the general purpose registers as Y BUS output destination.

ALU FUNCTION: The IKONAS processor, using 8 Am29Ø3's, can perform 7 arithmetic and 9 logical operations on two 32 bit operands. In addition the Am29Ø3 can perform 9 special functions--principally multiplication, division, and normalization. See the Am29Ø3 data sheets for details of the available operations. This field also contains bits selecting shift type (logical or arithmetic) and direction (left or right) for the ALU shifter and Q shifter. Q register and B register write control are also contained in this field.

ALU CARRY CONTROL: Carry control circuitry is designed to allow operands to be treated as two 16 bit words or as one 32 bit word. In double 16 bit format $C_{in}Ø$ and $C_{in}16$ may be set to either 1's or Ø's. In 32 bit format, $C_{in}Ø$ may be set to Ø, 1, $C_{out}31$, or $C_{out}31$ inverted.

ALU SHIFT CONTROL: The ALU and Q shifters may be used to shift or rotate data. This field controls whether a shift or rotate is performed and whether the operations are long (64 bits using ALU and Q shifters as a unit) or short (using ALU and Q shifters as independent 32 bit units). The shift input (Ø or 1) is determined by this field. (Recall that direction and type of shift are controlled by the ALU FUNCTION field.)

Y BUS SOURCE/DESTINATION: The Y BUS is a communication path among the Am29Ø3 ALU general purpose registers, several special purpose registers, and an optional hardware multiplier. Possible sources of data on the Y BUS are the ALU output, the IKONAS BUS, and the multiplier output. Destinations possible are the general purpose registers (using the B address), the MDR, the MAR, and the multiplier inputs X and Y. When set up in the appropriate fields, the general purpose registers may be a second destination for data being written to the MDR, MAR, or multiplier inputs.

DR BUS DATA SOURCE: This field determines the data source for the DR bus. Data may come from the MDR or from the microcode data field for immediate operands.

IKONAS BUS ADDRESS SOURCE: For IKONAS BUS read and write cycles address data may come from the MAR directly or from the MAR shifted such that frame buffer X and Y addresses stored in upper and lower half words are packed into a single 24 bit address.

IKONAS BUS ENABLE: When set =1, this bit causes a Read or Write cycle on the IKONAS BUS.

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A BRIEF BIBLIOGRAPHY ON MICROPROGRAMMING AND BIT-SLICE PROCESSORS

I. Publications of Advanced Micro Devices, Inc.
901 Thompson Place
Sunnyvale, CA 94086
(available through Hamilton Avnet)

The Am2900 Family Data Book
Note: 2903, 2911 are major building blocks of the IKONAS processor IKASM^{tm}, the IKONAS cross assembler for microcode,is similar to ADASM

Microprogramming Handbook, John R. Mick and Jim Brick
Publication Number: AM-PUB029
Essentially a refinement of articles appearing in EDN, vol.23 no.2,3,4; January 20, February 5, February 20, 1978.

Microprogram Design with the Am2900 Family
Publication Number: AM-PUB069

Build a Microcomputer--Chapter II Microprogrammed Design
Publication Number: AM-PUB073-2

Applications literature for the Am2903

II. Articles

"A primer on bit-slice processors", John Nemec, Electronic Design, February 1, 1977.

"Use 4-bit slices to design powerful microprogrammed processors", Jim Clymer, Electronic Design, May 10, 1977.

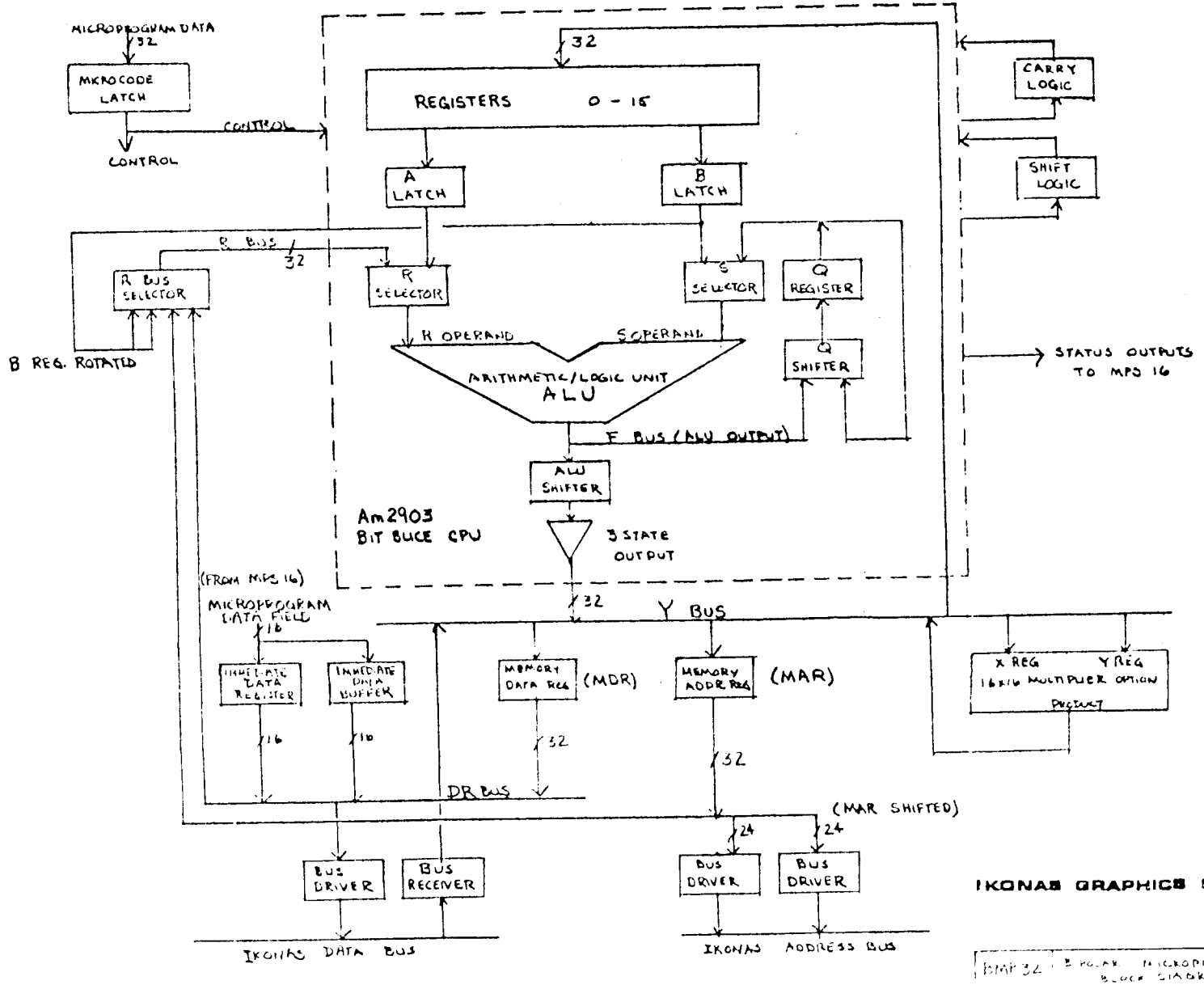
"Microprogramming: Making your mini move faster", John Trudeau, Digital Design, January, 1977.

"Bipolar μP's: Introduction to architecture and applications", John Nemec and Stephen Y. Lau, EDN, September 20, October 4, 1977.

"Microgrogramming: A General Design Tool", Robert Jaeger, Computer Design, August 1974.

III. Book

Microprogrammable Computer Architectures, Alan B. Salibury, Elsevier Computer Science Library, American Elsevier Publishing Co., Inc. New York, 1976.



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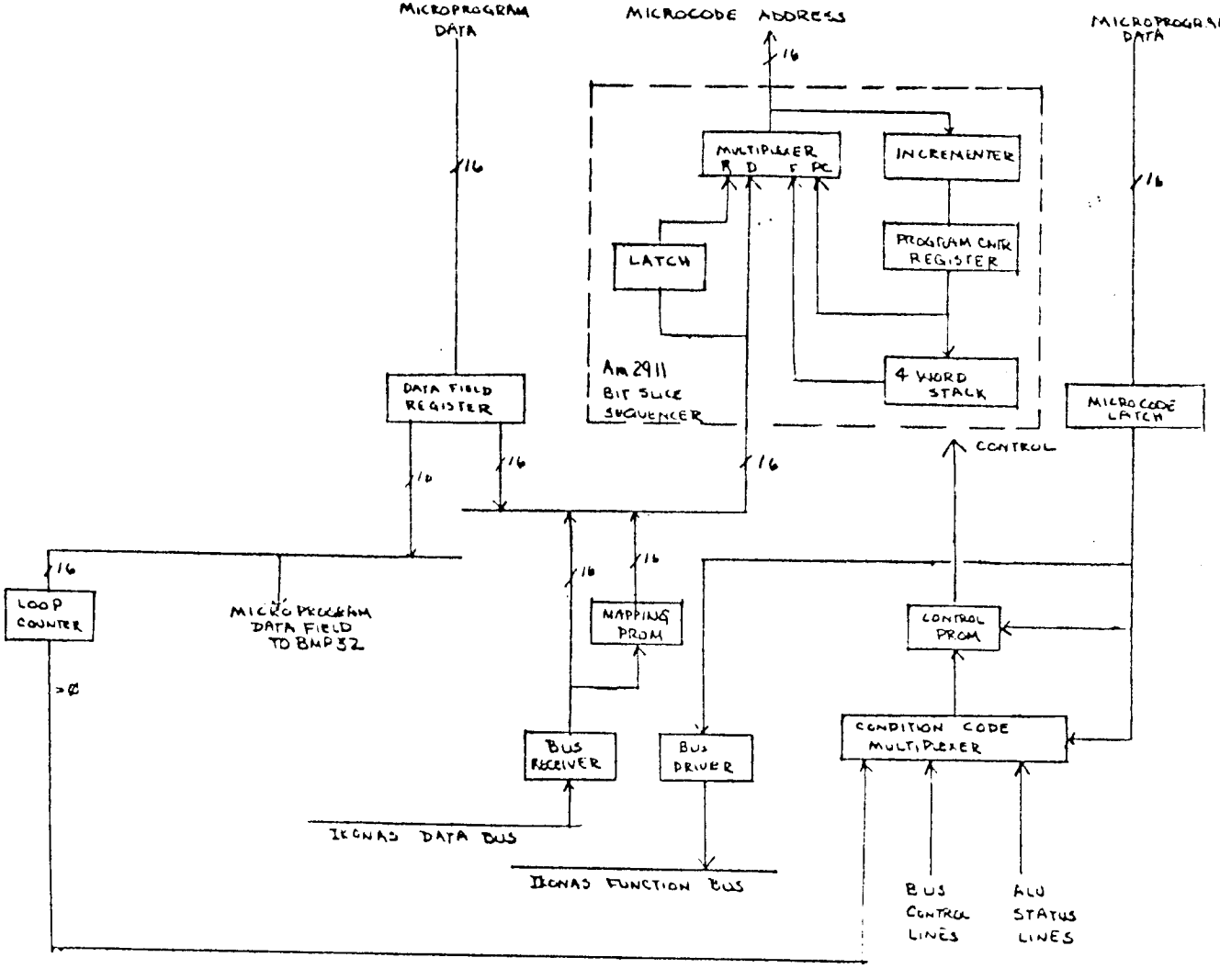
IMAP 32	32 BIT BIPOLAR MICROPROCESSOR BLOCK DIAGRAM	1 of 1 8/79



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MPS16	MICRO PROGRAM SEQUENCER BLOCK DIAGRAM	1 of 1 8/79

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SYSTEM CONFIGURATION GUIDE

The flexible, expandable nature of IKONAS graphics systems makes a multitude of system configurations possible. The modular design of IKONAS products makes it possible to begin with a small frame buffer system and later to add more image memory and processor elements. The following system configuration guide lists those modules which are essential to a frame buffer system, those which are essential for a system including a processor, and those which may be added to the basic systems.

BASIC FRAME BUFFER CONFIGURATION:

	Module Name
Image Memory	DR 16B
Frame Buffer Controller	FB/HC
Video Output	VO 30 or VO 24/HS
Host Interface	
Card Cage and Power Supply	CB 20

Each DR 16B can be accessed as 512x512x2 or 1024x512x1. Minimum configuration contains one DR 16B. Maximum configurations are 512x512x32 and 1024x1024x24. CB 20 holds 20 cards. Multiple cage configurations are possible.

The basic configuration does not include a color look-up table. One of the modules LU 24, LU 24/HS, LUI 24 should be chosen to add color look-up capability.

The Video Input Module, VI 8 (2 cards), can be added to the system to provide real time storage of video signals.

Mass Image Storage, KD 64, can be added to the system to store unencoded images or, for real time playback, run-length encoded images.

Animation capability can be added to the system by including the Mass Image Storage and one of the modules RLI 8, RLS 10, or RLU 24 for run-length decoding.

BASIC PROCESSOR CONFIGURATION:

	Module Name
Processor	BMP 32
Microprogram Sequencer	MPS 16
Microprogram Memory (2 cards required)	SR 1, SR 4, or SR 8
Processor Working Memory	SR 1, SR 4, or SR 8
Frame Buffer System (from above)	

The processor is designed to be used in a system that contains a frame buffer. All system timing is developed by the Frame Buffer Controller, FB/HC.

Additional processing power may be added by including one or more Multiplier-Accumulator Modules, MA 1024. Multiple MA 1024's may be programmed to run in parallel.

ROM modules may be added to the system to provide look-up tables and/or firmware storage.

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PRICE LIST FOR STANDARD MODULES
8/15/79

PROCESSOR ELEMENTS:		
BMP 32	Bipolar Microprocessor	$2000
MPS 16	Microprogram Sequencer	1500
MA 1024	Multiplier Accumulator	2200
MEMORY:		
DR 16B	Dynamic RAM	2000
ROM 16	Read Only Memory 16Kx16	2700
ROM 32	Read Only Memory 32Kx16	4100
ROM 64	Read Only Memory 64Kx16	6400
SR 1	Static RAM 1Kx32	2000
SR 4	Static RAM 4Kx32	2900
SR 8	Static RAM 8Kx32	**Future**
MASS IMAGE STORAGE:		
KD 64	Disk and Controller	9600
VIDEO INPUT:		
VI 8	Video Input Module (2 cards)	2850
VIDEO OUTPUT:		
FB/HC	Frame Buffer Controller	2000
RLI 8	Run-Length Decoder (Intensity Control)	2400
RLS 10	Run-Length Decoder (Shade Look-up)	2200
RLU 24	Run-Length Decoder (Unencoded shade)	2600
LU 24	Color Look-Up Table	2000
LU 24/HS	Color Look-Up Table/High Speed	**2900**
LUI 24	Color Look-Up Table (Intensity Control)	2300
VO 30	Gamma Correction and Video Output	2000
VO 24/HS	Video Output Module/High Speed	2000
INTERFACES:		
	Interfaces for popular minicomputers	2000-3000
MISCELLANEOUS:		
CB 20	Card Cage and Power Supply	3000

-----Prices subject to change without notification-----

WHEV - Ref

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IKONAS MODULAR INTERACTIVE PERIPHERAL DEVICES

DT 11	11"x 11" digitizing tablet with RS232 output, power supply, four button cursor, and 20 ft cable	$1350
JS 3	3 axis joystick with spring return	
	JS 3-1 analog output	$ 650
	JS 3-2 RS232 output	~~$1300~~ #1965
TB 3	3 inch track ball	
	TB 3-1 pulse and direction output	$2000
	TB 3-2 RS232 output	$2450
BB 16	16 software assignable function buttons with lighted indicators and parallel outputs	$ 500
DB 4	4 control dials	
	DB 4-1 analog output	$ 450
	DB 4-2 TTL pulse output	~~$ 495~~
KB 63	Keyboard with RS232 output	$ 750

Note: Each of these devices is provided with a separate enclosure. However, several enclosures can be ganged together into a single unit.

Prices subject to change without notificaton.

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TYPICAL SYSTEM PRICING

Minimal System - 512^2x8 with Look Up Table

DR64B	$ 7000.00
FBC	2500.00
LUV024	3800.00
IF	3200.00
CBP	4200.00
	$20,700.00

Typical System - 512^2x24 with Look Up Table processor, Matrix multiplier and monitor

3	DR64B	@7000	$ 21000.00
	FBC		2500.00
	LUV024		3800.00
	IF		3200.00
	BPS		3850.00
	MCM4		6000.00
2	SR4		6000.00
	MA 1024/D		3600.00
	CBP		4200.00
	MON 19		4300.00
			$58,450.00

MCW: 9/8/80

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PRICE LIST FOR STANDARD MODULES

5 September 1980

Frame Buffer Modules		
DR 64B	Image Memory 512 x 512 x 8	$7000
FBC	Frame Buffer Controller	2500
LUVO 24	Color Look Up Table and 8 bit Video Outputs 15 MHz	3800
LUVO 24/HS	High Speed Color Look Up Table and 8 bit Video Outputs 40 MHz	5000
LUVO 30/HS	High Speed Color Look Up Table and 10 bit Video Outputs 40 MHz	5500
XBS 24	Cross Bar Switch	2000
Monitors		
MON 19	19" Color Monitor: 15MHz for 512 x 512 Display	4300
MON 19/HS	19" Color Monitor: 40MHz for 1024 x 1024 Display	9200
Processing Modules and Processor Memory		
BPS 32	Bipolar Processor and Sequencer: 32 bit, 200 nsec bipolar microprocessor and sequencer	3850
MCM 4	Microcode Memory: 4K x 64 Static RAM for microprogram storage	6000
SR 4	Static RAM: 4K x 32 Static RAM for BPS or MA 1024 scratchpad	3000
MA 1024	Programmable Matrix Multiplier	3000
MA 1024/D	Programmable Matrix Multiplier with Divide Option	3600
Video Input		
VI 8	Video Input Module (monochrome): 8bits/sample, 16MHz	3650
VI 24	Video Input Module (RGB): 24 bits/sample, 16MHz	6950
Interfaces		
IF/*/DMA	DMA Interface to Host Computer; price may vary	3200
Mechanical		
CBP	Chassis and Power Supplies: 12 card capacity	4200

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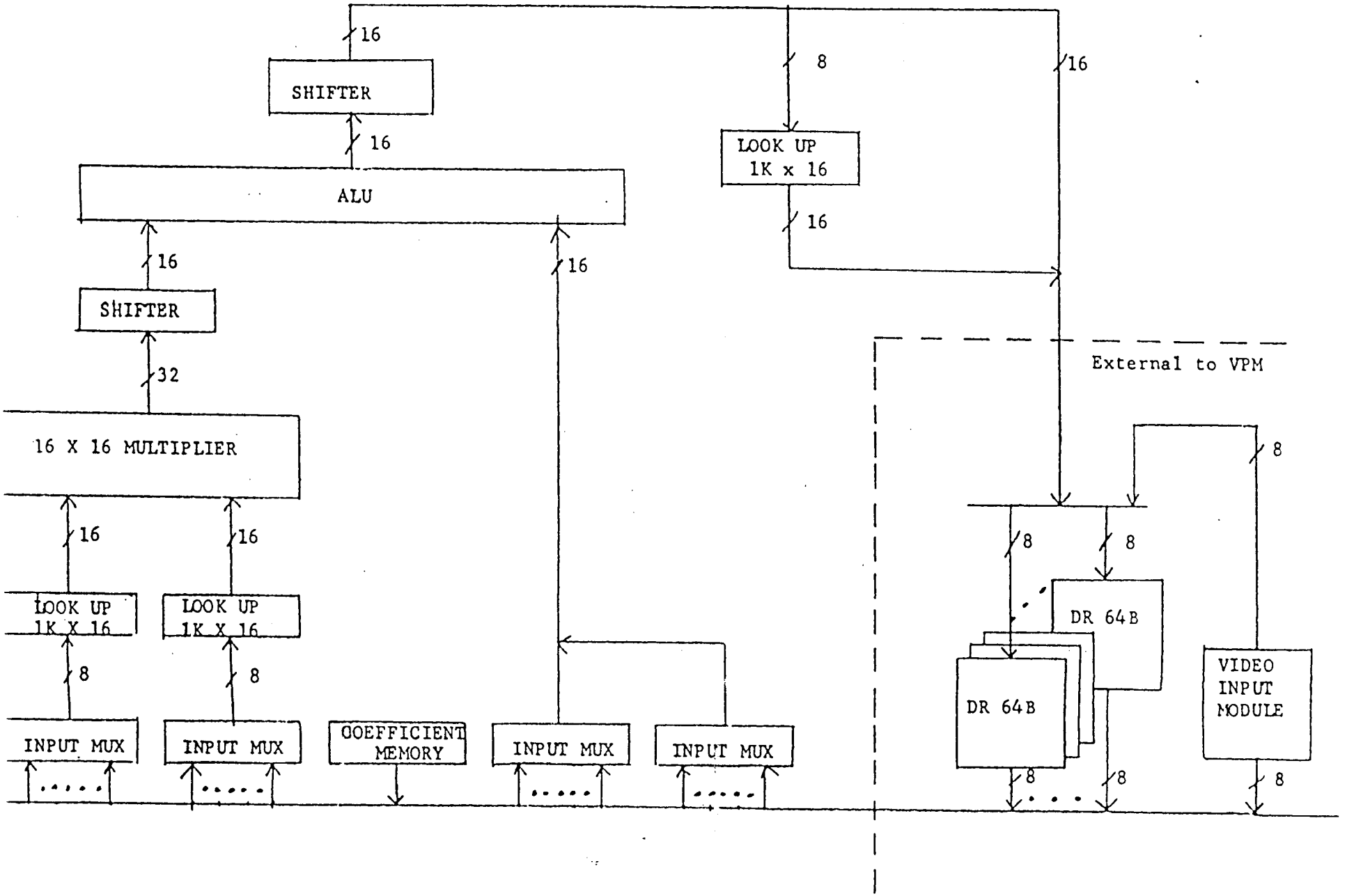
VPM--VIDEO PROCESSING MODULE

The VPM Video Processing Module adds a variety of image processing capabilities to the IKONAS GRAPHICS display system. Image addition, subtraction, multiplication, scaling, and look-up type corrections can be accomplished in one frame time. High precision digital filtering can be performed at very high speeds, e.g. filtering with a 3 x 3 coefficient matrix is performed in less than one third of a second.

The VPM features a 16 x 16 bit hardware multiplier and 16 bit ALU for exceptional processing precision at 10MHz rates. The unit is controlled by registers set via the IKONAS BUS from a host computer or internal processor.

Each of the inputs to the VPM may be chosen from any DR 64B image memory module (512 x 512 x 8) in the system, an 8 bit video input A/D converter (VI 8), or an internal 1K x 16 coefficient memory. Each 8 bit input to the multiplier stage of the VPM addresses a 1K x 16 look-up memory which feeds a 16 x 16 bit 100 nsec hardware multiplier. (Division can be accomplished by using the look-up memory to generate reciprocals.) The multiplier results feed a shifter which in turn provides one of the 16 bit inputs to the ALU. The second input to the ALU comes directly from either one of the DR 64B modules, the video input, or the coefficient memory.

The ALU output of 16 bits can be stored directly back into two DR 64B modules or a shifter can choose 8 bits of the results to feed an additional 1K x 16 look-up table. The 8 or 16 bit results can then be stored back in either one or two DR 64B modules.



IKONAS

VPM--Video Processing Module
Block Diagram

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MA 1024 - Multiplier Accumulator

The Multiplier Accumulator, MA 1024, is a microprogrammable hardware multiplier module. Designed to efficiently perform 3-D point transformations and shading calculations, the module must be used in conjunction with at least one dual ported Static RAM module. The on-card 1K x 16 coefficient memory supplies one multipler input; data read from the dual ported Static RAM under MA 1024 control supplies the second input. Products, or accumulations of products, may be read by the IKONAS BUS (processor) or written back into the dual ported Static RAM under MA 1024 control. The /D option to the MA 1024 provides for the computation of "W" and it reciprocal, allowing perspective division to be performed. 3-D point transformations without perspective can be performed in less than 4 microseconds. Transformation with perspective division requires less than 6 microseconds.

IKONAS BUS INTERFACE TO MA 1024

IKONAS BUS may WRITE to the following locations on the multiplier:

- 1K x 16 Coefficient Memory (CM)
- 1K x 32 Microprogram Memory (MPM)
- Control Word Ø
  - Microprogram Memory Starting Address (8 bits)
  - Microprogram Memory Page (2 bits)
  - Coefficient Memory Starting Address (8 bits)
  - Coefficient Memory Page (2 bits)
- Control Word 1
  - Static RAM Input Address (15 bits)
  - Static RAM Output Address (15 bits)
- Control Word 2
  - Loop Ø Counter Data (12 bits)

IKONAS BUS may READ from the following locations on the multiplier:

- 1K x 16 Coefficient Memory (CM)
- 32 bit XY Product Latch
- 32 bit ZS Product Latch
- 16 bit W

AUXILLARY BUS INTERFACE TO MA 1024

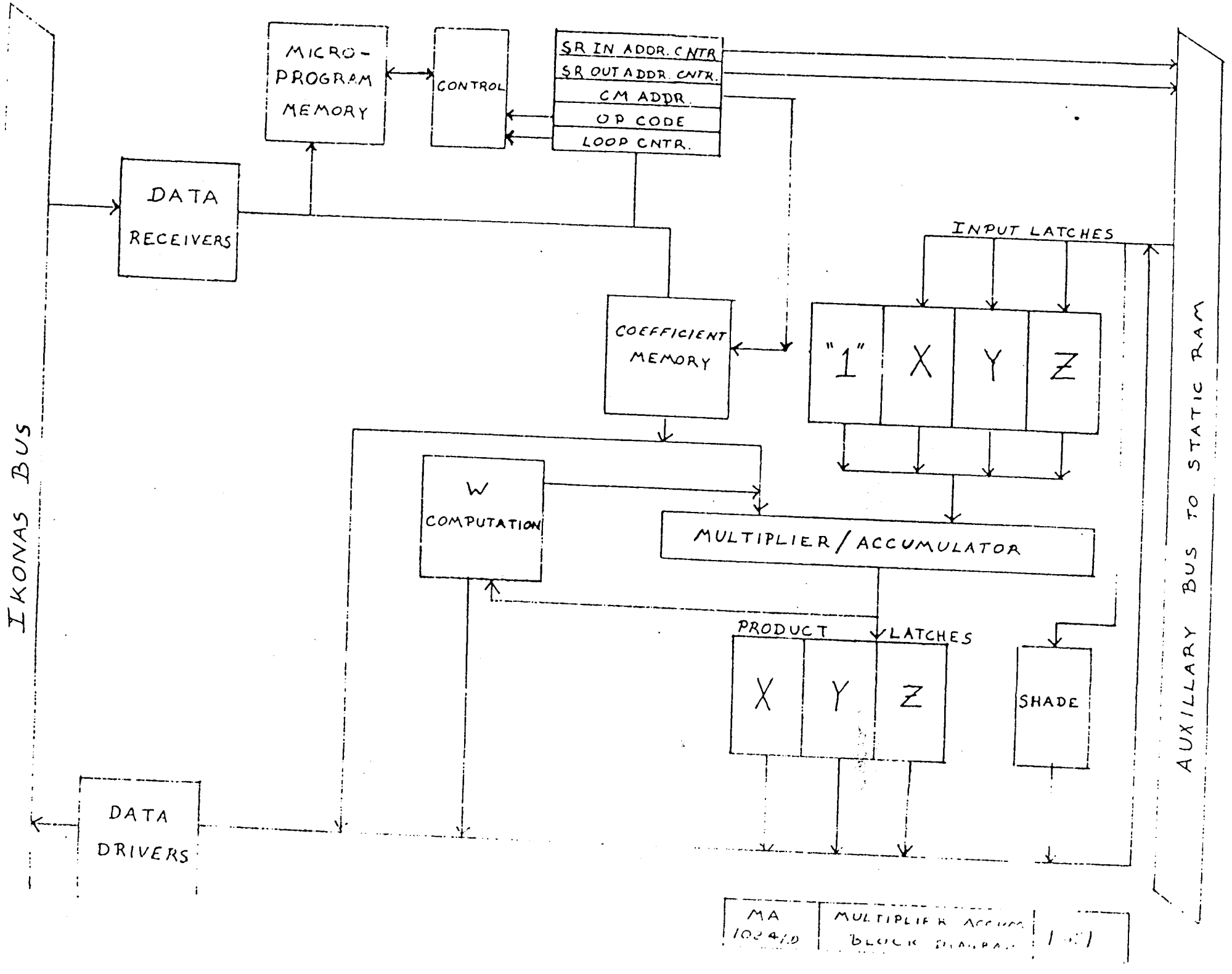
Any of up to 2^{15} Static RAM locations may be accessed by the MA 1024 via the AUX BUS. Static RAM input and output addresses are held in counters loaded from the IKONAS BUS and incremented under microcode control. Address source (input/output) is controlled by the Static RAM Read/Write line (SRW-L).

AUX BUS may WRITE to:

- 32 bit XY Input Latch
- 32 bit ZS Input Latch

AUX BUS may READ from:

- 32 bit XY Product Latch
- 32 bit ZS Product Latch



MA
1024/D
MULTIPLIER ACCUM
BLOCK DIAGRAM
1 of 1

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MPC--Multifunction Peripheral Controller

The Multifunction Peripheral Controller, MPC, is a versatile module combining external interfacing, data preprocessing, and simple interaction with the IKONAS display system on a single card. The user is provided a significant degree of flexibility and choice in both number and format of inputs. Available on the MPC are serial RS232 ports, TTL pulse ports, parallel (16 bit) digital ports, and analog ports. Each active interface is sampled by the on-board 16 bit microprocessor at video frame rates. Capabilities of the microprocessor extend the flexibility of the MPC by allowing the user access to simple display functions.

External MPC inputs include 16 parallel ports, three (optionally four) RS232 serial ports, and various analog port formats. Digitizing tablets can be interfaced either serially or in parallel depending on tablet specification. The user may specify either single-ended or differential analog inputs for use with control dials or similar inputs. Other system interactive devices which can be interfaced through the MPC system include a control switch array, joy sticks, and track balls.

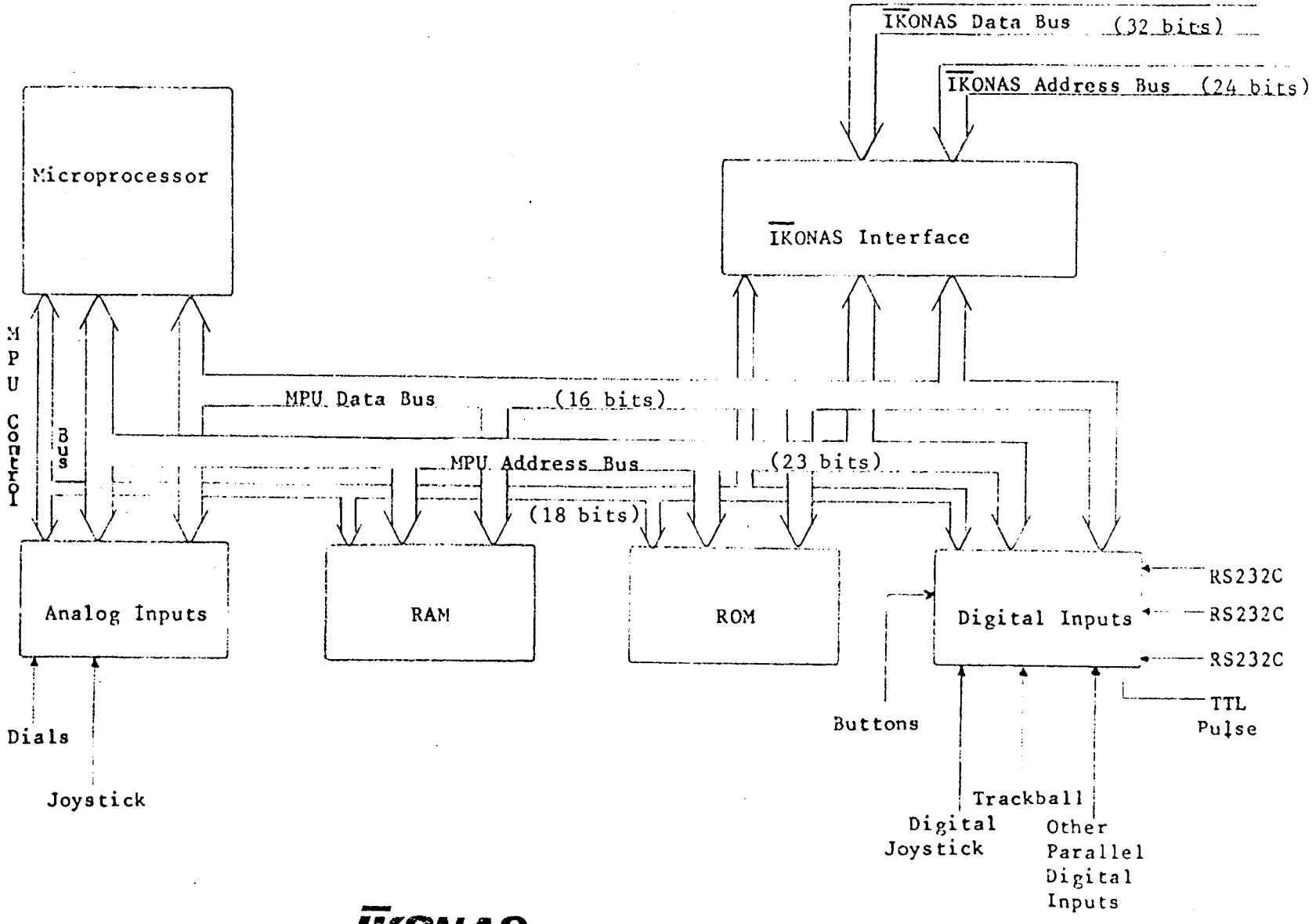
External device polling and user access to display functions are the primary tasks of the on-board microprocessor. Each active interface is interrogated at video frame rates and data can be either stored or preprocessed prior to its use within the IKONAS display system. Users can exercise some control over display functions such as pan, scroll, and zoom through the MPC. Further, control over both cursor location and format is available. The microprocessor is configured with ROM for system and display functions, sufficient RAM to allow for storage and preprocessing of data, a control terminal connection using a dedicated RS232 port, and interfaces to all of the external ports.

MPC INTERFACE PORT SPECIFICATION

SERIAL PORTS--RS232		
Number Dedicated		
Microprocessor terminal		1
Number Undedicated		
Standard MPCXXØ		2
Option MPCXX1		3
TTL PULSE PORTS		
Standard MPCØXX		Ø
Option MPC1XX		16
PARALLEL PORTS		
Number Inputs		16
Number bits/input		16
ANALOG/DIGITAL PORTS		
Number Inputs		
Standard-Single Ended	MPCXØX	16
Option-Differential	MPCX1X	8
	MPCX2X	16
Resolution		12 bits
Linearity		±1/2 LSB
Quantizing error		±1/2 LSB
A/D Range		
MPCXØX		Ø-1Ø volts
MPCX1X,MPCX2X		±1Ø volts

SAMPLE RATE

Minimum sample rate is system video frame rate which may be either 3ØHz or 6Ø Hz.



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MPC- Multifunction Peripheral Controller
Block Diagram

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MICROPROGRAM SEQUENCER CONTROL

Figure 1 is a block diagram of the MPS 16. Note the DATA FIELD REGISTER and the path from it to the LOOP COUNTER and the BMP 32. The CONTROL PROM, CONDITION CODE MULTIPLEXER, and the path from the MICROCODE LATCH to the IKONAS FUNCTION BUS are other important features. The sequencer, through the Am2911 and its related circuitry, uses the information in the microcode word and from the condition code lines to generate the 16 bit next address in the microprogram memory. Maximum size of the microprogram memory is 64K words, each 64 bits wide.

The lower 32 bits of a microcode word are inputs to the sequencer for next address selection. The bits are divided into the following fields:

DATA FIELD
OP CODE
CONDITION CODE SELECT
CONDITION CODE PARITY SELECT
LOAD CONTROL
IKONAS BUS FUNCTION CODE

DATA FIELD: Depending on the OP CODE and LOAD CONTROL bits, the 16 bit data field may be used as a pipeline address (D input to the 2911), ALU immediate data, or loop count.

OP CODE: The OP CODE determines what type of program control instruction is to be executed--that is, it addresses the CONTROL PROM which determines the next microcode address depending on the result of the condition code test. The Am2911 sequencer can output next microprogram address from one of four inputs: the data field (D), the 4 word on chip stack for subroutines and loops (F), the microprogram counter (PC), or an on chip latch which is loaded with the D data from the previous instruction (R). Features of the 2911 allow loops and subroutines to be executed with no overhead cycles. The CONTROL PROM has essentially the same instruction set as the Am2911A. Since the instruction set is in firmware, it can be changed or expanded.

CONDITION CODE SELECT: Condition codes are used to control conditional execution of the OP CODES. The condition code select bits choose 1 of 16 conditions to be tested. Presently implemented conditions are: counter=Ø, Host Request Line High, IKONAS BUS busy, IKONAS BUS or IMAGE MEMORY busy, Video Blanked, ALU overflow, ALU negative, ALU zero, and ALU carry out. Other specific condition codes can be easily added.

CONDITION CODE PARITY SELECT: This bit determines whether the conditional operation takes place on condition TRUE or condition FALSE.

LOAD CONTROL: Load Control determines whether the data field will be latched into the loop counter on the MPS 16 or into the immediate data register on the BMP 32.

IKONAS BUS FUNCTION CODE: This field controls read and write operations in Static RAM (32 bit parallel format), Dynamic RAM (512x512 or 1Ø24x1Ø24 format), or other special purpose devices (matrix multiplier, disk controller, etc.).

PROCESSOR CONTROL

In the processor block diagram, Figure 2, the important features are the 16 GENERAL PURPOSE REGISTERS, SELECTORS, and SHIFTERS within the 29Ø3, the R BUS SELECTOR and its sources, the Y BUS, the MDR, MAR, and IMMEDIATE DATA REGISTER and their paths to the IKONAS DATA and ADDRESS busses. The 16 general purpose registers are dual ported RAM with two independent address ports (A and B) and two independent output latches. Data may be written into the registers only using the B address port.

The 32 bits of microcode which are input to the processor are divided into the following fields:

R OPERAND SELECT
S OPERAND SELECT
ALU INSTRUCTION
ALU CARRY CONTROL
ALU SHIFT CONTROL
Y BUS SOURCE/DESTINATION
DR BUS DATA SOURCE
IKONAS BUS ADDRESS SOURCE
IKONAS BUS ENABLE

R OPERAND SELECT: This field selects one of the general purpose registers (Ø-15) or the R bus as the R operand. The field contains bits for A address and R bus select control. The R BUS data may be selected from the data registers (DR), lower 16 bits of DR, Memory Address Register (MAR), lower 16 bits of MAR, or the B register data in several forms: right rotated 8 or 16 bits, right shifted 8 or 16 bits.

S OPERAND SELECT: This field selects one of the general purpose registers (Ø-15) or the Q register as S operand. The B address bits within this field are also used to specify one of the general purpose registers as Y BUS output destination.

ALU FUNCTION: The IKONAS processor, using 8 Am29Ø3's, can perform 7 arithmetic and 9 logical operations on two 32 bit operands. In addition the Am29Ø3 can perform 9 special functions--principally multiplication, division, and normalization. See the Am29Ø3 data sheets for details of the available operations. This field also contains bits selecting shift type (logical or arithmetic) and direction (left or right) for the ALU shifter and Q shifter. Q register and B register write control are also contained in this field.

ALU CARRY CONTROL: Carry control circuitry is designed to allow operands to be treated as two 16 bit words or as one 32 bit word. In double 16 bit format $C_{in}Ø$ and $C_{in}16$ may be set to either 1's or Ø's. In 32 bit format, $C_{in}Ø$ may be set to Ø, 1, $C_{out}31$, or $C_{out}31$ inverted.

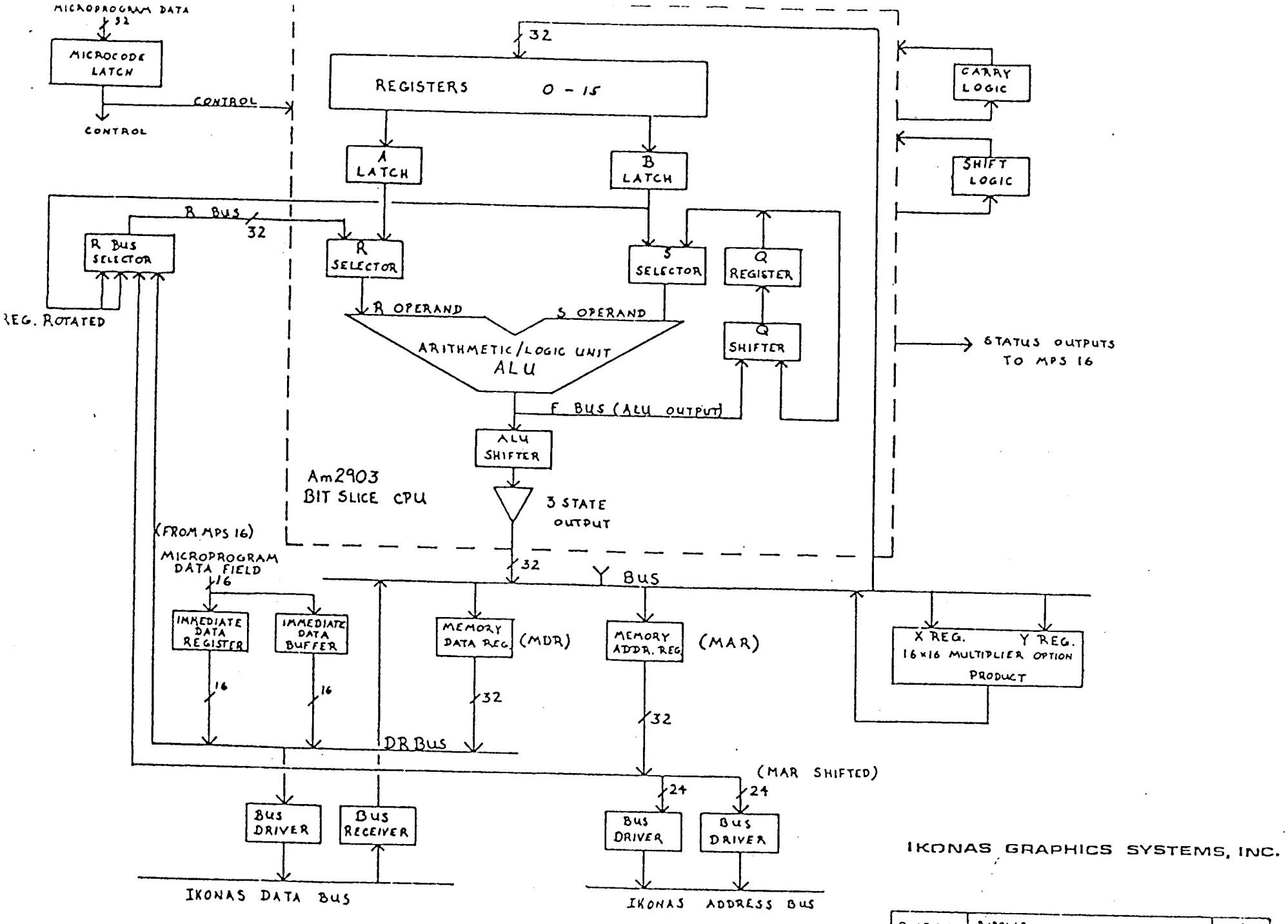
ALU SHIFT CONTROL: The ALU and Q shifters may be used to shift or rotate data. This field controls whether a shift or rotate is performed and whether the operations are long (64 bits using ALU and Q shifters as a unit) or short (using ALU and Q shifters as independent 32 bit units). The shift input (Ø or 1) is determined by this field. (Recall that direction and type of shift are controlled by the ALU FUNCTION field.)

Y BUS SOURCE/DESTINATION: The Y BUS is a communication path among the Am29Ø3 ALU general purpose registers, several special purpose registers, and an optional hardware multiplier. Possible sources of data on the Y BUS are the ALU output, the IKONAS BUS, and the multiplier output. Destinations possible are the general purpose registers (using the B address), the MDR, the MAR, and the multiplier inputs X and Y. When set up in the appropriate fields, the general purpose registers may be a second destination for data being written to the MDR, MAR, or multiplier inputs.

DR BUS DATA SOURCE: This field determines the data source for the DR bus. Data may come from the MDR or from the microcode data field for immediate operands.

IKONAS BUS ADDRESS SOURCE: For IKONAS BUS read and write cycles address data may come from the MAR directly or from the MAR shifted such that frame buffer X and Y addresses stored in upper and lower half words are packed into a single 24 bit address.

IKONAS BUS ENABLE: When set =1, this bit causes a Read or Write cycle on the IKONAS BUS.



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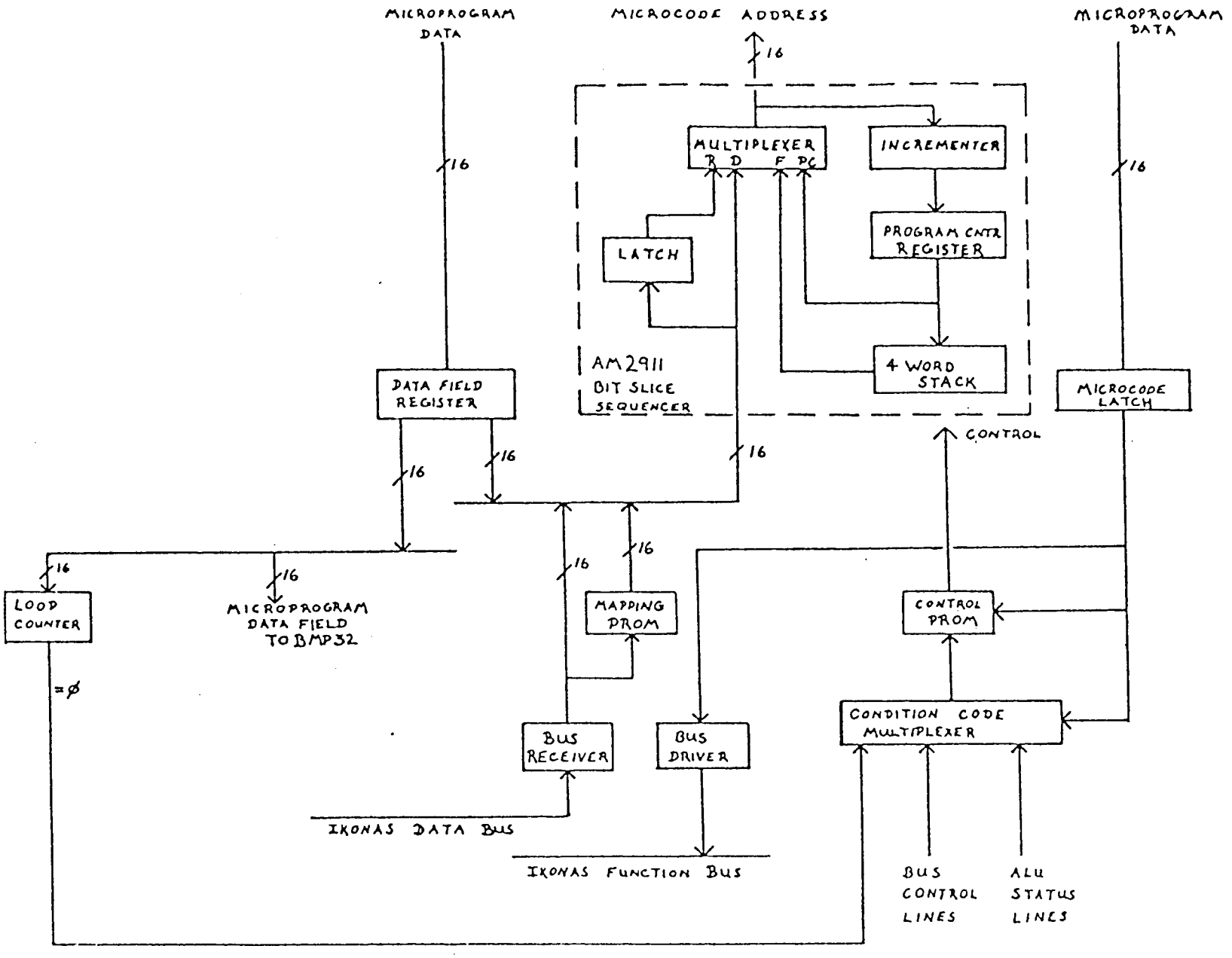
BMP 32	BIPOLAR MICROPROCESSOR BLOCK DIAGRAM	1 of 1 8/79



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MPS 16	MICROPROGRAM SEQUENCER BLOCK DIAGRAM	1 of 1 8/79