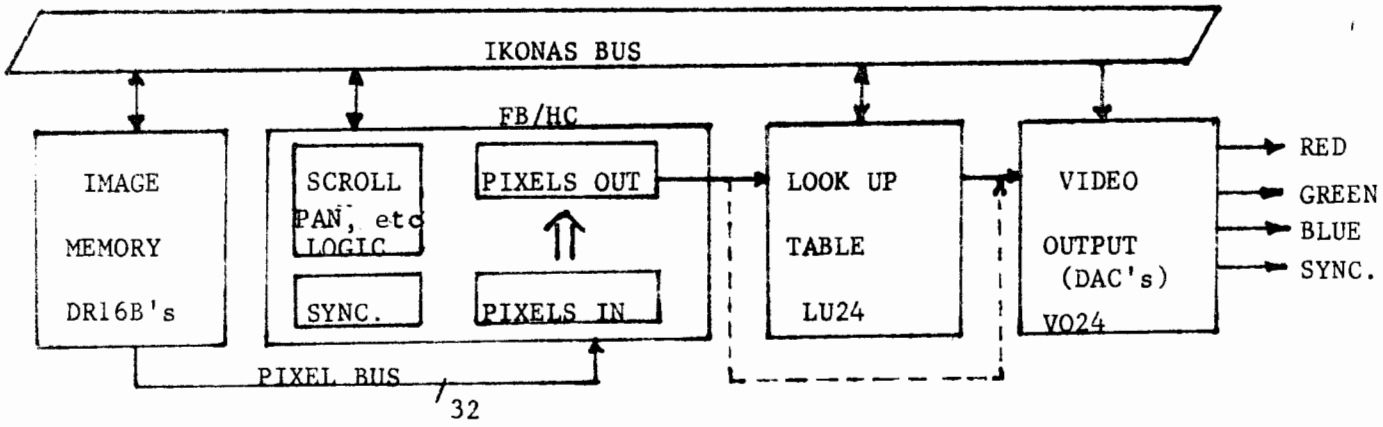
IKONAS GRAPHICS SYSTEMS INC
403 GLENWOOD AVE — RALEIGH NC 27603 — 919/833-5401

IMAGE MEMORY AND VIDEO CONTROL

IMAGE MEMORY

The image memory module, DR 16B, is a 16K x 32 dynamic RAM memory which may be addressed in 512 x 512 mode (2 bit planes/card) or 1024 x 1024 mode (2 cards/ bit plane). The image memory is ported to both the IKONAS BUS (read and write) and to the PIXEL BUS (read only). Cycle time of the DR 16B is 400 nsec. Each DR 16B has independent timing circuitry which allows a memory cycle to be initiated using only one 100 nsec IKONAS BUS cycle. The independent timing also allows memory accesses from the IKONAS BUS to be interleaved for higher data transfer speeds. Maximum transfer rate is 40 Mbytes/sec using interleaving.

Transparent refresh of the 16K dynamic RAMs, which occurs during the video horizontal refresh interval, is controlled by the FB/HC and requires 128 memory cycles every 2 milliseconds.



VIDEO REFRESH

The FB/HC controls transparent refresh of the video display. Allowing for display refresh, average memory access time rises to 533 nsec, resulting in a 7.5 Mbyte/sec host transfer rate, non-interleaved, or 30 Mbyte/sec transfer rate with interleaving.

The FB/HC accesses all image memory modules simultaneously and the output of the image memories feeds a double buffered PIXEL BUS. For each memory access, 32 bits are latched at the PIXEL BUS port of each DR 16B. In 512 mode these

bits represent 2 bits/pixel for 16 pixels with a maximum of 32 bits/pixel. The PIXEL BUS transfers data at the pixel rate from the image memories to the FB/HC.

In 1024 mode, the PIXEL BUS acts as 2 separate 16 (optionally 24) bit busses, one for odd pixels, one for even pixels. Each memory access fetches data for 64 pixels at a time (32 pixels/card, 2 cards/bit plane). Data for 2 pixels at a time is latched on the FB/HC and is passed out in appropriate order at 1024 pixel rate.

PAN, SCROLL, ZOOM, WINDOW, VIEWPORT, and HARDWARE CURSOR

Logic on the FB/HC controls pan, scroll, and zoom by generating appropriate image memory addresses. Pan and scroll occur in pixel increments. Zoom ratios are integer from 1:1 to 256:1. Image Memory window and display screen viewport parameters are controlled by setting registers on the FB/HC from the IKONAS BUS. As with other control registers in the IKONAS system, these registers appear as memory locations from the IKONAS BUS. The hardware cursor displays a full screen cross hair cursor intersecting at the desired location.

VIDEO OUTPUT

Output from the FB/HC is used as input to digital to analog converters (DACs) which produce video signals for a monitor, or as input to a color look-up table. Eight bit DACs are standard; 10 bit DACs are an available option. The FB/HC accepts up to 32 bits/pixel from the PIXEL BUS and outputs up to 32 bits/pixel. Four mappings from input to output are possible and are user specified. Standard mappings might be 8 (10) bits input mapped identically to three 8 (10) bit outputs to allow display of grey shade images (equal components of red, green, and blue), or three 8 (10) bit inputs mapped to three 8 (10) bit outputs--8 (10) bits each red, green, and blue.

Output from the FB/HC can be used to address a color look-up table whose outputs are then used as inputs to the DACs. The standard look-up table, LU 24, is organized as three 1K x 8 (10) look-up tables. Use of an 8 bit in, 10 bit out color map allows gamma correction curves to be implemented in the video output. Color map organization is very flexible and input from the FB/HC may be apportioned to the map in numerous ways.