UNCLASSIFIED

LESSON PLANS

for

SIDEBAND GENERATOR

MODEL SBG-1

THE TECHNICAL MATERIEL CORPORATION
MAMARONECK, N.Y. OTTAWA, ONTARIO

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REVISED OCT. 1966
PAUL GROVE

NOTICE

I N D E X

TITLE: TMC Synthesized Sideband Generator System

OBJECTIVES:

a) to discuss, by means of a block diagram, the TMC synthesized sideband generator system, in order that overall operation may be visualized.

b) to illustrate the versatility of various units of the system in combination, and to discuss the nomenclature of such combinations.

REFERENCES:

a) TMC Short Form Catalog

b) Technical Manual for Sideband Generator SBG-1 or SBG-2 (Modulator-Oscillator Group AN/URA-30)

TRAINING AIDS:

a) Chalkboard and associated materials.

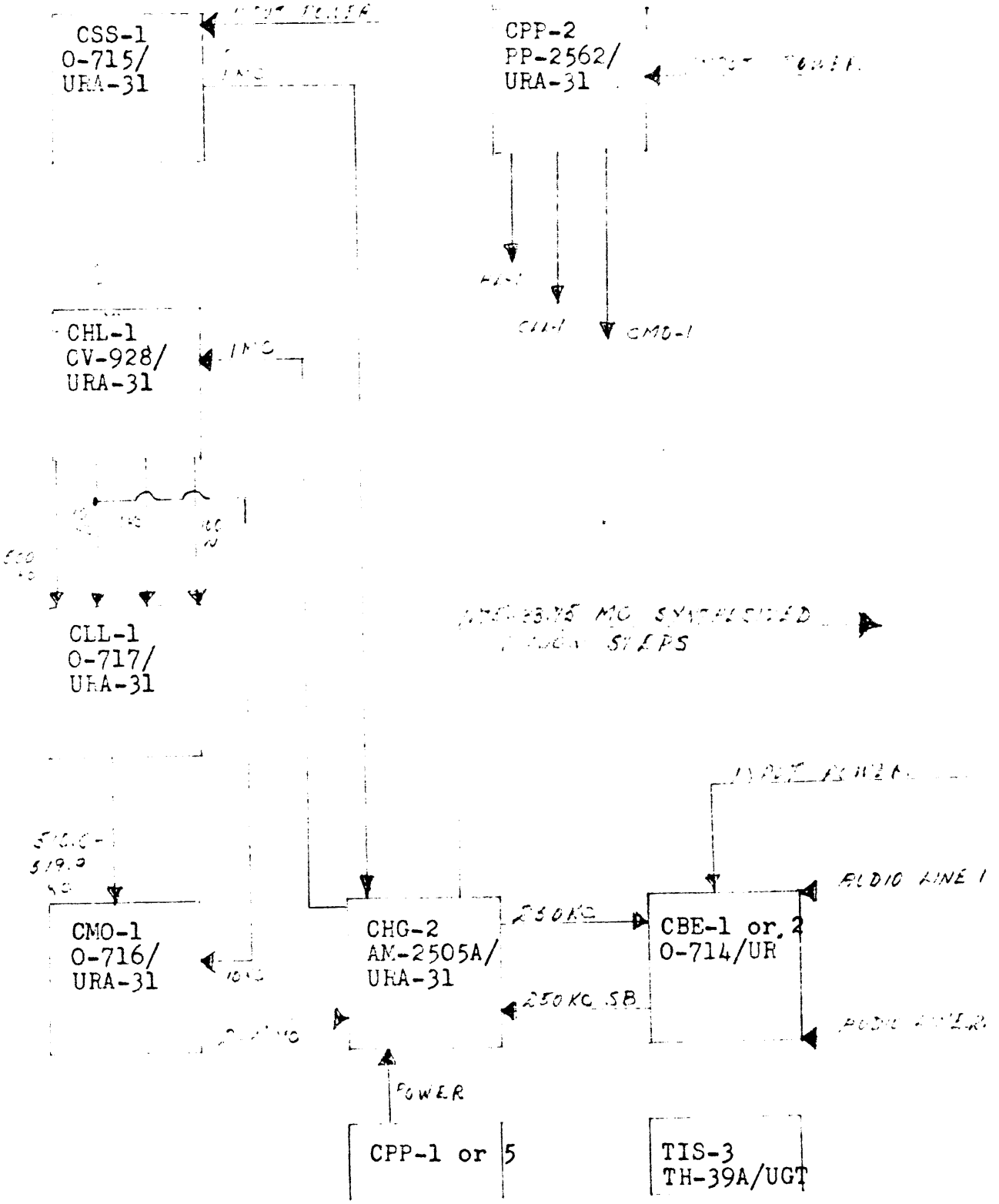
b) Sideband Generator Rack, connected for operation.

Revised: Oct. 1966

Paul E. Grove

PRESENTATION:

A. Block Diagram of the Sideband Generator System:



B. Discussion of the Sideband Generator System Using the Block Diagram:

1. The heart of the system is the one megacycle frequency standard, Model CSS-1. This transistorized unit has a self contained power supply. The output, at 1 mc, is accurate to 1 part per 100,000,000 per day. The 1 mc output is delivered to Frequency Amplifier Model CHG-2, where it is amplified, then sent to the Frequency Divider Chain, Model CHL-1.

2. The Frequency Divider Chain, Model CHL-1, contains circuits which count down the 1 mc input to provide outputs at 500 KC, 10 KC, 1 KC and 100 CPS, all locked to the standard.

3. Controlled Oscillator Model CLL-1 receives inputs at 500 KC, 10 KC, 1 KC and 100 CPS from the CHL-1. The CLL-1, by means of three synthesizer loops, provides an output in the range of 510.0 - 519.9 KC, in 100 cycle steps. Two front panel controls, the KILOCYCLES control and the HUNDREDS control determine the exact output in the 510.0 to 519.9 KC range.

4. Controlled Master Oscillator Model CMO-1 receives the 510.0 to 519.9 KC signal from the Model CLL-1, together with a 10 KC signal from the Model CHL-1. This unit contains a well designed variable frequency oscillator with an associated vernier dial and counter, operable over the range of 2 to 4 mcs. A 100 KC crystal oscillator circuit is also incorporated for calibration purposes. The remainder of the CMO-1 circuitry utilizes the frequencies obtained from the CLL-1 and the CHL-1 to synthesize the 2 to 4 mc oscillator in 100 cycle steps.

5. The Sideband Exciter Model CBE-1 or CBE-2 receives audio inputs from two channels and a 250 KC sub-carrier from the Model CHG-2. The output of the sideband exciter depends on the settings of various controls and the type of operation desired. It may be a 250 KC sub carrier, or single, double or independent sideband transmission with various degrees of carrier re-insertion, at a nominal frequency of 250 KCS. The output of the CBE is sent back to the Frequency Amplifier Model CHG-2.

6. Frequency Amplifier Model CHG-2 receives:

   a) a 2 to 4 mc input from the CMO-1, synthesized in 100 cycle steps.

   b) a 1 mc input from Frequency Standard Model CSS-1

c) a subcarrier or sideband input at 250 KCS from Sideband exciter Model CBE-1 or CBE-2.

The Model CHG-2 frequency translates the 2-4 mc synthesized input from the Model CMO-1, and the input from the Model CBE sideband exciter, to provide a sideband output in the range 1.75 to 33.75 mcs, synthesized in 100 cycle steps. Power for the Model CHG-2 is supplied by either a Model CPP-1 or a Model CPP-5 power supply, depending on the transmitter model.

7. Shown unconnected is the Tone Intelligence Unit, Model TIS-3. (TH-39A/UGT) This unit may be interconnected with the sideband exciter, Model CBE, to provide FAX, FSK, or CW operation.

C. Nomenclatures:

The units described are available in many combinations and arrangements. For details on nomenclature, consult TMC catalogs and Sales Bulletins.

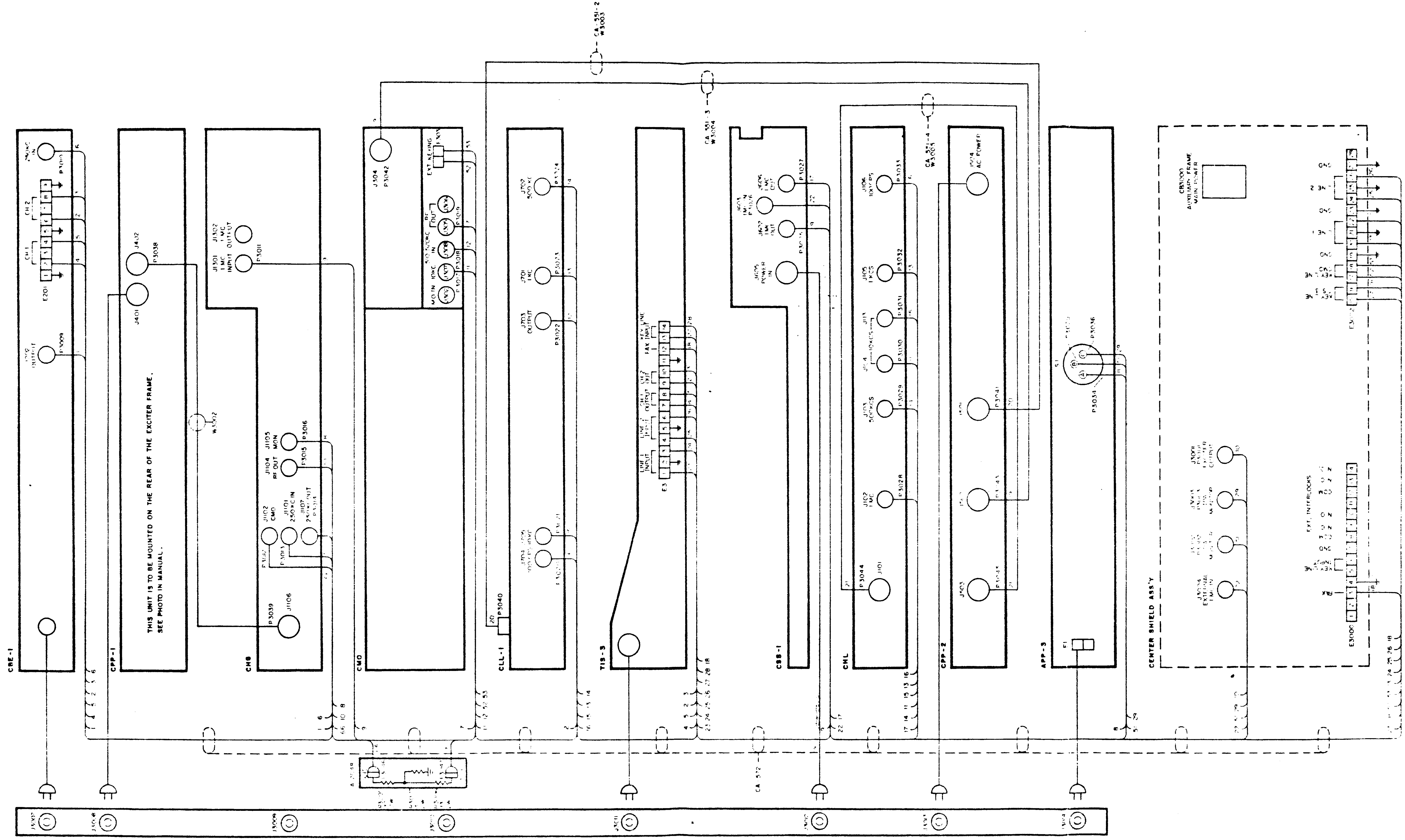
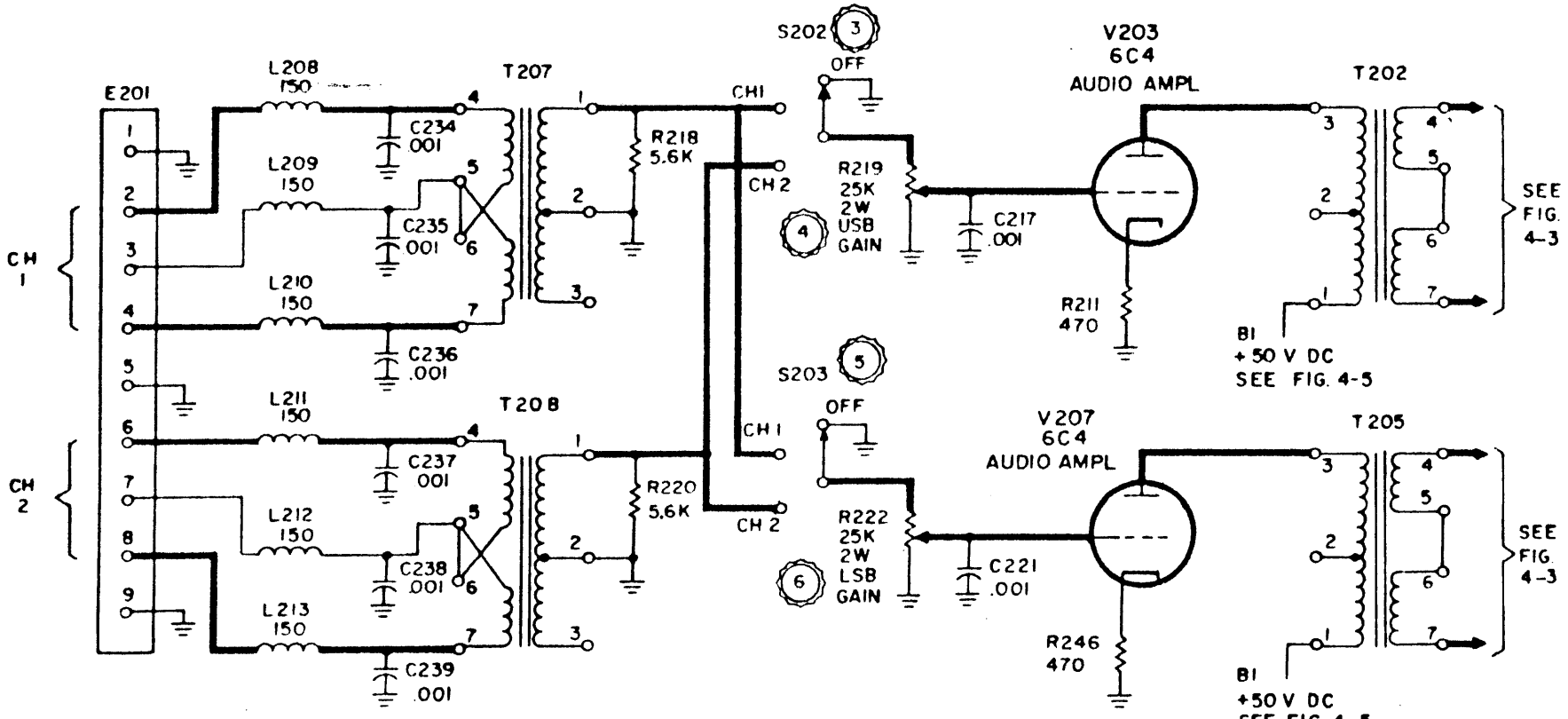


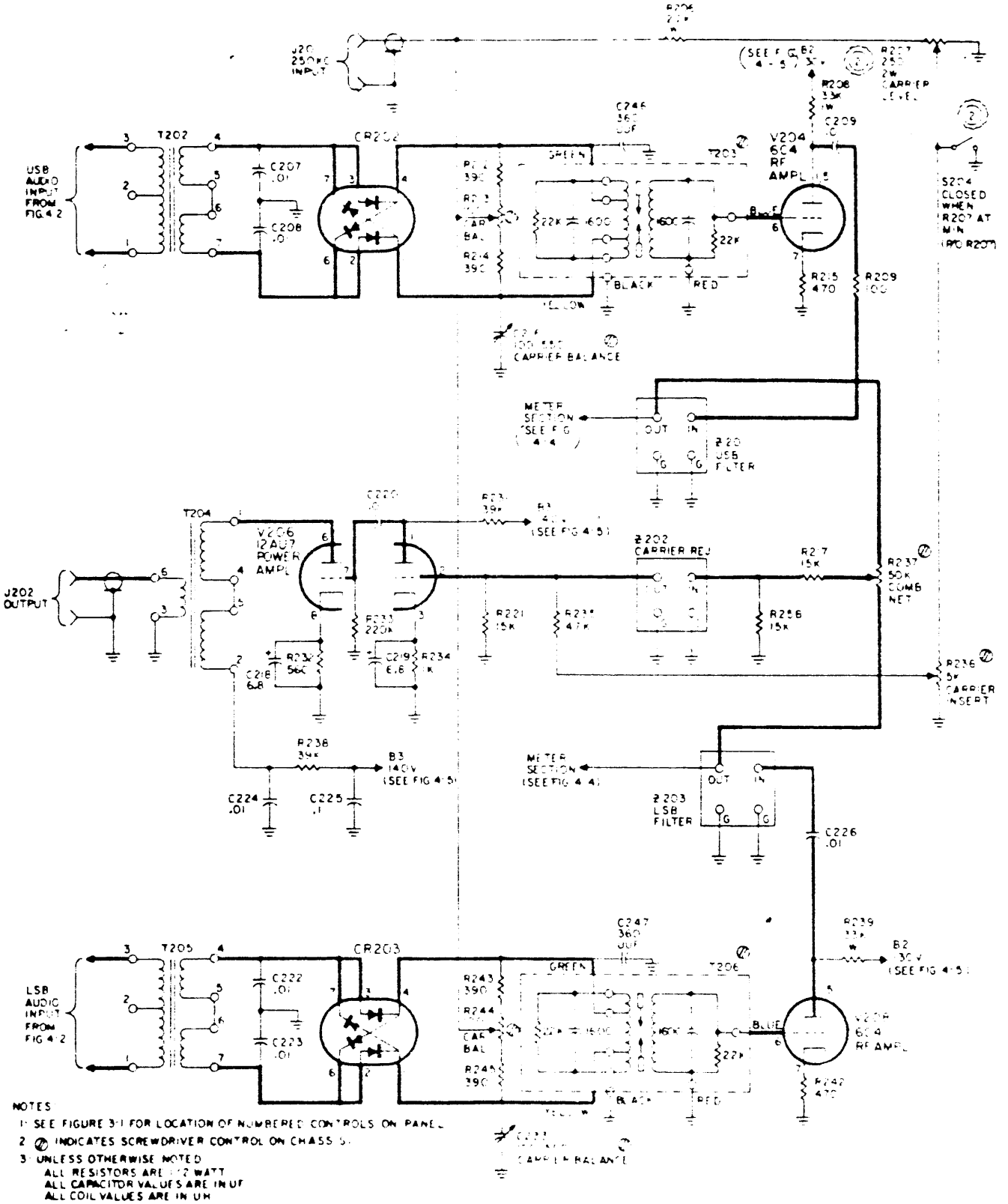
Figure I-2-1. Wiring Diagram Showing Interconnection of SBG-1 Rack Mounted Units for GPT-10K and GPT-40K Transmitters



NOTES—

1. SEE FIGURE 3-1 FOR LOCATION OF NUMBERED CONTROLS ON PANEL.
2. UNLESS OTHERWISE NOTED—
   ALL RESISTORS ARE 1/2 WATT.
   ALL CAPACITOR VALUES ARE IN UF.
   ALL COIL VALUES ARE IN UH.

Figure 4-2. Simplified Schematic Diagram, Audio Input Section



NOTES:

1. SEE FIGURE 3-1 FOR LOCATION OF NUMBERED CONTROLS ON PANEL.
2. ⓥ INDICATES SCREWDRIVER CONTROL ON CHASSIS.
3. UNLESS OTHERWISE NOTED:
   - ALL RESISTORS ARE 1/2 WATT
   - ALL CAPACITOR VALUES ARE IN UF
   - ALL COIL VALUES ARE IN UH

Figure 4-3. Simplified Schematic Diagram 250-Kc Input And Balanced Modulator Section

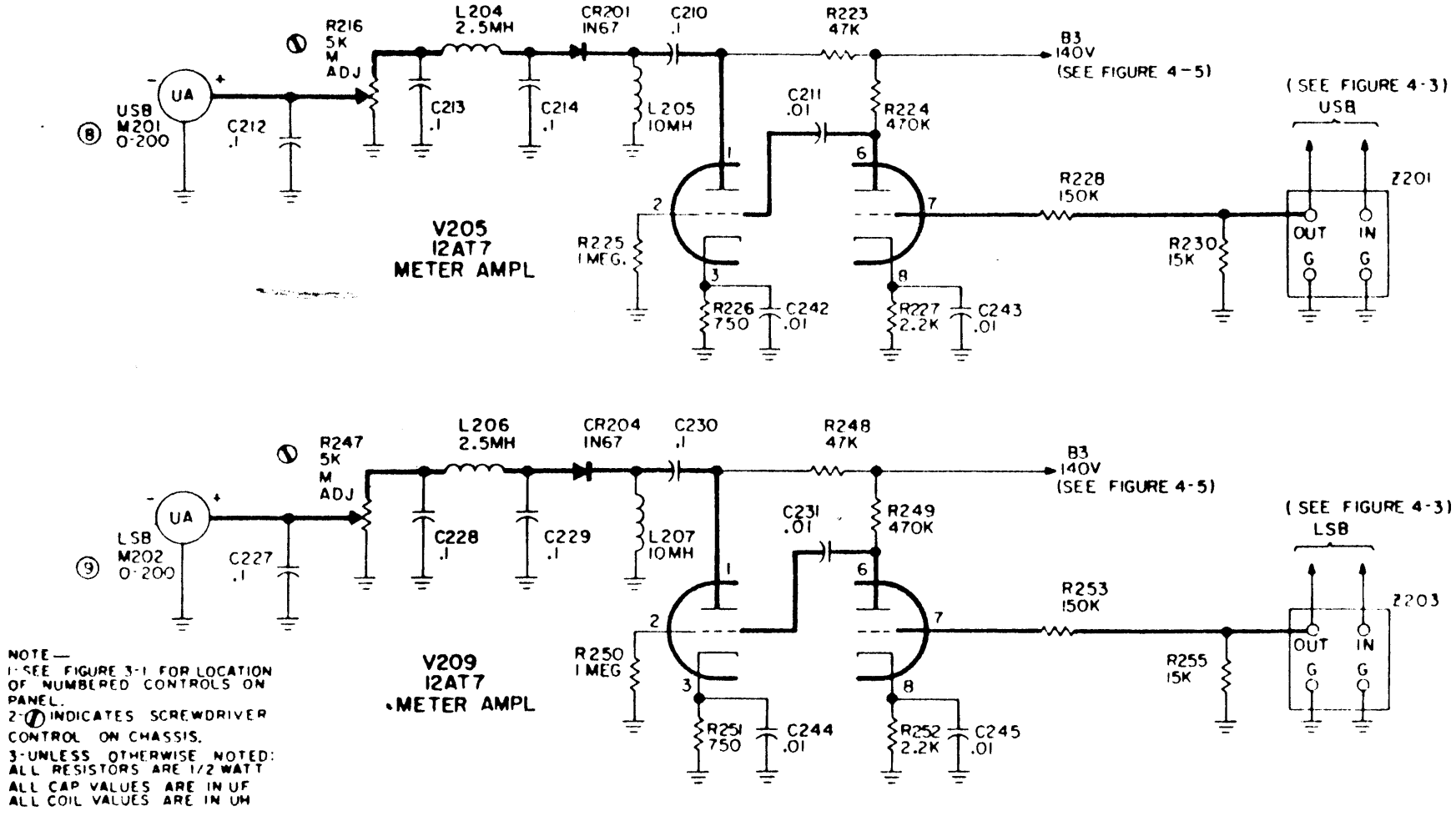


Figure 4-4. Schematic Diagram, Meter Section

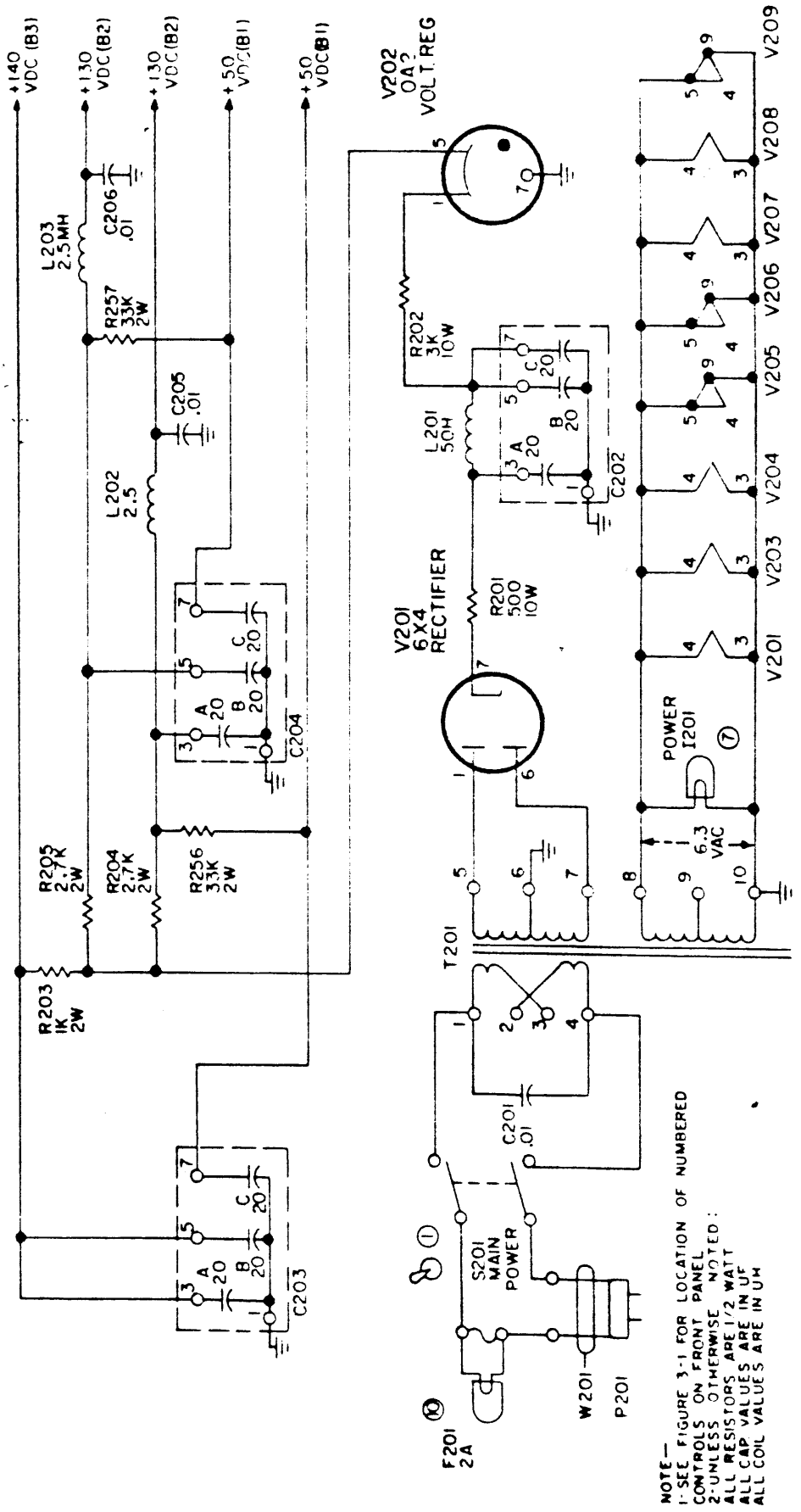


Figure 4-5. Schematic Diagram, Power Supply Section

SECTION 1

TITLE: TMC Phase Detector Circuit

OBJECTIVES:

a) to explain the operation of the phase detector circuit used throughout TMC transmitting and receiving equipment.

b) to stress the importance, simplicity and versatility of the circuit.

REFERENCES:

a) Technical Manual for Sideband Generator SBG-1 or SBG-2 (Modulator-Oscillator Group, AN/URA-30). (Section 4)

b) Technical Manual for Sideband Converter Model SBC-1 or SBC-2. (AN/URA-42) (Section 4)

TRAINING AIDS:

Chalkboard and associated materials.

PRESENTATION:

(Following figure to be sketched on chalkboard)

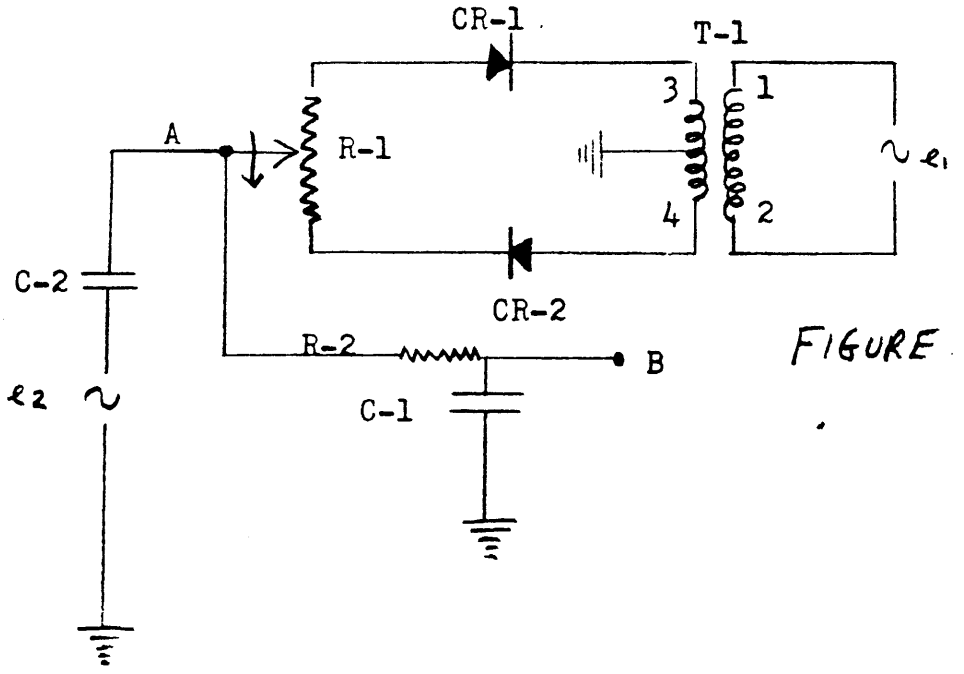


FIGURE #1

A. General Discussion:

1. The purpose of the phase detector circuit is to compare the phase difference between two nominally identical frequencies and to produce a correction voltage proportional to the amount of phase error.

2. One input to the phase detector is locked to an accurate frequency standard or reference; this is termed the "reference" or "standard" input.

3. The second input to the phase detector is an independent oscillator or source whose frequency it is desired to control.

4. The correction voltage produced by the phase detector is passed to control circuits, which act to correct the frequency of the independent oscillator or source.

5. In the typical TMC phase detector circuit, the two frequencies are "locked in" when their phase difference is plus or minus 90 degrees. In this situation the average correction voltage produced by the phase detector is zero.

6. When the frequency of the independent oscillator drifts by an extremely small amount, a change of phase is seen by the phase detector, which immediately produces a correction voltage of the proper polarity and amplitude to correct the frequency of the independent oscillator.

7. The phase difference between the reference frequency and the independent oscillator or source is continuously changing by small increments, but the average frequency of the independent oscillator is kept constant.

B. Circuit Operation: (refer to figure #1)

1. An AC voltage, el, is applied to T1; this is the reference or standard input signal, locked to an accurate reference. This voltage is developed across terminals 3 and 4 of T1, which is centertapped to ground.

2. When terminal 3 of T1 is positive, diodes CR-1 and CR-2 are back biased and no current flows in R-1. At point "A" is a high impedance to ground. When terminal 3 of T-1 is negative, diodes CR-1 and CR-2 conduct, developing a voltage across R-1.

3. At the electrical center of R-1, with CR-1 and CR-2 conducting, there appears an effective ground, because of the centertapping of T-1. Thus, with conduction through R-1, the wiper is at ground if moved to electrical center, and any signal at point A will be lost.

4. The correction voltage is developed at point A. This correction voltage is a portion of e2, the voltage of the independent oscillator, also connected at point A.
Whether this voltage is allowed to appear or not depends on the phase relationship between e2 and el.

5. A simple relationship is given as an aid in analyzing the waveforms on the following page:

   a) when el is positive at terminal 3 of T-1, e2 will be developed at point A.

   b) when el is negative at terminal 3 of T-1, point A is grounded and e2 will not be developed at point A.

C. Adjustment of Phase Detector Balance Pot, R-1:

1. Remove input e2.

2. Connect a zero center scale VTVM at point A. Set meter for low DC voltage.

3. Have input el operating.

4. With R-1 fully CCW, maximum negative voltage will be read. As R-1 is moved in a CW direction, the negative voltage will decrease. At electrical center, the voltage will be zero.
As the pot is moved CW beyond electrical zero, the voltage will be positive; finally, at full CW position, the voltage will be maximum positive.

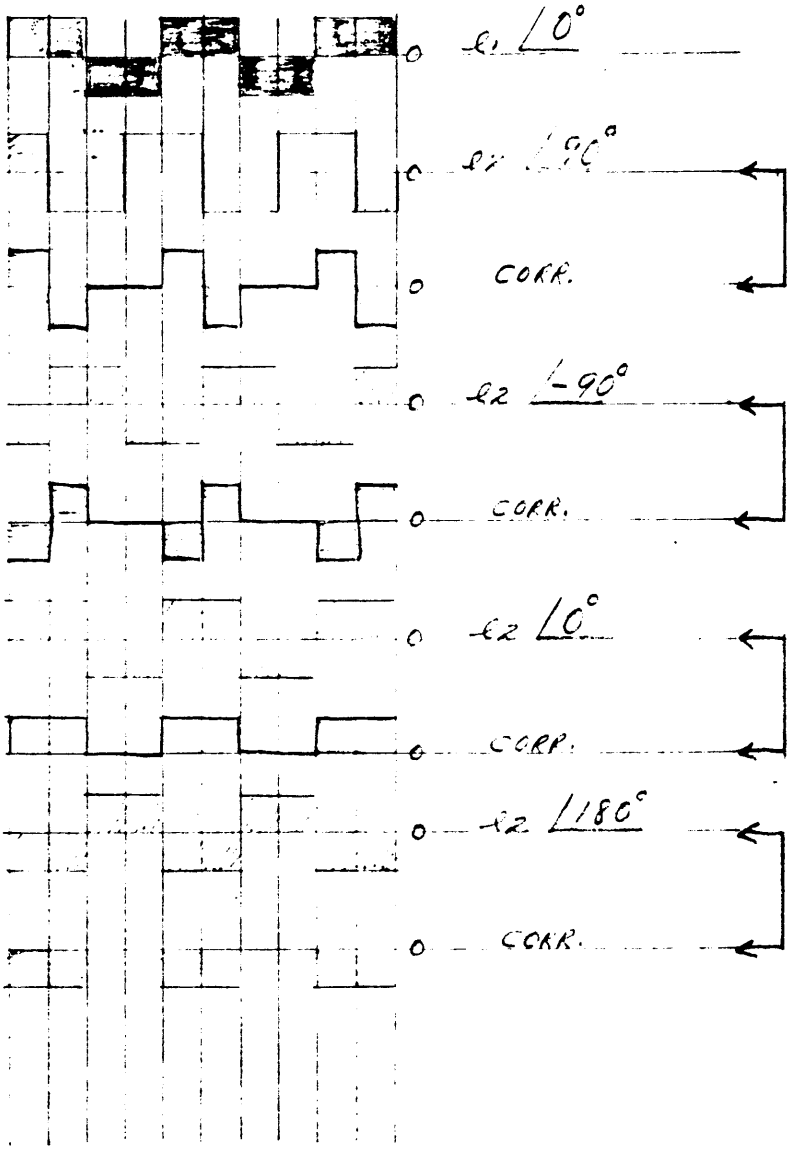
5. Set R-1 for zero volts. (electrical zero)

6. Re-connect input e2.

D. A Plot of Correction Voltage versus Phas Difference:

The fcllowing plot shows el, the standard, at a phase angle of 0 degrees, with e2, the second input, at various phase angles with respect to el. Relative values of correction voltage are shown.

For simplicity, the voltages are shown as square waves, even though, in actual practice, most inputs are sinusoidal. This in no way detracts from the validity of the analysis.



SECTION 2

TITLE: Primary Frequency Standard Model CSS-1 (O-715/URA-31)

OBJECTIVES:

a) to describe the role of the frequency standard in the Controlled Precision Oscillator system.

b) to discuss the circuitry of primary standards CSS-1 and CSS-1A, pointing up the differences in the two models.

c) to demonstrate, with appropriate test equipment, the alignment of the unit.

REFERENCES:

a) Technical Manual for Model CSS-1 (O-715/URA-31)

b) TMC Production Specification #S-490 (CSS-1)

c) TMC Production Specification #S-658 (CSS-1A)

d) Schematic CK-441 (CSS-1)

e) Schematic CK-559) (CSS-1A)

TRAINING AIDS:

a) Model CSS-1, set up for operation.

b) Frequency Counter H.P. 524C.

c) Oscilloscope.

d) H.P. VTVM 410B or equivalent.

PRESENTATION:

A. General Discussion:

1. Primary frequency standard Model CSS-1 is a dependable stable crystal oscillator having an accuracy of 1 part per 100,000,000 per day.

   a) Output frequency is 1 mc.

   b) Output amplitude is nominally 1.0 V RMS

   c) Output impedance is nominally 72 ohms.

2. The accuracy of all synthesizing circuits in the Controlled Precision Oscillator system is derived from the CSS-1.

3. Connections:

   a) J-605: Power input

   b) J-602: 1 mc output to CHG unit.

   c) J-606: 1 mc output to CHL unit.

   d) J-603: 1 mc input for comparison.

   e) J-601: 1 mc output to front panel for monitoring.

   f) J-604: 1 mc input at front panel for comparison.

   Note: On units now being shipped, the 1 mc output of the CSS-1 unit is sent first to the CHG unit, where it is amplified and then directed to the CHL unit.

B. Discussion of Circuitry: (Model CSS-1)

1. Power Supply:

   a) a conventional full wave bridge circuit is employed.

   b) L-603 and C-608 form an LC ripple filter.

   c) Cable W-601 is always connected, and the rectifier circuit operates continuously.

   d) at the junction of CR-601 and R-618 will be measured approximately plus 28 V DC.

e) at terminal #3 of sealed unit Z-602 will be measured plus 28 Volts. This voltage is applied at all times to insure oven stabilization.

f) at the "high" side of C-610 will be measured approximately 20 volts.

g) when S-601 is in the "standby" position, B plus is removed from all circuitry except the oven, and standby indicator I-601 is lighted.

h) when S-601 is in the "power" position, B plus is applied to transistor amplifiers Q-601, Q-602 and Q-603. The "power" indicator, I-602, is lighted.

i) Zener diode CR-601 is used to protect transistor circuitry from abnormally high voltages.

2. Sealed Crystal Unit Z-602:

a) sealed unit Z-602 contains a James Knights 1 mc crystal transistor oscillator circuit and a proportional oven. Oven heat varies with crystal temperature.

b) a hatch at the top of the unit provides acess to the frequency adjustment. This is a factory adjustment only, and should not be disturbed.

c) power is applied continuously to the oven; however, from a cold start, a 1 hour warmup is required.

d) at terminal #6 of Z-602 will be measured about 2.0 V RMS.

3. Transistor Amplifier Circuits:

a) Transistor amplifiers Q-601 and Q-602 are conventional circuits, in a parallel connected common emitter configuration. The collectors ar tied together at the red terminal of filter T-603.

b) Filter T-604 is peaked at 1 mc. When peaked, the 1 mc voltage at the blue terminal of T-604 is about .8V RMS.

c) R-617 is the output adjust potentiometer. The full output of T-604 is delivered to phase comparator amplifier Q-603. The signal input to parallel amplifiers Q-601 and Q-602 is adjusted by R-617.

d) T-603 is an additional filter peak d at 1 mc. The 1 mc output is applied to J-602 and J-606 directly, and to front panel jack J-601 through a 2200 ohm isolating resistor.

4. Phase Comparator Circuit:

a) the full output of T-604 is applied to conventional common emitter transistor amplifier Q-603. The output, taken from the collector, is applied to a phase comparator circuit.

b) the second input to the phase comparator circuit is also a 1 mc signal; this signal may be superior or inferior to the internal 1 mc signal; but, in any case, the sealed unit Z-602 should not be tampered with.

c) if the two 1 mc signals are near coincidence, their phase difference will cause meter M-601 to sweep; the number of sweeps per second is determined by the difference between the two signals in cycles per second.

d) when the two 1 mc signals are exactly in coincidence, meter M-601 will remain stationary at some point, not necessarily zero.

e) the RMS value of the applied external 1 mc signal must not exceed 1 volt. When the signal exceeds 1 volt, attenuator pad R-621, R-622, R-623 must be made up and connected at the points shown.

f) the sensitivity control, R-616, is adjusted from the front panel for the convenience of the operator, according to the amplitude of the external 1 mc signal, to prevent pinning the meter.

5. Notes concerning Standard Model CSS-1A:

The instructor should now call attention to the schematic of standard Model CSS-1A, pointing out the minor differences in the models, among these:

a) T-604 has been replaced by a transistor emitter follower stage. (Coupling capacitor C-612 added)

b) Output adjust pot R-617 value is changed from 1000 to 2500 ohms.

c) R-618 changed from 50 ohms to 33 ohms.

C. Alignment of Standard Model CSS-1:

1. Connect a 70 ohm load to J-602.

2. Place "Standby" "Power" switch, S-601, to "Power".

3. Turn output adjust pot, R-617, for maximum output.

4. Connect probe of VTVM at output (#6) of Z-602. The voltage should be about 2.0 V RMS.

5. Place the probe of the VTVM to the "high" side of R-617. Adjust T-604 for maximum reading. The voltage should be about .8V RMS. (not in newer units)

6. Place the probe of the VTVM across the 70 ohm load at J-602. Adjust T-603 for maximum output. The voltage should exceed 1.0 V RMS.

7. Place the probe of the VTVM on one of the yellow terminals of Z-601, and adjust the slug for maximum indication.

8. Place front panel sensitivity control R-616 in maximum sensitivity position. Adjust the phase detector balance pot, R-614, to bring the needle of meter M-601 to center scale.

9. If the step above has been performed correctly, the meter needle will not move from center scale as the sensitivity pot is moved to the minimum position.

10. Adjust R-617 for 1.0 V RMS out at J-602.

11. This completes the alignment of the unit.

D. Troubleshooting:

1. In general, the alignment procedure constitutes an excellent check on the general condition of the unit. However, several points are listed here which may be of value in tracing trouble.

2. The following readings were taken on a typical unit during production test: NOTE: UNIT IS CSS-1A

   a) L-603: plus 46 volts each side.

   b) Junction R-618, CR-601: plus 29 volts.

   c) C-611 pin #5: plus 20 Volts.

   d) C-612, both sides: 1.3V RMS.

   e) R-617 tap: minimum: 0V; maximum: 1.25V RMS

   f) J-602, J-606: 1.5V RMS with R-617 at maximum.

   g) Counter reading at J-602: 1 mc.

   h) Z-601: yellow: 1.6V RMS with Z-601 peaked.

3. Conduction balance of amplifiers Q-601 and Q-602 may be checked as follows:

   a) measure, with a high impedance VTVM, the DC voltage between B1, Q-601, and B2, Q-602. the polarity may be positive or negative, depending on the positions of the probes, but the voltage difference between these points should not exceed .1 volt.

   b) perform the step outlined above with E1 and E2, of Q-601 and Q-602, respectively.

   c) the actual voltage to ground from B1, B2, E1, and E2 is about plus 20 Volts.

SUMMARY:

The instructor should review the discussion of the Model CSS-1, emphasizing important adjustments and indications.
It should be strongly noted that the trapdoor adjustment on sealed unit Z-602 should not be tampered with.
If possible, a signal from WWV should be obtained and piped in to the phase comparator circuit for a class demonstration; in the absence of such a signal, a second CSS-1 unit should be used.

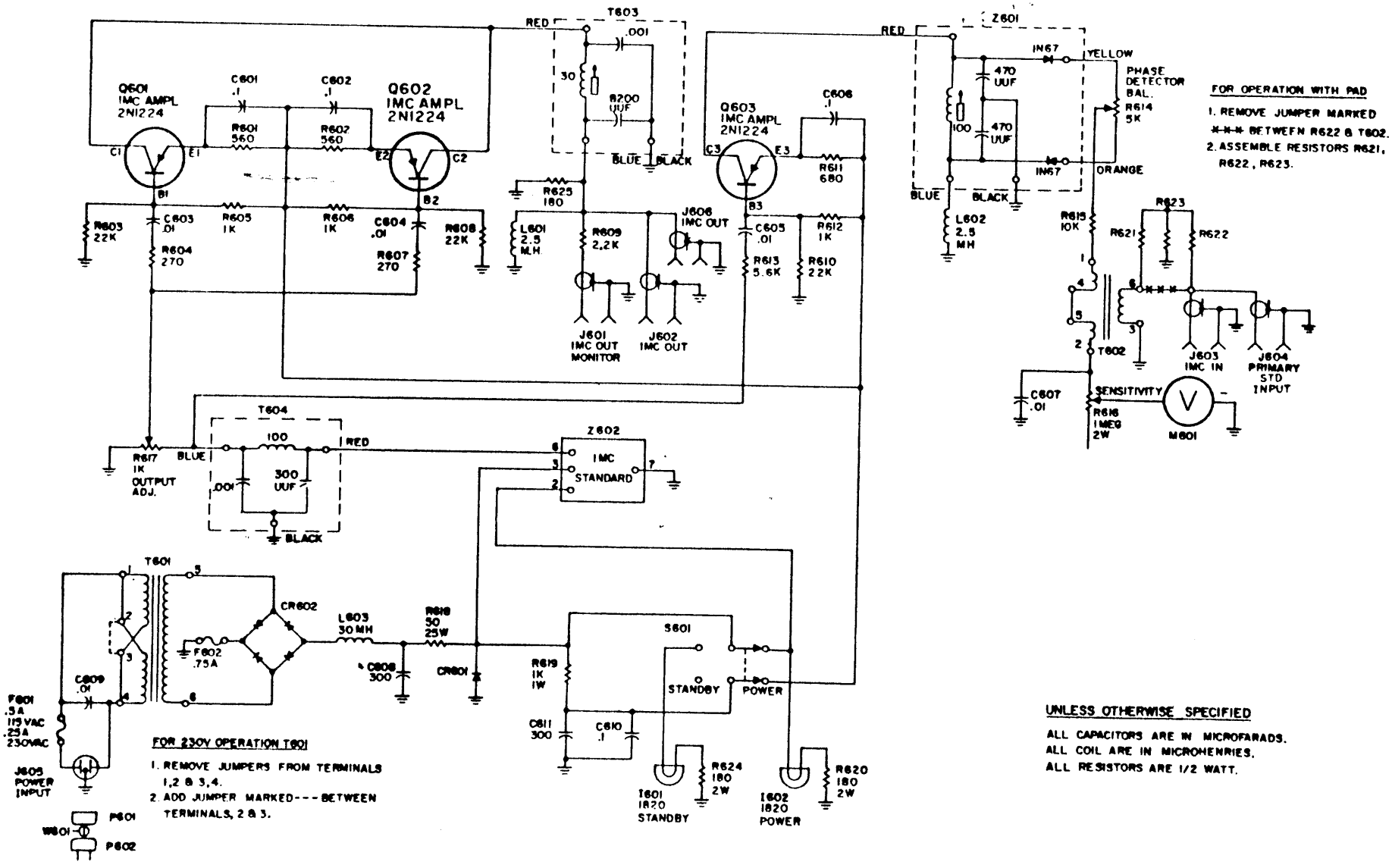


Figure III(C)-8-1. Primary Standard CSS-1, Schematic Diagram

SECTION 3

TITLE: Divider Chain Model CHL-1 (CV-928/URA-31)

OBJECTIVES:

a) to describe the functions of the Divider Chain in the Controlled Precision Oscillator system; to emphasize the importance of the unit and to show its dependence on Primary Standard Model CSS-1.

b) to discuss the circuitry of the divider chain, pointing up significant circuit parameters.

c) to demonstrate, with appropriate test equipment, the alignment of the unit.

REFERENCES:

a) Technical Manual for Divider Chain Model CHL-1.

b) TMC production specification # S-489.

c) Display Schematic TMC # CK-386-F.

Note:

Additional information on the Phantastron circuit may be obtained in the following commercial texts:

a) Radar Circuit Analysis; Air Force Publication 52-8.
b) Principles of Radar; MIT, 3rd edition.
c) Principles and Practice of Radar, by H. L. Penrose.

TRAINING AIDS:

a) CHL-1 unit, set up for operation with CSS-1 and CPP-2.

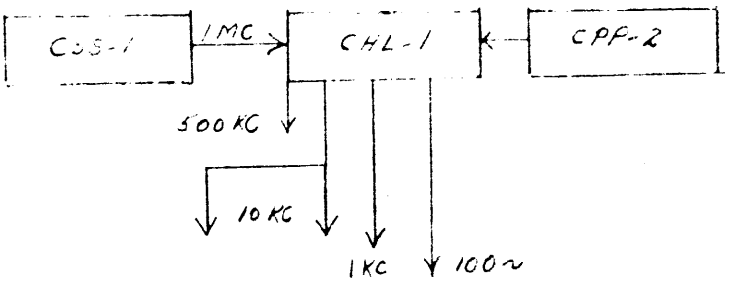
b) Oscilloscope.

c) VTVM.

d) Frequency Counter.

PRESENTATION:

A. Block Diagram:



1. Primary Standard Model CSS-1 supplies a 1 mc signal, accurate to 1 part in 100,000,000, at a nominal 1 volt level, into an output impedance of 70 ohms.

2. Power Supply Model CPP-2 supplies all voltages required.

3. Divider Chain CHL-1 delivers:

   a) outputs of 500 KC, 10 KC, 1 KC, and 100 cps to Controlled Oscillator Model CLL-1.

   b) a 10 KC output to Controlled Master Oscillator, Model CMO-1.

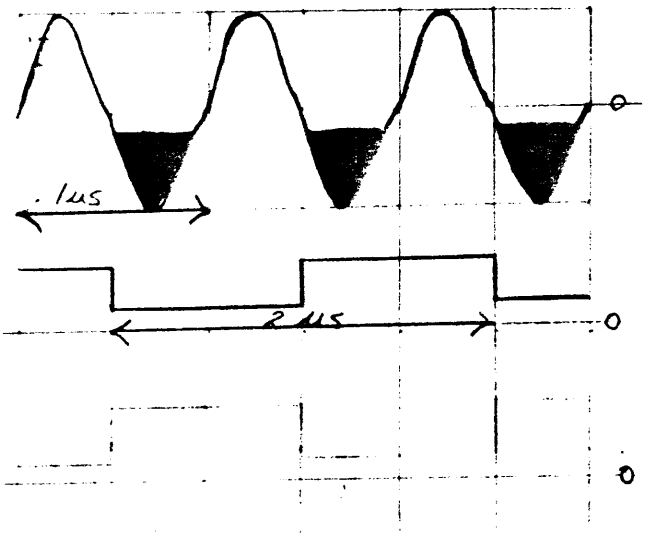
B. Circuit Description: (refer to schematic CK-386-F)

1. The 1 mc signal enters the divider from the standard at J-102, is coupled through transformer T-101, and is applied via diodes CR-101 and CR-102 to both control grids of Flip-Flop multivibrator V-102.

   The RF at the primary of T-101 is about 1 volt; at the secondary, about 18 volts.

2. With a positive 60 volts on the cathodes and a positive 55 volts on the grids, diodes CR-101 and CR-102 are back biased, with the anodes 11 volts negative with respect to the cathodes. Transformer T-101 steps up the input signal, but only the negative excursion of the input will initiate action of the circuit, due to the bias on the diodes.

3. Statically, one section of V-102 is conducting and the other is cut off. Assume that the left section is cut off; then eb left is high. The right section is conducting and eb right is low.
When the first negative excursion arrives, it will cut off the right section, which will cause the circuit to "flip"; the left section now conducts. This condition prevails until the next negative excursion of the input arrives, when the circuit "flops".
The period of the square wave at the output plate is 2 usec, corresponding to a frequency of 500 kcs.
A plot of input frequency and plate voltage is shown.



1 mc input signal
period: 1 usec

eb left section: (output)
period: 2 usec

eb right section:

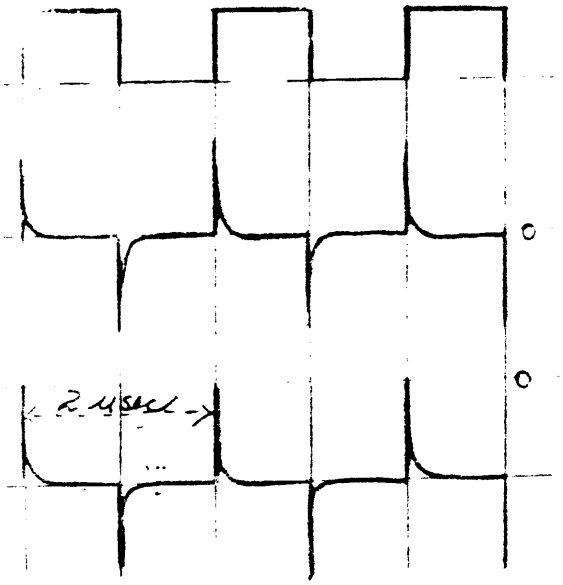
4. The output, at pin 6 of V102, is coupled to two circuits:

a) a 500 KC amplifier.
b) an isolation amplifier.

5. The 500 KC amplifier is conventional. In its plate circuit is a tank, peaked at 500 KCS. This output is sinusoidal, with a nominal value at output jack J-103 of 3.4 volts.

6. The isolation amplifier is actually a differentiator and negative clamping circuit. C-105 and R-109 form a differentiator circuit, since t, the period, is 2 usec, and T, the time constant, is RC or .1 usec.

7. Due to the clamping action of C-106, R-110 and V-103A, the signal at the grid of V-103A is clamped negatively from zero reference.



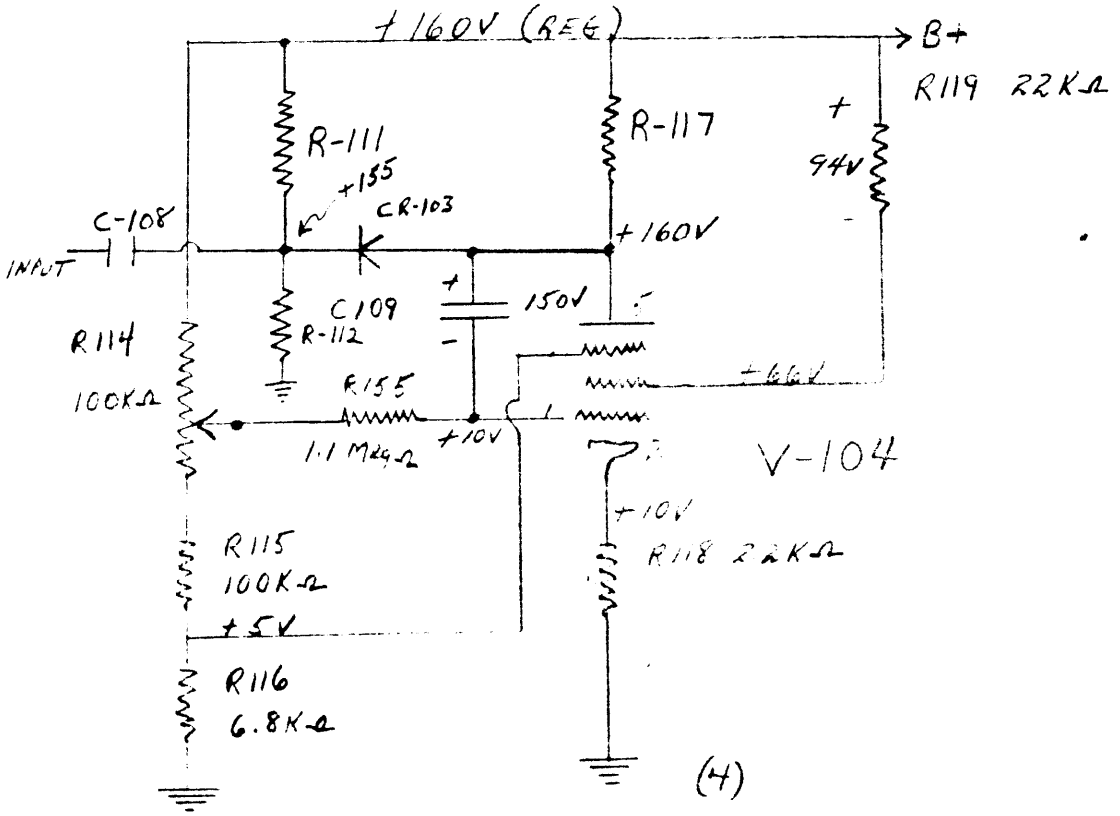
Plat voltage, V-102

Voltage across R-109

Voltage at grid, V-103A.

8. The signal at the plate of V-103A is essentially a train of negative spikes, spaced at 2 usec intervals. The positive spikes at the plate are reduced by clamping action and rendered ineffective by diode CR-103. Negative spikes, corresponding to a frequency of 500 KC, are passed by CR-103 to trigger V-104, the 100 KC Phantastron circuit. A brief description of this circuit follows.

9. Phantastron Circuit V-104: (static condition) Voltages are approximate only.



a) Statically, a voltage divider to B plus from the screen causes 4.27 ma. of screen current to flow. The screen then rests at 66 volts. The control grid, pin 1, is also connected to B plus through a voltage divider, but the large value of resistance in the grid circuit holds this current to a very small value. Total cathode current is 4.54 ma., and this current puts pin 2 at 10 volts. Note that this current is made up, for the most part, by the screen current. Voltage divider action at the suppressor places pin 7 at 5 volts. Since the cathode is at 10 volts, the suppressor is -5 volts with respect to the cathode. This is sufficient bias to cut off the plate, which rests at 160 volts.
Note that Ik - Isg is 370 ua. This represents the total control grid and suppressor current, a very small percentage of the cathode current.
Capacitor C-109 is charged to 150 volts, the difference between the plate and control grid voltage.

b) Negative triggers arrive at the plate of V-104 every 2 usec. These initiate the first phase of the phantastron division: a rapid, almost instantaneous change in circuit conditions.

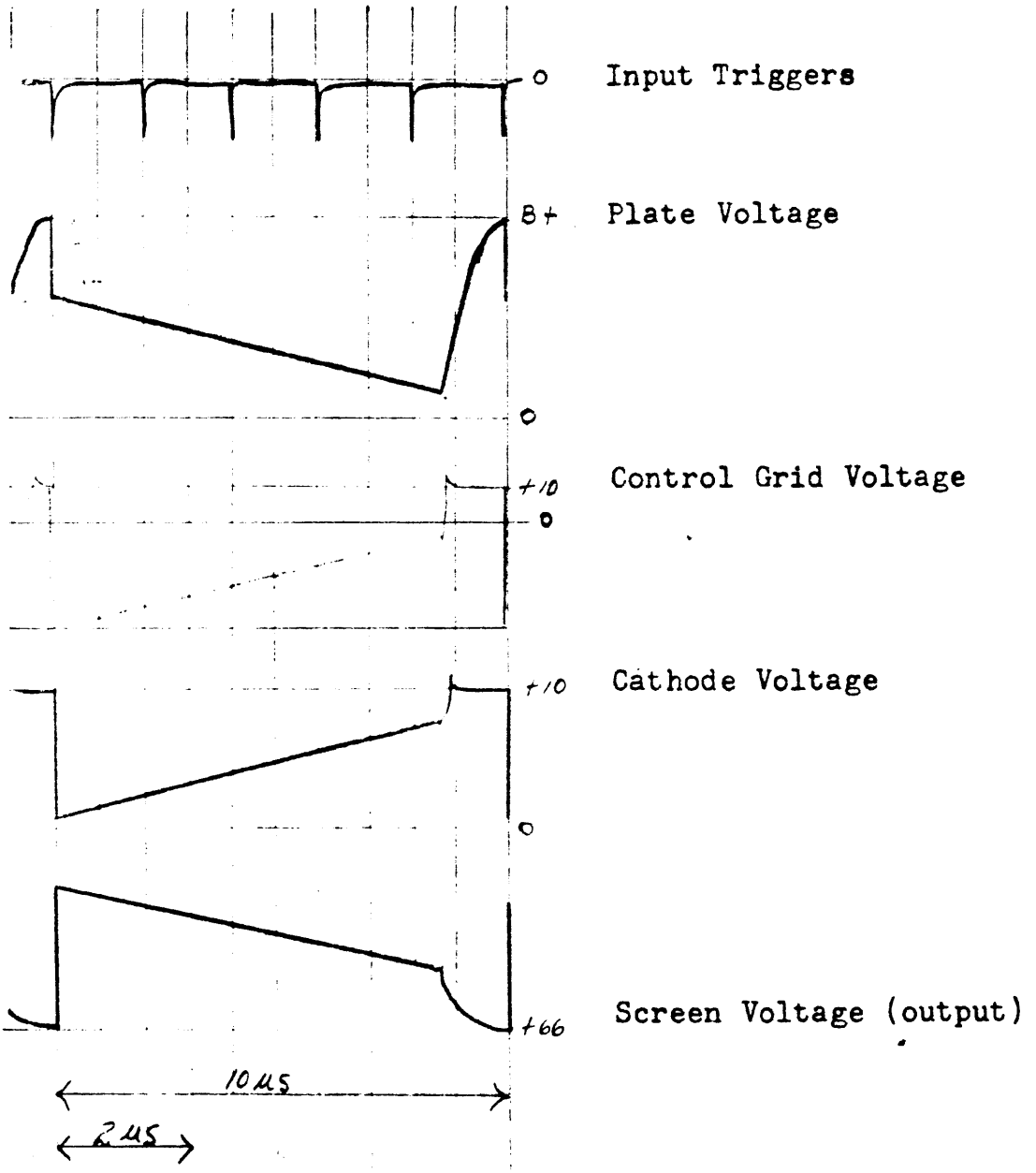
Note: the idealized waveforms on the following pages should be examined in conjunction with the explanation which follows.

c) When the first trigger arrives, the plate voltage drops; capacitor C-109 sees a change of charge, causing the control grid to go sharply negative. Control grid current ceases abruptly; the cathode follows the grid and drops to a very low value. The screen voltage rises sharply, because screen current is reduced to a very low value. The suppressor is no longer able to cut off the plate, and plate current flows. This ends the first phase of the phantastron cycle.

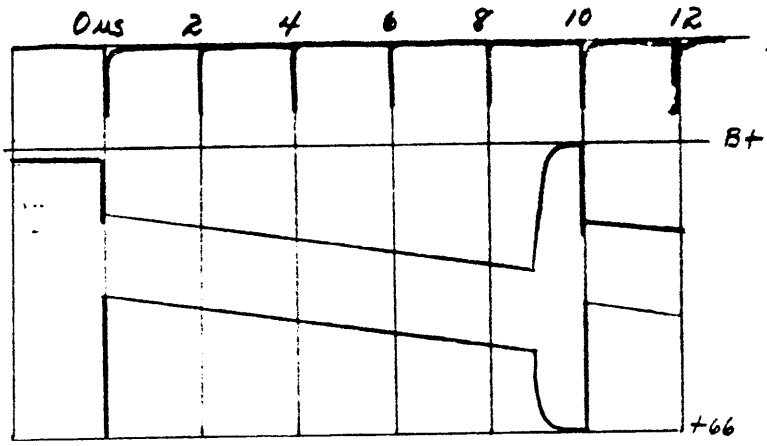
d) As C-109 discharges through R-155 and part of R-114, the grid voltage is allowed to rise, plate current increases, the plate voltage falls, and C-109 sees a new change of charge. This action continues throughout the second phase, resulting in a linear decrease of ep and esg, and a linear rise of ek and eg.

e) During the second phase, triggers following the initial trigger are blocked by diode CR-103, because the plate voltage is now lower, and the cathode of CR-103 is at substantially B plus.
The second phase ends when the plate is again cut off by rising cathode voltage. Capacitor C-109 quickly charges to B plus via the cathode and very low resistance between the conducting control grid and cathode
This recovery phase is rapid, but not so rapid as the first phase of the phantastron operation

Idealized Phantastron Waveforms



f) The time width of the second phase may be adjusted by R-114, the 100 KC adjust pot, in the grid circuit. This width may be set to coincide with the 4th (8us), 5th (10 us), or 6th (12 us), trigger.
For a frequency division of 100 KCS, R-114 must be adjusted so that the recovery is accomplished just prior to the arrival of the 5th trigger.

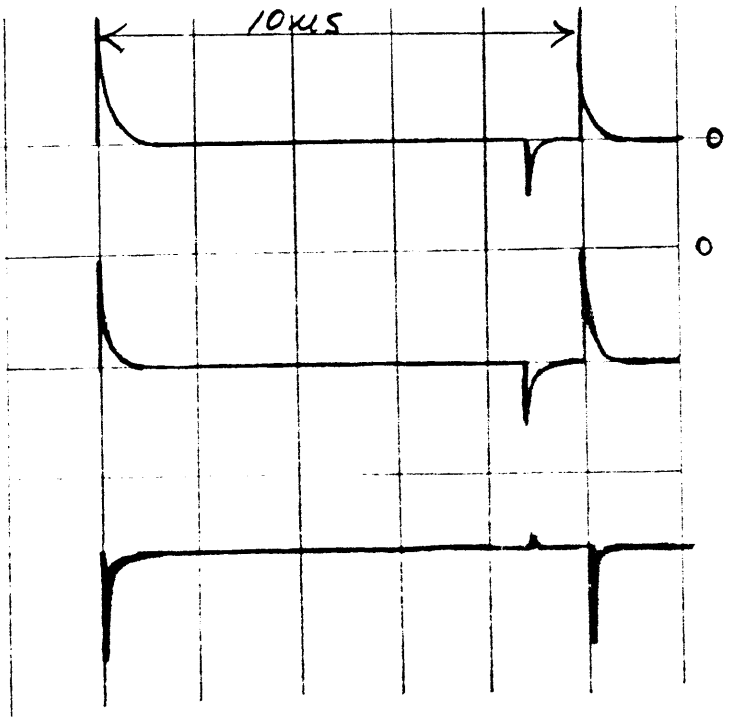


triggers to phantastron

plate waveform

screen waveform

10. The output, taken from the screen, is differentiated by C-110 and R-120. C-111, R-121 and V 103B form a negative clamping circuit. Thus, at the plate of v-103B appear negative triggers, 10 usec apart.
A 100 KC test point is taken from the cathode circuit of V-103B.



differentiated output at R-120

clamped waveform at grid of V-103B

output triggers at plate of V-103B

11. The triggers from the plate of V-103B are used to divide the 100 KC down to 10 KC by means of another phantastron circuit, V-105.
The remainder of the CHL-1 circuitry is similar to the preceding, except for circuit values. Three 10: 1 dividers count down the frequency to 10 KC, 1 KC and 100 cycles. All outputs are taken from BNC jacks at the rear of the chassis.

12. The following adjustments are located on the top of the chassis:

a) 100 KC adjust: R-114

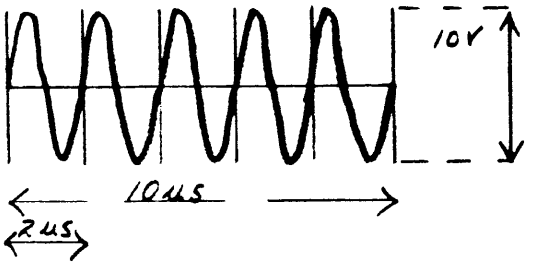
b) 10 KC adjust: R-124

c) 1 KC adjust: R-135

d) 100 cycle adjust: R-147

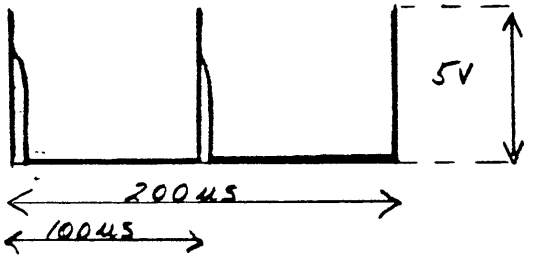
On the following page is a chart showing oscilloscope waveforms taken with a Tektronics Model 545. In addition, RMS vacuum tube voltmeter readings are given.

Oscilloscope waveforms at output jacks: CHL-1



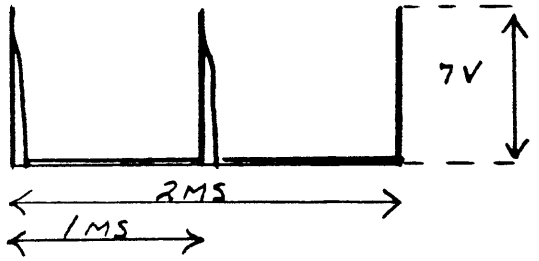
J103 500KC OUTPUT
1μS / CM

VTVM: 3.4V AC



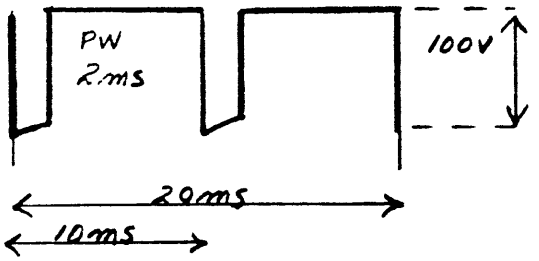
J104 10KC OUTPUT
20μs / CM

VTVM: 3.3V AC



J105 1KC OUTPUT
.2ms /CM

VTVM: 4.0V AC



J106 100V OUTPUT
2MS / CM

VTVM 18V AC

C. Alignment of Model CHL-1 Frequency Divider

1. Equipment required:

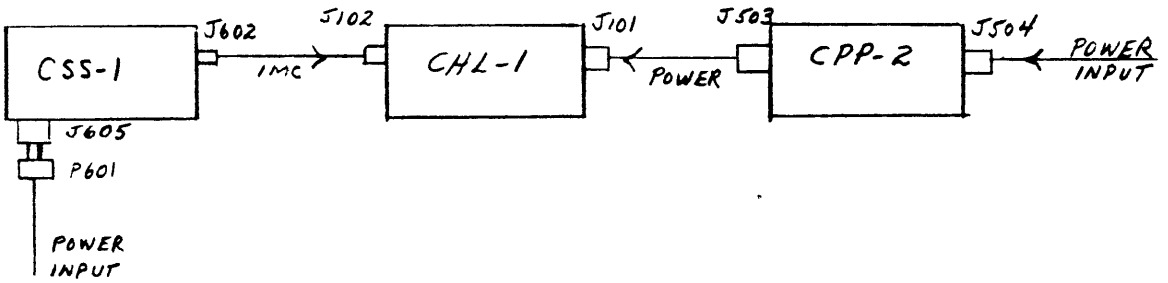
   a) CHL-1 unit, set up for operation with CSS-1 unit and CPP-2 power supply unit.

   b) Frequency Counter. (Hewlett Packard 524C)

   c) Vacuum Tube Voltmeter. (H.P. 410B)

   Note: an oscilloscope is not required for alignment, but will be found useful for examination of waveforms.

2. Set up the equipment as shown in the sketch below.



3. Measure the 1 mc voltage at the primary of T-101; it should be 1 V RMS. If necessary, adjust R-617, the output adjust pot on the CSS-1.

4. Connect the VTVM to the 500 KC test jack. Tune L-102 for maximum output. The voltage should be approximately 3.4 V RMS. Connect the counter to the 500 KC test jack. It should read 500 KCS.

5. Connect the counter to the 100 KC test jack. Adjust R-114 until the counter reads 100 KCS. Leave R-114 in the center of the range over which 100 KCS is obtained.

6. Connect the counter to the 10 KCS test jack. Adjust R-124 until the counter reads 10 KCS. R-124 should be left in the center of the range over which 10 KCS is obtained. When the VTVM is connected to the 10 KC test jack, it should read approximately 3.3 V RMS.

7. Connect the frequency counter to the 1 KC test jack. Adjust R-135 to the center of the range which gives a reading of 1 KC. When connected here, the VTVM should read approximately 4.0 V. RMS

8. Connect the counter to the 100 cps test jack Adjust R-147 to the center of the range which gives a

reading of 100 cps on the counter. The VTVM connected here should read approximately 18.0 V RMS.

9. Lock all controls. This completes the alignment of the CHL-1 unit.

SUMMARY:

1. With schematic CK-386-F, review the circuitry and important points. (fig. III(D)-8-1 of tech. manual)
2. Emphasize that the 1 mc signal feeding the unit must be accurate and stable.
3. Note that any malfunction in any divider will affect all subsequent circuits.

Model CHL-1 Voltage Chart

A. Chart #1: DC Voltages, 1 mc input disconnected

	1	2	3	4	5	6	7	8	9
V-101	0	0	105	FIL	FIL	120	1.85	—	—
V-102	120	60	68	FIL	FIL	120	60	68	FIL
V-103	160	-5.2	0	FIL	FIL	145	0	28	FIL
V-104	11	11	FIL	FIL	160	58	5.4	—	—
V-105	16	16	FIL	FIL	160	65	5.4	—	—
V-106	150	0	2.8	FIL	FIL	155	0	3	FIL
V-107	20	20	FIL	FIL	160	76	5.4	—	—
V-108	16	16	FIL	FIL	160	76	5.3	—	—

B. Chart #2: DC Voltages, 1 mc input connected

	1	2	3	4	5	6	7	8	9
V-101	0	-1.3	82	FIL	FIL	130	1.3	—	—
V-102	135	56	62	FIL	FIL	130	56	62	FIL
V-103	120	-3	0	FIL	FIL	150	-9.2	.9	FIL
V-104	5.4	7.7	0	FIL	120	110	5.2	—	—
V-105	5	8.4	FIL	FIL	105	120	5.1	—	—
V-106	159	-40	.22	FIL	FIL	155	-16	.55	FIL
V-107	5.8	9.4	FIL	FIL	110	125	5	—	—
V-108	1.5	6.3	FIL	FIL	88	130	5.2	—	—

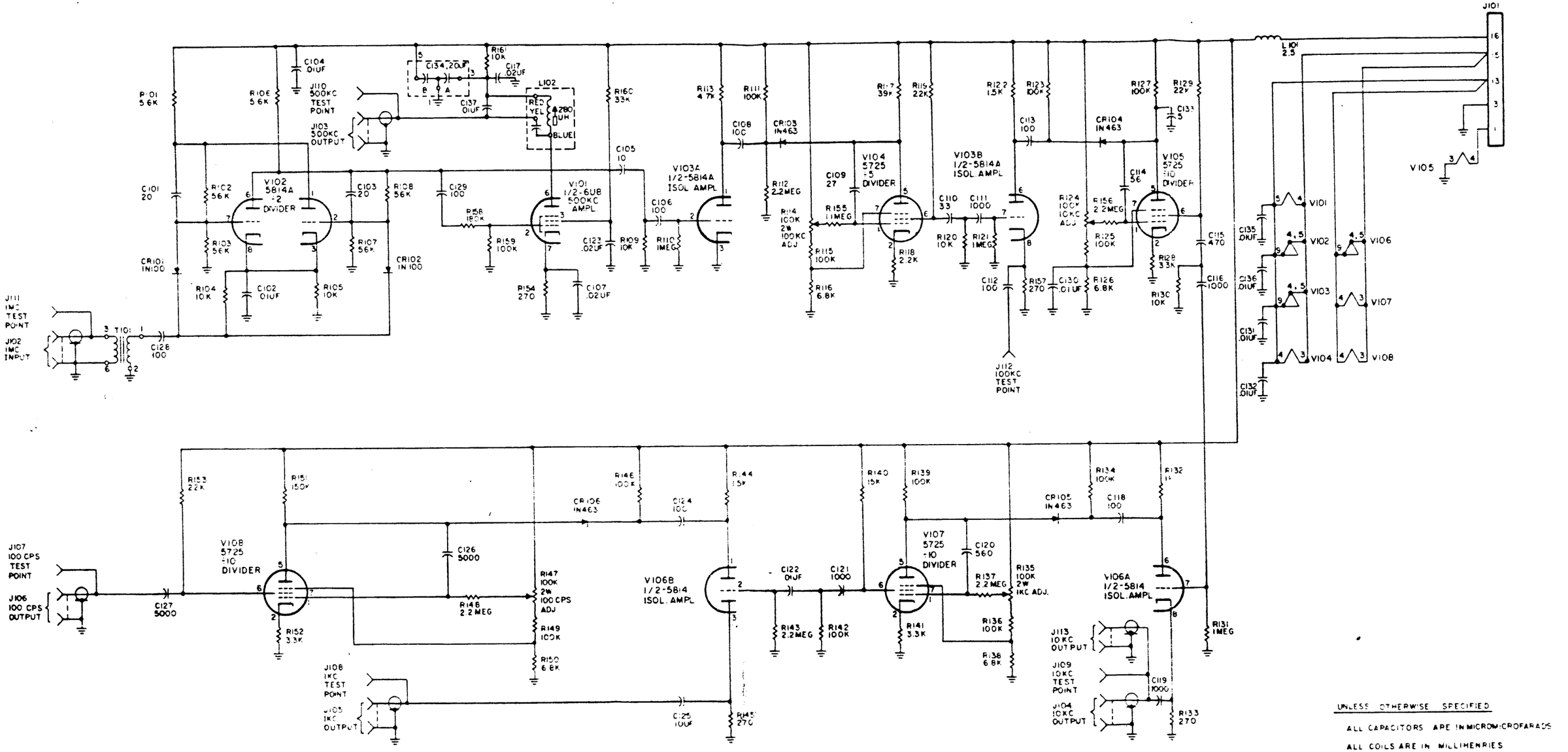
C. Chart #3: AC Voltages

	1	2	3	4	5	6	7	8	9
V-101	0	1.5	0	FIL	FIL	100	0	—	—
V-102	10	5	0	FIL	FIL	10	5.5	0	FIL
V-103	22	2	0	FIL	FIL	4	10	2.7	FIL
V-104	10	8.2	FIL	FIL	21	22	.7	—	—
V-105	18	15	FIL	FIL	36	20	0	—	—
V-106	1.4	34	4.6	FIL	FIL	1.6	16	3.6	FIL
V-107	14	11	FIL	FIL	26	21	.2	—	—
V-108	13	9.5	FIL	FIL	44	19	.2	—	—

Model CHL-1 Resistance Chart

Unit completely disconnected. All readings to ground.

	1	2	3	4	5	6	7	8	9
V-101	—	110K	55K	INF	INF	35K	250	—	—
V-102	30K	37K	8K	INF	INF	30K	37K	8K	INF
V-103	35K	1M	0	INF	INF	30K	1M	240	INF
V-104	1M	2.2K	INF	INF	61K	45K	7K	—	—
V-105	2.2M	35K	0	F,L	110K	50K	65K	—	—
V-106	30K	2M	250	INF	INF	26K	1M	220	INF
V-107	2M	3.5K	INF	INF	110K	40K	6.5K	—	—
V-108	2.1M	3.5K	INF	INF	110K	50K	6.9K	—	—
...									



UNLESS OTHERWISE SPECIFIED

ALL CAPACITORS ARE IN MICROMICROFARADS

ALL COILS ARE IN MILLIHENRIES

ALL RESISTORS ARE 1/2 WATT.

Figure III(D)-8-1. Divider Chain CHL-1, Schematic Diagram

SECTION 4

TITLE: Controlled Oscillator Model CLL-1 (O-717/URA-31)

OBJECTIVES:

a) to explain the function of the Model CLL-1 controlled oscillator in the Controlled Precision Oscillator system.

b) to discuss the circuitry of the Model CLL-1, pointing up significant circuit parameters.

c) to demonstrate, with appropriate test equipment, the alignment of the unit.

REFERENCES:

a) Technical Manual for CLL-1 (O-717/URA-31)

b) TMC Production Specification #S-491.

c) Schematic of CLL-1 #CK-446.

TRAINING AIDS:

a) Model CLL-1 unit, set up for operation with CSS-1, CHL-1, and CPP-2 units.

b) Oscilloscope: Tektronics Model 545, or equivalent.

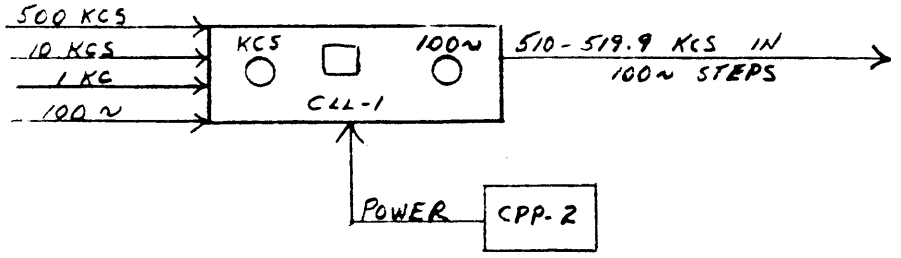
c) VTVM: H.P. Model 410B, or equivalent.

d) Frequency Counter: H.P. 524C.

PRESENTATION:

A. General Discussion:

1. Block Diagram:



2. Controlled Oscillator Model CLL-1 receives inputs at 500 KCS, 10 KCS, 1 KC, and 100 CPS from the Model CHL-1 frequency divider. The Output of the CLL-1 is a frequency in the range 510.0 - 519.9 KCS, in 100 cycle steps, depending on the settings of the KILOCYCLES and HUNDREDS front panel controls.

3. The operation of the unit depends on three synthesizer loops, each of which will be discussed in detail.

4. A monitor oscilloscope on the front panel provides a rapid check on the operation of each loop.

5. Power is furnished by the CPP-2 unit.

6. The 510.0 - 519.9 KCS output is used to synthesize the frequency of Controlled Master Oscillator Model CMO in the range of 2 to 4 MCS, in 100 cycle steps.

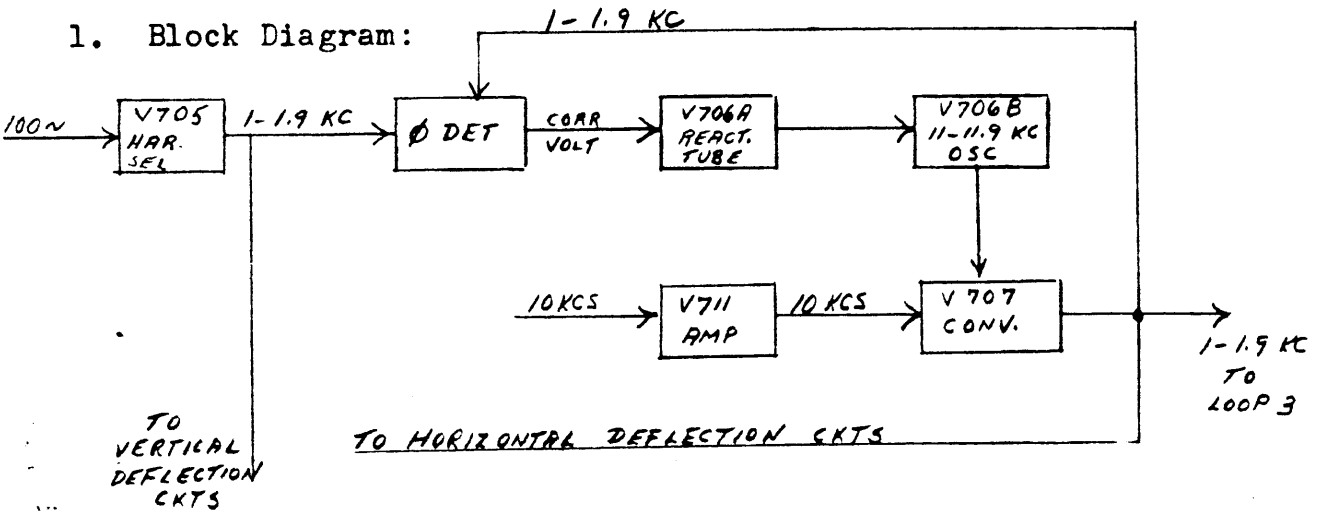
7. On the CLL-1, the KILOCYCLES and HUNDREDS knobs are set to correspond with the THOUSANDS and HUNDREDS digits of the CMO output frequency. The process is repeated for every 10 KC increment of CMO frequency.

EXAMPLES:

CMO OUTPUT	CLL KC DIAL	CLL HUNDREDS DIAL	CLL OUTPUT
2,000,000	0	0	510,000
2,525,500	5	5	515,500
3,248,900	8	9	518,900
3,258,900	8	9	518,900
3,344,200	4	2	514,200

B. Operation of Loop #1:

1. Block Diagram:



2. The input to harmonic selector V-705 is 100 CPS. Harmonic selector V-705 selects the 10th to the 19th harmonic of 100 CPS, depending on the position of S-702, the HUNDREDS switch. This represents frequencies in the range 1 KC to 1.9 KCS, which are passed to a phase detector circuit.

3. The 10 KCS input is amplified by V-711, and sent to converter stage V-707. The second input to converter stage V-707 is the output of an internal 11 to 11.9 KCS oscillator, V-706B, the exact output of which is determined by S-702, the HUNDREDS switch.

4. The output of converter V-707 is a difference frequency in the range of 1 to 1.9 KCS. This is the second input to the phase detector circuit. The output of the phase detector is a correction voltage, whose characteristics depend on the phase difference between the two applied 1-1.9 KC inputs.

5. The correction voltage is applied to reactance tube V-706A, which is designed to "pull in" the frequency of internal oscillator V-706B.

6. The output of loop #1 is a frequency in the range of 1 to 1.9 KCS, phase locked by the accurate 100 CPS and 10 KCS inputs. This output is sent to loop #3, and, via selector switches, to the horizontal deflection circuits of the monitor oscilloscope. The vertical deflection circuits of the monitor scope are fed by harmonic selector V-705. Thus, with the loop synthesized, a rectangle will be observed on the monitor scope in each position of S-702, the HUNDREDS switch.

Detailed Discussion of Loop #1:

Refer to F[illegible]e III (E)-4-1: Loop 1, CLL-1 Tech Manual

1. The 100 CPS input from the CHL-1 enters at J-704 and is presented to V-705, the harmonic selector, which is initially unbiased. The stage will develop grid leak bias due to clamping action and the output will be rich in harmonics.
   HUNDREDS switch section S-702A selects the proper capacity to resonate at the desired harmonic with L-710, a 60 mh choke.
   The output, designated as the " 1 - 1.9 KC standard", is delivered to the phase detector at the wiper on R-755, the balance adjust potentiometer, and to the vertical deflection circuits of the monitor scope.

2. The 10 KCS input from the CHL-1 enters at J-705 and is amplified in V-711. The 10 KCS output of V-711 is delivered to Grid 3, pin #7 of converter V-707.

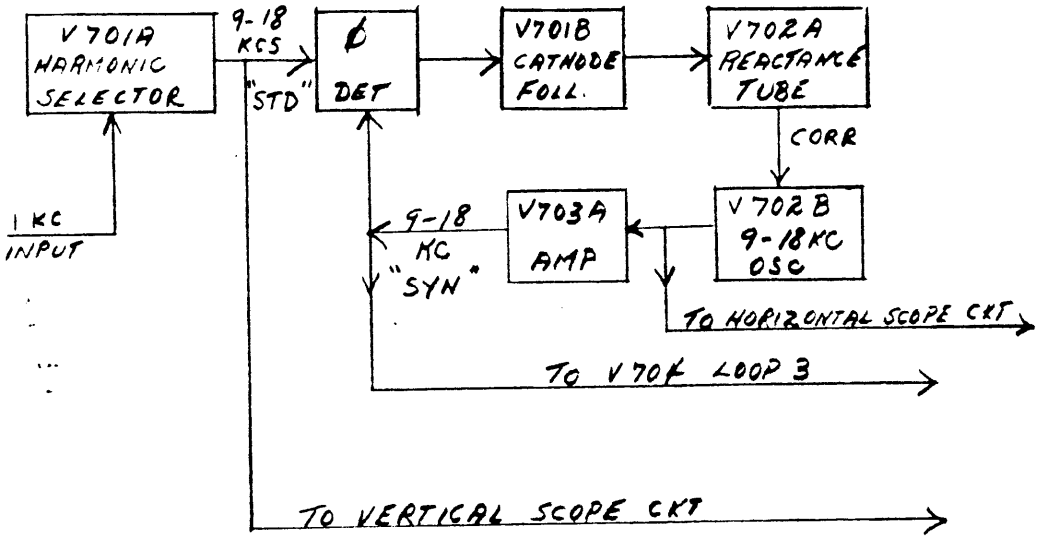
3. The second input to converter stage V-707 arrives at grid 1, pin #2 from V-706B, the internal 11-11.9 KCS oscillator, whose frequency determining characteristics depend on the setting of switch S-702B.

4. The output of converter V-707 is a difference frequency in the range 1 to 1.9 KCS. This is the second input to the phase detector, applied at T-703. Note that the components and switching arrangements in the plate circuit of converter V-707 are identical with those in the plate section of V-705. This second 1 - 1.9 KCS signal is designated as the "synthesized" 1 - 1.9 KC signal and it is applied not only to the phase detector, but to the horizontal deflection circuits of the monitor scope, and to loop #3.

5. The correction voltage developed by the phase detector is taken from the wiper of R-755, and passed through low pass filter R-748, C-793 thence to the grid of reactance tube V-706A. The reactance tube shunts the internal oscillator V-706B with the proper reactance to correct its frequency.

D. Operation of Loop #2:

1. Block Diagram:



2. The 1 KC input from frequency divider CHL-1 is applied to harmonic selector V-701A. This stage selects the 9th through the 18th harmonic of 1 KC, depending on the setting of S-701A, the KILOCYCLES switch. The output, 9 to 18 KCS, is applied to a phase detector circuit, and, via the monitor scope selector switch, to the vertical deflection circuits of the monitor.

3. V-702B is an internal oscillator, whose output frequency is 9 to 18 KCS, in ten steps, depending on the setting of KILOCYCLES switch S-701B. The output of this oscillator supplies input to amplifier V-703A, and is also sent to the horizontal deflection circuits of the monitor scope.

4. The amplified 9 to 18 KC output of V-703A is applied to the phase detector circuit and to the circuitry of loop #3.

5. The phase detector compares the phase of the two 9-18 KC inputs and develops a correction voltage which reacts on internal oscillator V-702B via cathode follower V-701B and reactance tube V-702A.

6. The output of loop #2, then, is a 9 to 18 KC signal phase locked to the accurate 1 KC input from the frequency divider model CHL-1.

7. When the monitor scope switch is thrown to "L-2", a rectangle will appear if the "standard" and "synthesized" 9 to 18 KC signals are locked in.

E. Detailed Discussion of Loop #2:

Refer to Figure III (E)-4-2 Loop #2, CLL-1 Tech Manual

1. The 1 KC input arrives at J-701 and drives unbiased stage V-701A to produce an output rich in harmonics. S-701A, part of the KILOCYCLES switch, shunts L-701 with the proper capacity to resonate at the 9th through 18th harmonics of the input. A portion of this output is tapped off L-701 and sent to the vertical deflection circuits of the monitor scope. Another output is coupled through C-711 and delivered to the phase detector at the balance pot wiper, R-712.

2. V-702B is an internal oscillator, the output frequency of which is determined principally by L-702 and capacitors switched in by S-701B, part of the KILOCYCLES switch. Trimmers C-719, C-721, C-723, C-725, C-727, C-729, C-731, C-733, C-735 and C-739 adjust the frequency on each position of S-701B during alignment.

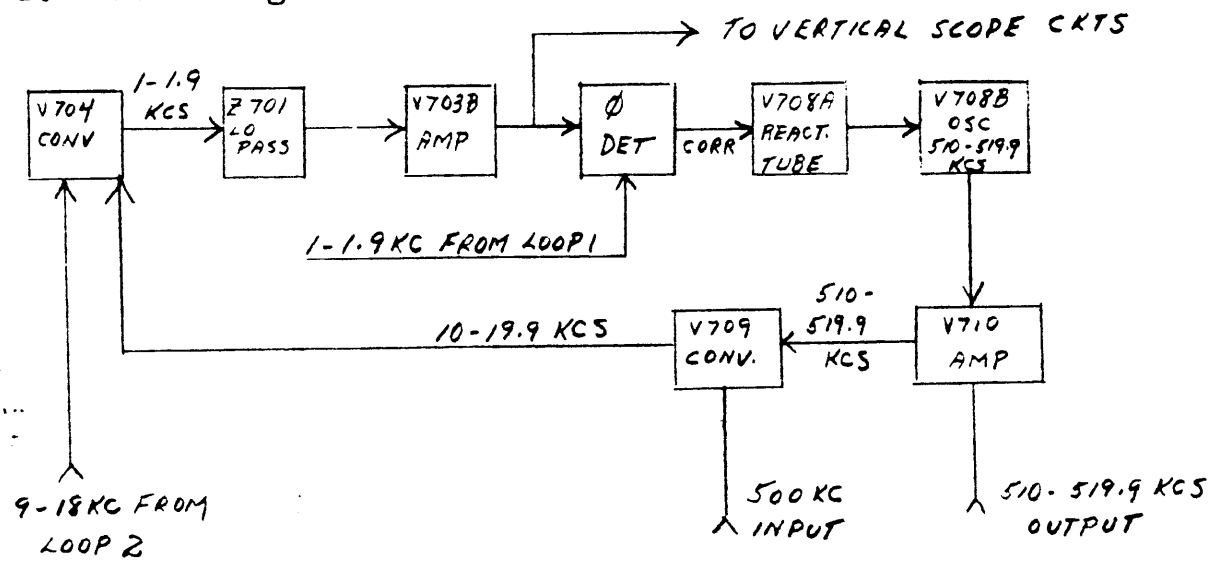
3. The 9 to 18 KC oscillator output, taken from the cathode of V-702B, is applied to amplifier V-703A, and to the horizontal deflection circuits of the monitor scope.

4. The output of amplifier V-703A is the second input to the phase detector circuit, applied at T-704. At this point the output to loop #3 is also taken.

5. The correction voltage developed by the phase detector at the wiper arm of R-712 is sent to cathode follower stage V-701B. The output of the cathode follower feeds reactance tube V-702A, which "pulls in" the internal oscillator V-702B to the correct frequency.

F. Operation of Loop #3:

1. Block Diagram:



2. V-708B is an internal oscillator with an output frequency of 510 - 519.9 KCS in ten steps, as selected by the KILOCYCLES switch, S-701D, and HUNDREDS switch, S-702D. The output is amplified by V-710 and applied:

   a) to the output jack J-703.

   b) to converter stage V-709.

3. The second input to converter stage V-709 is 500 KCS, supplied by frequency divider model CHL-1. The difference frequency output is in the range 10 - 19.9 KCS, and this signal is applied to another converter stage, V-704. The second input to converter stage V-704 is the 9 to 18 KC signal from loop #2.

4. The output of converter stage V-704 is a difference frequency, in the range 1 to 1.9 KCS. This is sent to a phase detector circuit via a low pass filter and amplifier stage V-703B. The low pass filter has a cut off frequency of 2 KCS.

5. The phase of the two 1 - 1.9 KC inputs applied to the phase detector is compared and a correction voltage is developed and sent to reactance tube V-708A, which keeps the 510 - 519.9 KC oscillator "locked in"

Detailed Discussion of Loop #3:

Refer to Figure III (E)-4-3 Loop #3, CLL-1 Tech Manual

1. V-708B, an internal 510 - 519.9 KCS oscillator, has as its primary frequency determining components L-707, L-708, C-763, and C-765.
With S-701D is position 9, and S-702D in position 9, L-708 is adjusted for an output frequency of 519.9 KC, plus or minus 5 KCS. Then L-707 is adjusted for an output frequency of 519.9 KCS, plus or minus 10 CPS. Trimmers C-772 Through C-780 are adjusted for the proper frequencies on the other switch positions, i.e., 518,900 CPS, 517,900 CPS, 516,900, etc. Then S-701D is placed in position 5, which represents a frequency of 515,900 CPS; trimmers C-782 through C-790 are adjusted for each position of S-702D for output frequencies of 515,800, 515,700, 515,600, etc.

2. The output, taken from pin 8 of V-708B, is applied to amplifier V-710.
R.F. transformer T-702 is peaked for maximum output at output jack J-703.
At the "yellow" dot on T-702, the output is sampled and applied to the control grid of converter stage V-709.

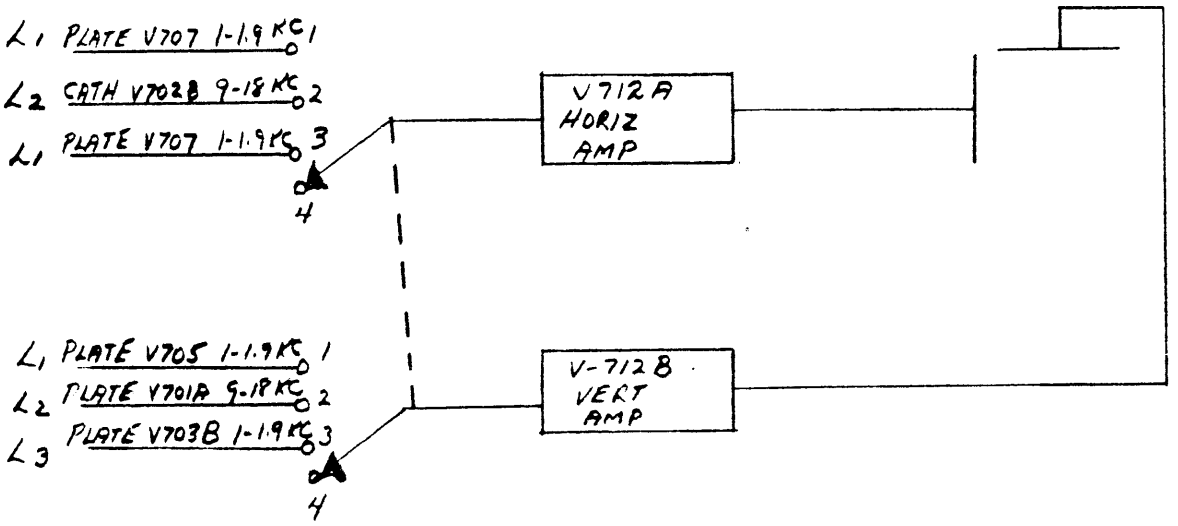
3. The second input to converter V-709 is 500 KCS, from J-702. The plate circuit of V-709 is resonant to the appropriate difference frequency, by means of L-706 and capacity inserted by S-701C. The difference frequency is in the range 10 - 19.9 KCS. This is applied to grid 3, pin #7, of converter V-704.

4. The second input to converter V-704 is the 9 - 18 KC signal from loop #2, applied to control grid pin #2. The difference frequency is in the range 1 - 1.9 KC, and it is applied to terminal #1 of Z-701, a low pass filter with a cutoff frequency of 2 KCS.
The output of Z-701, pin #2, is applied to amplifier V-703B, the output of which is applied to the phase detector at T-704.
In addition, the output of V-703B is applied, via R-768, to the vertical deflection circuits of the monitor scope.

5. The second input to the phase detector, 1 - 1.9 KCS from loop #1, is applied at the wiper of R-763. The correction voltage, developed at this point, is applied to reactance tube V-708A, which corrects the frequency of the 510 - 519.9 KCS internal oscillator, V-708B.

6. The horizontal deflection circuits for loop #3 are fed from the plate of V-707, the 1 - 1.9 KC converter in loop #1. Thus, for a rectangular pattern in loop #3 position, loops #1 and #3 must be operating properly.

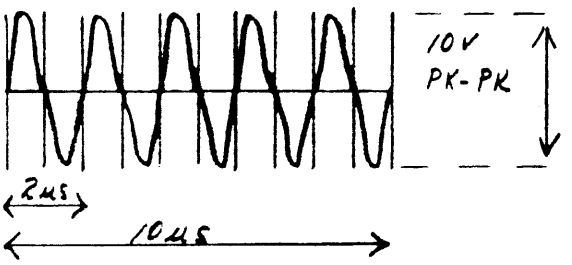
H. Monitor Scope Circuits: Block Diagram:



I. Alignment of Controlled Oscillator Model CLL-1:

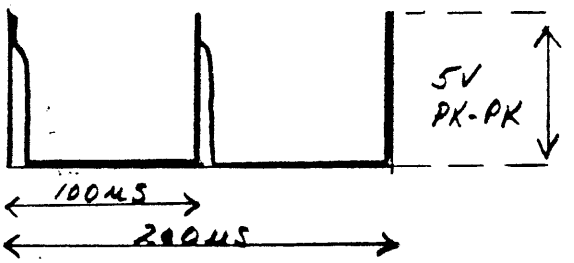
Refer to Test Procedure Section of SBG-2 Technical Manual page III-6-19.

I. Significant Waveforms to be observed:



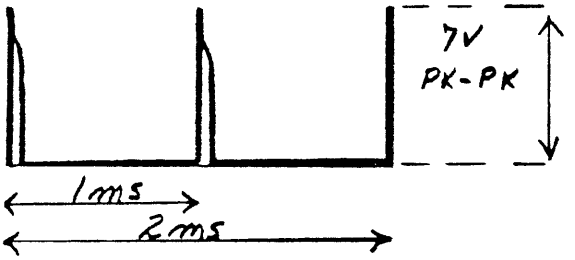
J-702 : 500 KC INPUT
1μs / CM

VTVM : 3.4 V AC



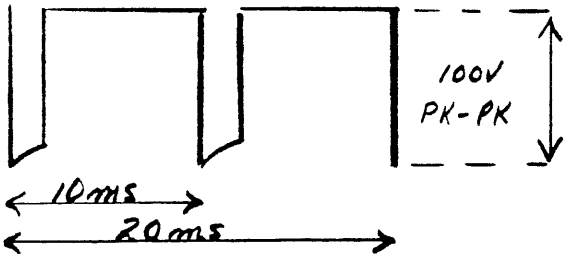
J-705: 10KC INPUT
20μs / CM

VTVM : 3.9 V AC



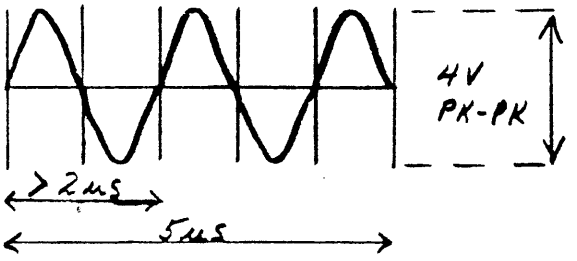
J-701 1KC INPUT
.2 ms / CM

VTVM : 4.0V AC



J-704 : 100~ INPUT
2 MS / CM

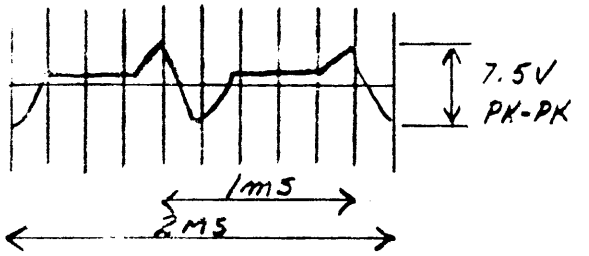
VTVM : 18 V AC



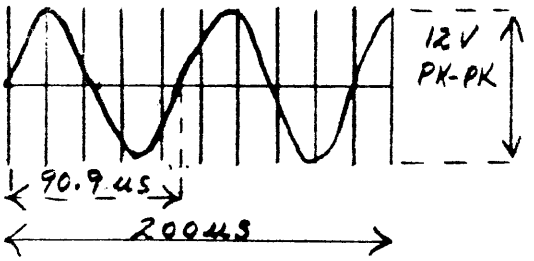
J-703 : 510 - 519.9 KC OUTPUT
.5ms / CM

VTVM : 1.4V AC

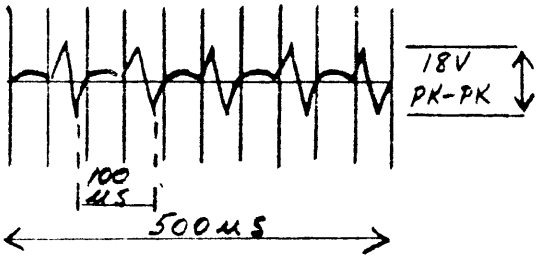
KC, HUNDREDS KNOBS AT 0, 0.
WAVEFORM SHIFTS SLIGHTLY
AS KNOBS ARE MOVED.



TP-5 J-711
.2 MS/CM
HUNDREDS SWITCH AT "0"
f = 1KC
WAVEFORM SHIFTS AS HUNDREDS KNOB MOVED.



TP-8 J-714
20us/CM
HUNDREDS SWITCH AT "0"
WAVEFORM SHIFTS AS HUNDREDS KNOBS MOVED.

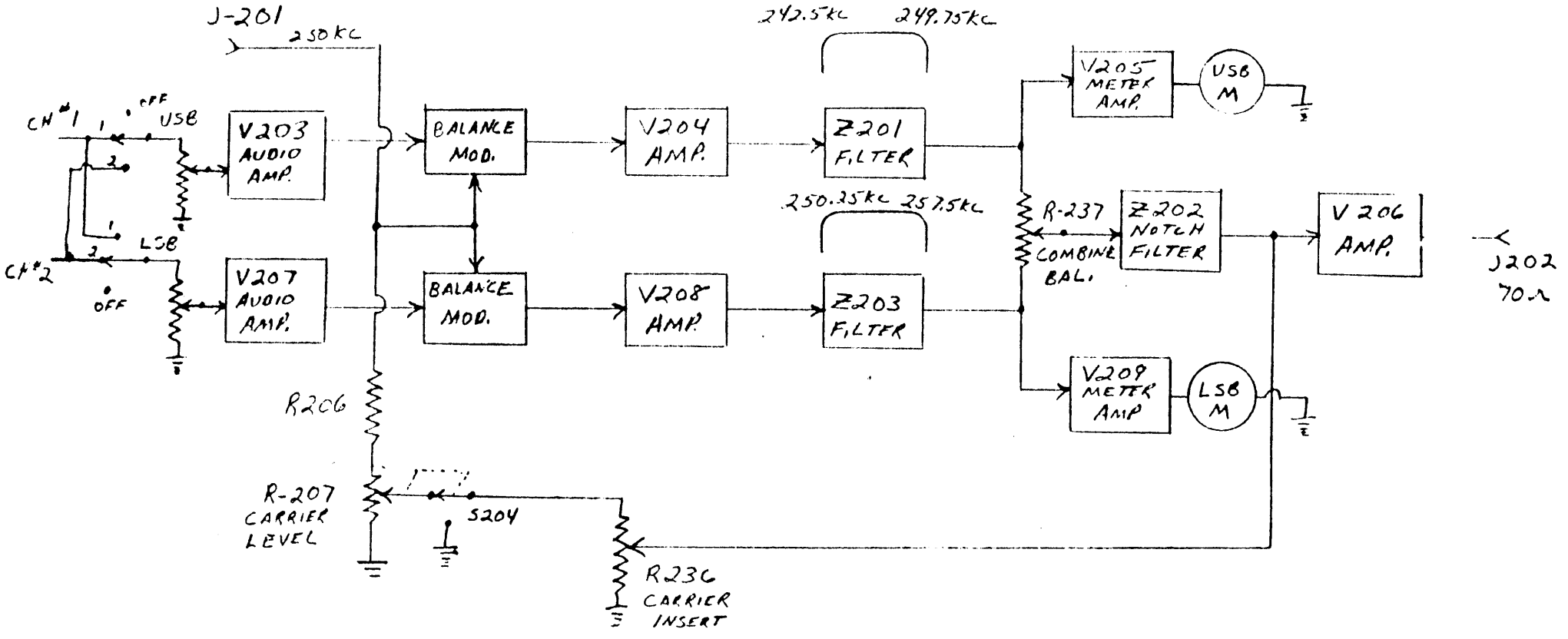


TP-1 J-707
50us/CM
KILOCYCLES SWITCH AT 1 (10KC)

WAVEFORM SHIFTS AS KC KNOB MOVED

SECTION 5

SECTION 6

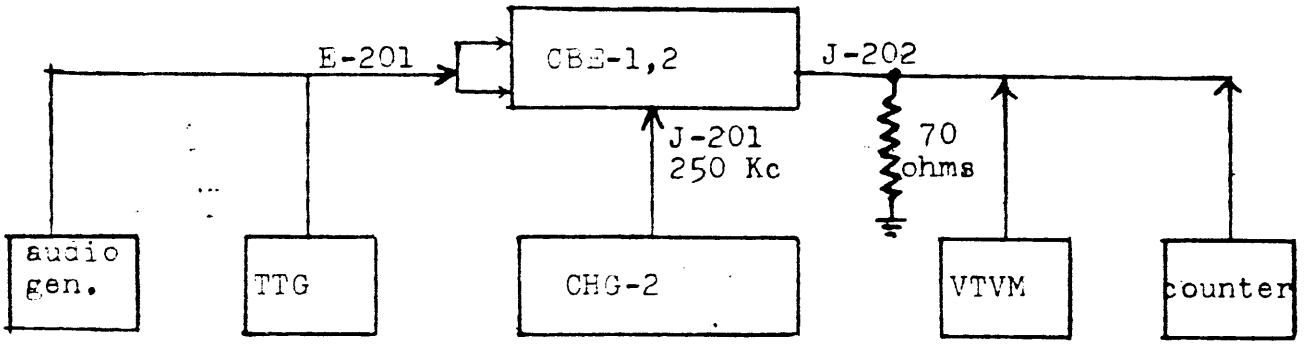


CBE-1, 2
BLOCK DIAGRAM
Vail Shaw

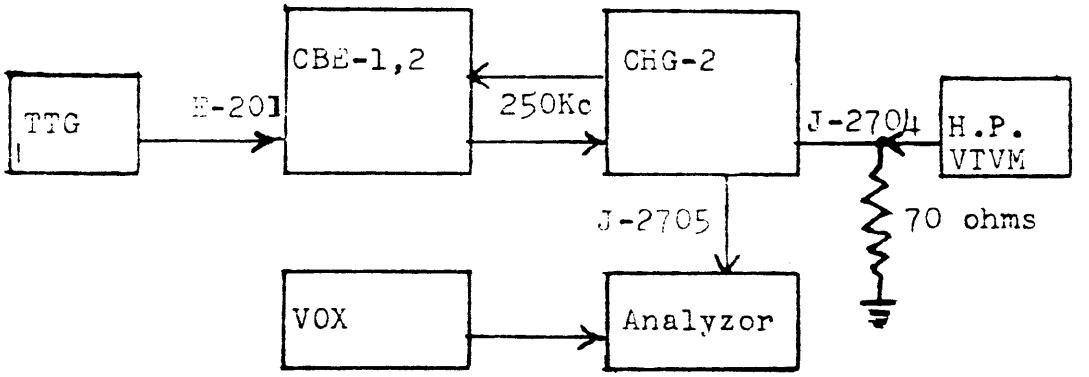
III-6-9 Test Procedure for Sideband Exciter Model CBE-1 or CBE-2 as used with the SBG sideband generator.

Figure III-6-5

Alignment test setup for sections 1 and 2.



Distortion Test setup for section 3.



Note: The CBE-1 and the CBE-2 differ in one respect, the USB and LSB filter for the CBE-1 has a bandwidth of 7.5 Kc and the CBE-2 a 3.5 Kc bandwidth.

Revised: 4/66

Paul E. Grove

CBE-1,2 Alignment Procedure as used with CHG-1.

Test Equipment Required

1. Frequency Counter: H.P. 524c, or equivalent.
2. A.C. VTVM (Ballantine Model 314 or equivalent).
3. 70 Ohm Non-Inductive Resistance.
4. Panalyzer Model SB-12 A.
5. Variable Frequency Oscillator: Model VOX.
6. Audio Generator: H.P. Model 200cb.
7. Two Tone Generator.
8. AC VTVM (H.P. Model 410c).

Preliminary

(a) Remove Unit from the frame using the top of the CHG-1 as support.
(b) Connect the 70 ohm non-inductive resistor to J-202.
(c) Turn USB and LSB selector switches to OFF.
(d) Turn carrier level control OFF (Max. CCW).
(e) Connect and turn AC power ON.
(f) Connect 250 Kc from CHG-1 to J-201. Insure that it is 1 to 1.5 Vrms. (2.8 to 4.2V Peak to Peak)

Alignment

(a) Set the Two Tone Generator for a single tone.
(b) Connect the TTG (Two Tone Gen.) output to E-201, Terminals 2 and 4. (Balanced or Unbalanced depending upon output of the TTG.), Insure that the USB and LSB switches are OFF.
(c) Adjust the output level of TTG for 0.025 V Unbalanced, or 0.012 V Balanced. (-30 DBM).
(d) Turn R-213 Max. CW to feed 250 Kc to T-203.
(e) Connect the probe of the VTVM (Ball.) to pin 1 of V-204, plate of the RF amplifier. (Approx. 1 to 2 Volts).
(f) Adjust the top and bottom slugs of T-203 for Max. Indication.
(g) Adjust R-213 and C-216 for Min. Indication on VTVM.
(h) Turn R-244 Max. CW to feed 250 Kc to T-206.
(i) Connect the probe of the VTVM (Ball.) to pin 1 of V-208, plate of the RF amp. (approx. 1 to 2 Volts).
(j) Adjust the top and bottom slugs of T-206 for Max. Indication.
(k) Adjust R-244 and C-233 for Min. on the VTVM.

Adjustment of Combining Network

(a) Connect Ball. VTVM to the out terminal of Z-201; set USB switch to Channel 1, Adjust USB gain for a 0.1 V on the VTVM.

Adjustment of Combining Network - (Continued)

(b) Turn USB switch to OFF (DO NOT touch USB gain Control).
(c) Turn LSB switch to Channel 1, connect VTVM to OUT terminal of Z-203.
(d) Adjust LSB gain control for 0.1 V on the VTVM.
(e) Connect the VTVM to the IN terminal of Z-202: Note VTVM indication. Turn OFF LSB switch and turn USB switch to channel 1, both indications should be the same.
(f) Adjust R-237 until both Sidebands read the same when switching from USB to LSB.

Checking Sensitivity Of USB and LSB Channels

(a) Put the LSB selector switch to Channel 1, put the USB selector switch to OFF, carrier level control to OFF(Max.CCW), LSB gain to Max. CW.
(b) Check with the VTVM that there is 0.05 V at the grid of the first audio amplifier V-207, pin 6.
(c) Connect the VTVM to the 70 ohm resistor connected to J-202, indication should be greater than 0.12 volts(.12 - .2 V).
(d) Put the LSB selector switch to OFF, USB selector switch to Channel 1, USB gain control Max. CW. The VTVM connected to J-202 should again indicate greater than 0.12 Volts.

Meter Adjustments and Carrier Level

(a) USB selector switch to Channel 1, LSB switch OFF, carrier level control to OFF, adjust USB gain control so that the VTVM connected to the dummy load at J-202 indicates 0.12 V.
(b) Adjust R-216 (USB meter adjust) so that the USB meter indicates 100%.
(c) Set LSB selector switch to Channel 1, USB switch to OFF, Carrier level to OFF, adjust LSB gain control so that VTVM connected to J-202 indicates 0.12 Volts.
(d) Adjust R-247 (LSB meter adjust) so that LSB meter indicates 100%.
(e) LSB and USB selector switches to OFF, Carrier level control to 0 DB (Max. CW).
(f) Adjust R-236 (carrier insert) so that VTVM connected to J-202 indicates 0.12 volts.

2. CHECK FOR BANDWIDTH

(a) Connect an audio oscillator across a 600 ohm resistor to terminals 2 and 4 of E-201.
(b) Set the oscillator to have an output of .05 volts at 1Kc.
(c) Set the USB selector switch to OFF.
(d) Set the LSB selector switch to Channel 1.

2. CHECK FOR BANDWIDTH -(Continued)

(e) Connect the probe of the Ballantine meter to output of filter Z-203

(f) Connect counter to the output of filter (same point as previous step).

(g) Vary the audio generator between 250-7500 cycles for the CBE-1, or 250-3500 for the CBE-2 to obtain the peak reading on the meter. Adjust the meter to any convenient reference point. This will appear at approximately 2000 cycles for both units. CBE-1 and CBE-2.

(h) Vary the audio generator towards the lower frequency side 250 cycles for the CBE-1 or 250 cycles for the CBE-2. Note and record the frequency when the meter indicates a reduction of 1db, 2db, and 3db. Now tune the generator towards 7500 cps. Note and record the second frequency at the 1db, 2db, and 3db points. While tuning the generator to 7500 cycles from 250 cycles for the CBE-1, 3500 from 250 cycles for CBE-2, watch the meter for any variation greater than 3db below the point which has been set as a reference point.

(i) Subtract the two frequencies at the 3 db points. This should be less then 7250 cycles for the CBE-1 and 3250 cycles for the CBE-2.

(j) Set the LSB selector switch to OFF.

(k) Set the USB selector switch to Channel 1.

(l) Connect the probe of the Ballantine meter to the output of the USB filter Z-201

(m) Connect counter to the output of filter (same point as previous step).

(n) Vary the audio generator between 250-7500 cycles for the CBE-1, or 250-3500 for the SBE-2 to obtain the peak reading on the meter. Adjust the meter to any convenient reference point. This will appear at approximately 2000 cycles for both units. CBE-1 and 2.

(o) Vary the audio generator towards the lower frequency side, 250 cycles for the SBE-1 or 250 cycles for the SBE-2. Note and record the frequency when the meter indicates a reduction of 1 db, 2 db and 3 db. Now tune the generator towards 7500 cps. Note and record the second frequency at the 1 db, 2 db and 3 db points. While tuning the generator to 7500 cycles from 250 cycles for the SBE-1, 3500 cycles from 250 cycles for the SBE-2, watch the meter for any variation greater than 3 db below the point which has been set as a reference point.

(p) Subtract the two frequencies at the 3 db points. This should be less than 7250 cycles for the CBE-1 and 3250 cycles for the CBE-2.

3. DISTORTION TEST

After having aligned the unit as per 1 and 2 and completed the

3. DISTORTION TEST - (Continued)

alignment of the CHG-2, the distortion test can be made.

Preliminary:

1. Input from TTG to CBE - 0.012 volts (Balanced) o.025 volts (Unbalanced).
2. Output of CBE to CHG should NEVER exceed 0.12 volts.(PEV).
3. Output from CHG(250 Kc) to CBE 1 to 1.3 volts RMS.
4. Set up Panalizer as follows to measure distortion:
   a. gain--Fully clockwise.
   b. Amplitude scale switch to LOG.
   c. Cal. Osc. Level to OFF.
   d. Input attenuation as needed.
   e. Sweep width selector to 10 Kc.
   f. AFC---OFF.
   g. The VOX should be set 500 Kc higher than the output of the CHG-2 output Freq.
   h. VOX Output 0.1 ma.
   i. TTG audio selector switch set for two tones.
5. CHG properly tuned and H.P. VTVM connected as per fig. 2.

TEST

a. Connect the equipment as shown in Fig. 2.
b. Turn the carrier level control OFF.
c. Turn LSB to OFF.
d. Turn USB to channel that audio is coming in on.
e. Adjust USB gain until USB meter indicates 100%, then turn selector switch to OFF.
f. Turn LSB to channel that audio is coming in on.
g. Adjust LSB gain until LSB meter indicates 100%, then turn selector switch to OFF.
h. Adjust carrier level control to 0 DB(Max. Cw).
i. Tune the CHG and set the output level control so that the VTVM connected to J-2704 indicates 8.5 volts.
j. Using the input attenuator switches on the analyzer adjust the amplitude on the screen as close as possible to the zero(0) DB line, then adjust the gain control so that the indication is zero(0) DB.
k. Now turn the Carrier level control OFF(Max. CCW). The carrier should be down on the analyzer screen a - 55 DB. If anything else appears on the screen it should be down - 60 DB.

TEST -(Continued)

l. Turn USB selector switch to appropriate channel, two tones should appear on the screen at - 6 DB and intermodulation distortion should be down - 45 DB from the two tones or - 51 DB from original setting.

m. Check the LSB by the same method as above with the USB OFF and using the appropriate controls.

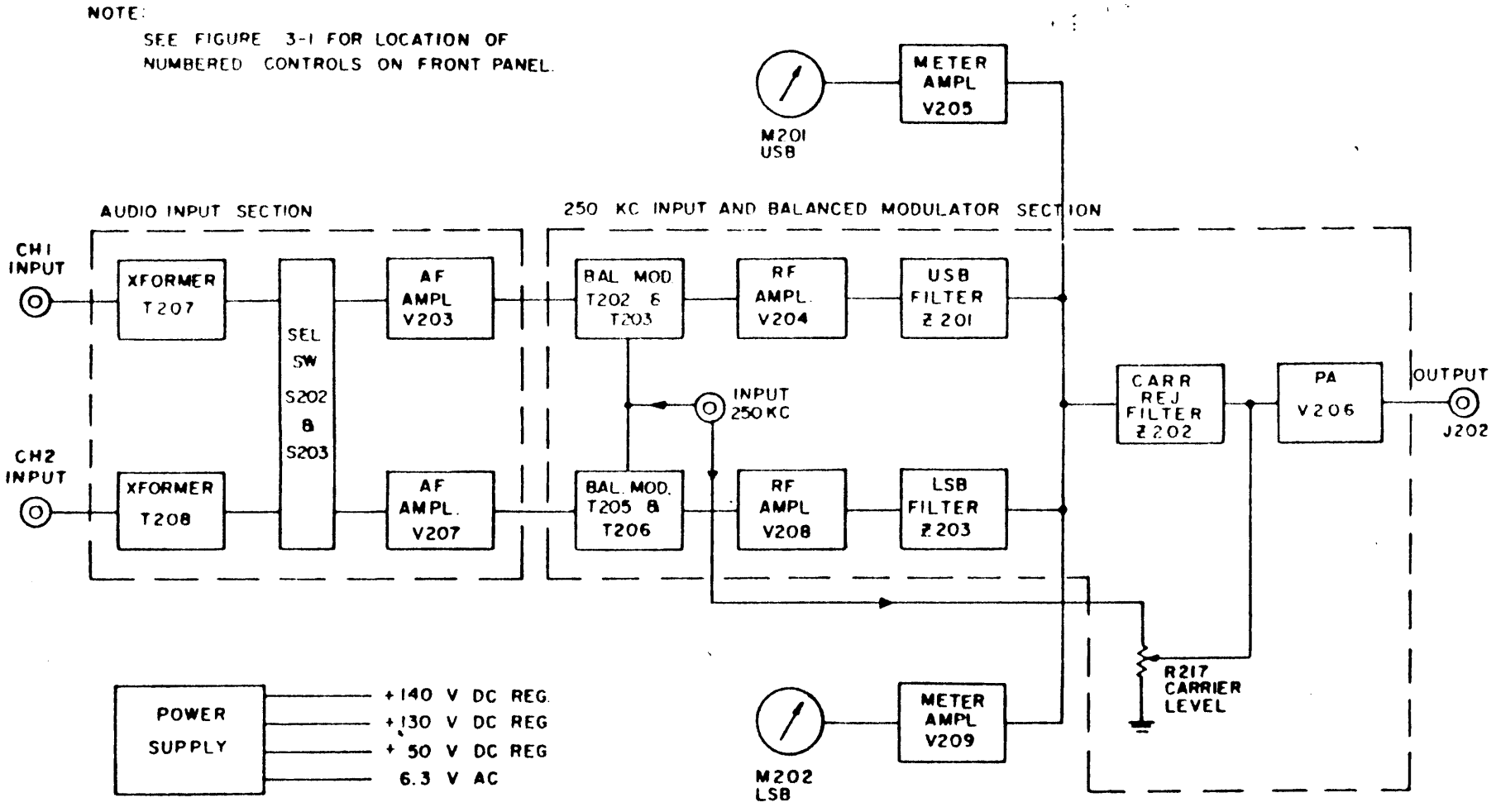


Figure 4-1. Block Diagram, CBE Sideband Exciter

FOR 230 VOLT OPERATION OF T201

1- REMOVE JUMPERS BETWEEN TERMINALS 1&2 AND 3&4

2- ADD JUMPER BETWEEN 2&3

NOTES:

1. SEE FIGURE 3-1 FOR LOCATION OF NUMBERED CONTROLS ON PANEL
2. UNLESS OTHERWISE NOTED -
   - ALL RESISTORS ARE 1/2 WATT
   - ALL CAPACITOR VALUES ARE IN UF
   - ALL COIL VALUES ARE IN UH
3. ⊘ INDICATES SCREWDRIVER CONTROL ON CHASSIS

0066120106

Figure 6-1 Schematic Diagram, Sideband Exciter, CRE-1 and -2

SECTION 7

TITLE: FREQUENCY AMPLIFIER MODEL CHG-2 (AM-2505A/URA-31)

OBJECTIVES:

a) to discuss the role of the Frequency Amplifier Model CHG-2 in the Synthesized Sideband Generator system.

b) to investigate the circuitry of the various sub units of the Model CHG-2, by means of block diagrams and circuit schematics.

c) to trace signals through the system in various positions of the bandswitches.

d) to discuss the alignment procedure in detail, as an aid in understanding the operation of the system.

e) to demonstrate, with appropriate test equipment, the alignment of the unit. This may be done concurrently with item (d) above.

REFERENCES:

a) Technical Manual for Frequency Amplifier Model CHG-2, (Amplifier, R.F., AM-2505A/URA-31)

b) Production Test Specification S-609, modified by this lesson plan.

c) Production Test Specification S-528 (I.F. Chassis)

d) Production Test Specification S-529 (Regenerative Divider)

e) Schematic CK-505 (complete schematic of unit)

TRAINING AIDS:

a) VTVM: Hewlett Packard Model 410B, or equivalent.

b) Oscilloscope: Tektronics Model 545A, or equivalent.

c) Frequency Counter: H.P. Model 524C, or equivalent.

d) Two signal generators, Measurements Corp. Model 82, or equivalent.

e) 70 ohm dummy load.

PRESENTATION:

A. General Description of CHG-2 Using Block Diagrams:

1. The general block diagram of the CHG-2 Frequency Amplifier is drawn on the following pages in two parts.

2. It should be noted that the switching arrangement shown in Part 2 is a simplified form of the actual switching scheme, and is drawn thus for explanation purposes only.

Figure 1: Part 1 of CHG-2 Block Diagram

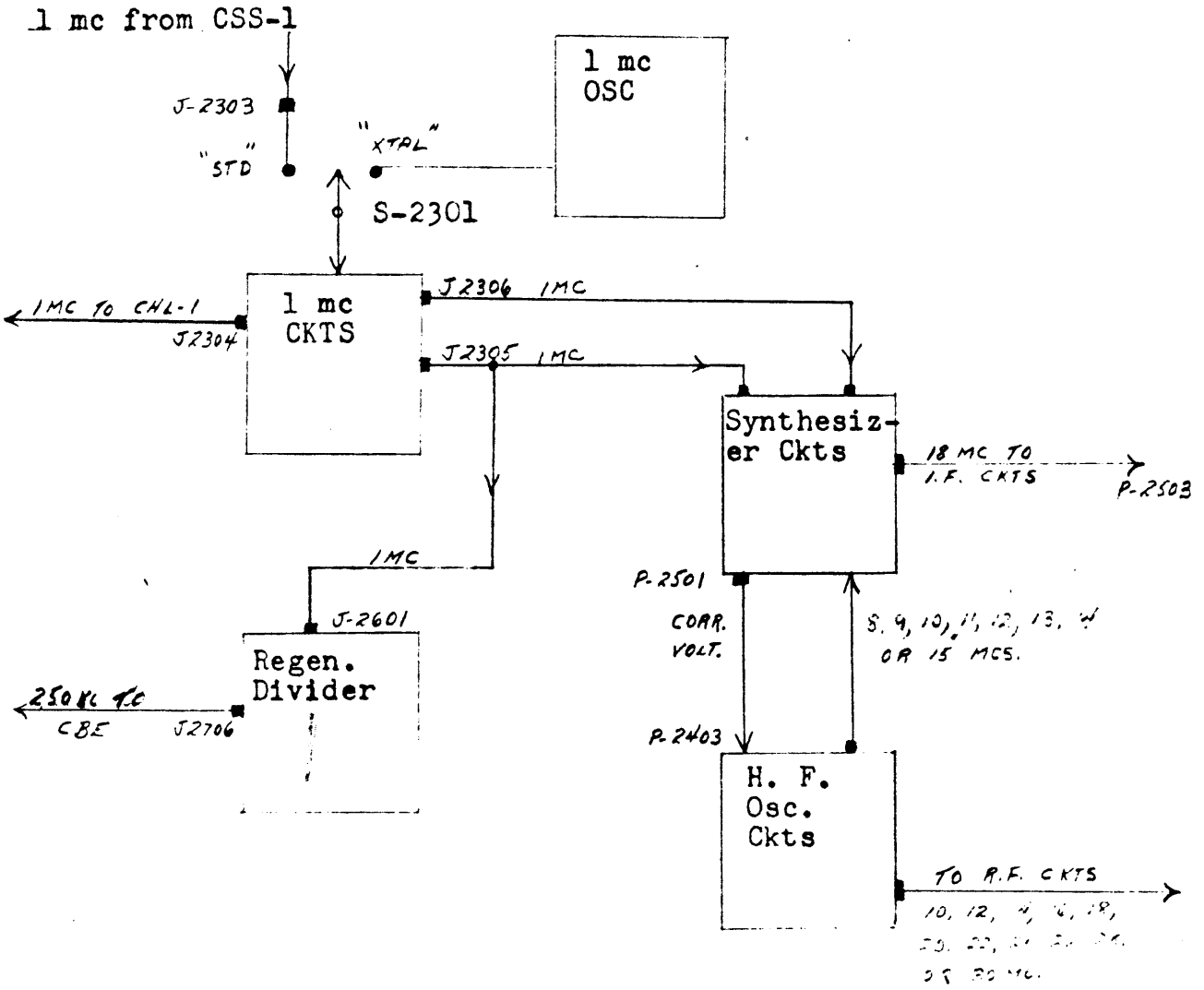


Figure 2: Part 2 of CHG-2 Block Diagram:

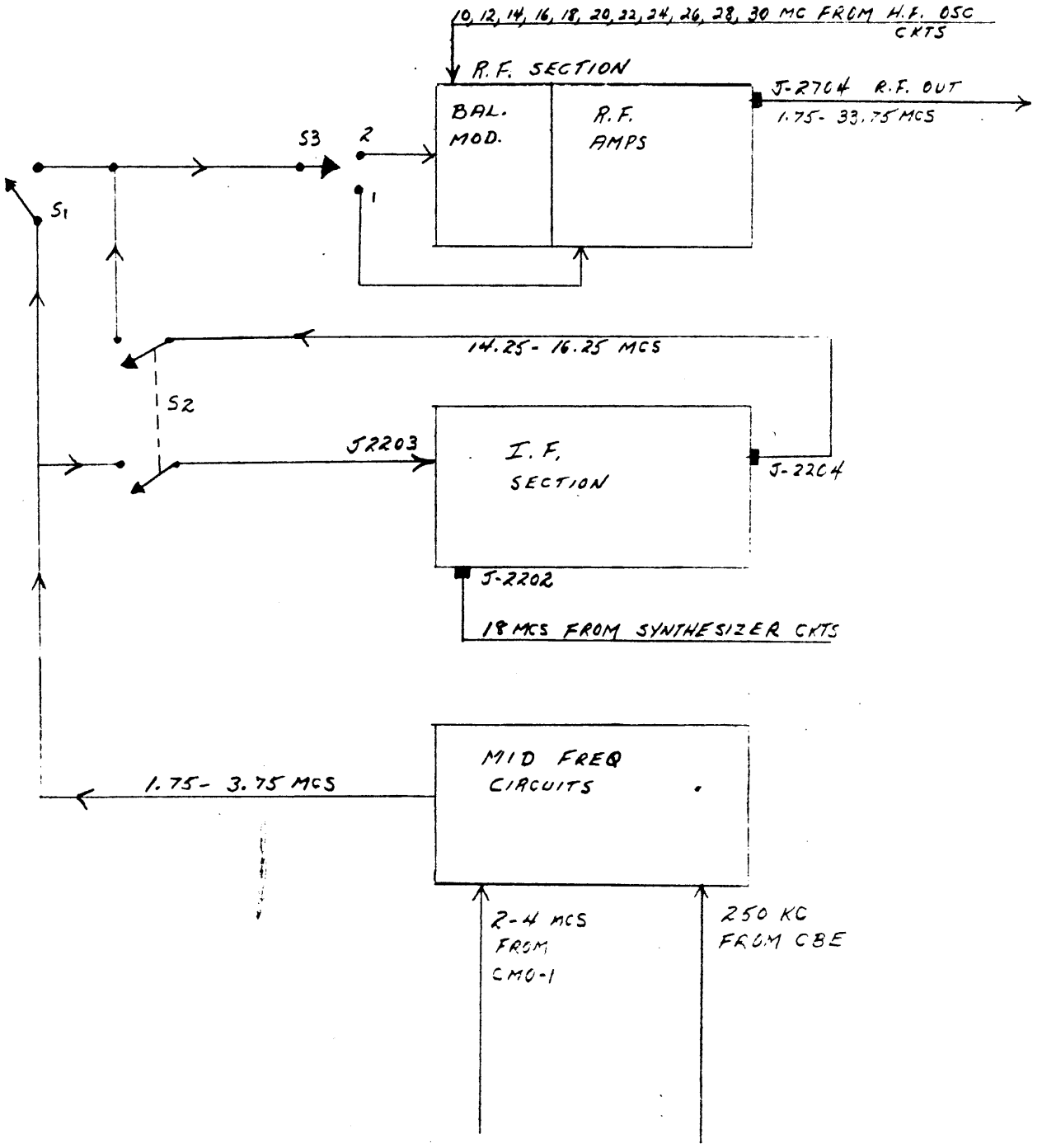
note:

S-1 closed on all bands except 2B, 4B, 6C, and 8C.

S-2 closed on bands 2B, 4B, 6C, and 8C; open on all other bands.

S-3 at position 1 on Band OA.

S-3 at position 2 on all bands except OA.



3. Frequency Amplifier Model CHG-2 may be considered, for analysis purposes, as a unit composed of seven functional sections. These sections are:

a) The One Megacycle Circuits.
b) The Regenerative Divider.
c) The Synthesizer Circuits.
d) The High Frequency Oscillator Circuits.
e) The I.F. Circuits.
f) The Mid Frequency Circuits.
g) The R.F. Circuits.

4. The One Megacycle Circuits:

A 1 mc signal from Frequency Standard Model CSS-1 enters at J-2303; this is connected to a selector switch, S-2301. The output of an internal 1 mc oscillator is also connected to S-2301. Depending upon the position of S-2301, the 1 mc amplifiers are excited with a 1 mc signal from either the internal or external source.
At J-2304, a 1 mc signal is taken out for application to the Frequency Divider Chain, Model CHL-1.
One megacycle outputs are taken at J-2305 and J-2306 for application to the synthesizer and regenerative divider circuits.

5. The Regenerative Divider:

The Regenerative Divider receives a 1 mc input at J-2601 and delivers, at J-2706, a 250 KC sub carrier locked to the accurate 1 mc input. The 250 KC sub carrier is fed to the Sideband Exciter, Model CBE.

6. The Synthesizer Circuits:

The Synthesizer circuits receive two 1 mc inputs from the 1 mc circuits, and switch selected frequencies of 8, 9, 10, 11, 12, 13, 14 and 15 mc from the High Frequency Oscillator circuits.
The synthesizer circuits perform two main functions:

a) they stabilize the output of the High Frequency Oscillator circuits.

b) they provide an 18 mc signal for use in the I.F. section.

7. The High Frequency Oscillator Circuits:

The High Frequency Oscillator Circuits provide switch selected stabilized injection frequencies of 10, 12, 14, 16, 18, 20, 22, 24, 26, 28 and 30 mcs to the balanced modulators in the RF section for final frequency translation.
In addition, they furnish switch selected frequencies of 8, 9, 10, 11, 12, 13, 14 and 15 mcs to the synthesizer circuits for use in generating the correction voltage.
The High Frequency Oscillator circuits receive a correction voltage from the synthesizer circuits; this correction voltage is applied to a varicap to stabilize the High Frequency Oscillator.

8. The I.F. Circuits:

The I.F. Section is used only for Bands 2B, 4B, 6C and 8C, which cover the range of 3.75 to 11.75 mcs. An 18 mc signal from the synthesizer circuits is mixed, in a balanced modulator, with a 1.75 to 3.75 mc signal from the Mid Frequency circuits. The output, in the range of 14.25 to 16.25 mcs, is amplified in an IF strip and applied to the R.F. section.

9. The Mid Frequency Circuits:

The Mid Frequency Circuits receive a 250 KC signal from the Sideband Exciter Model CBE, and a 2 to 4 mc signal from the Controlled Precision Oscillator system. These are mixed in a balanced modulator circuit to produce frequencies in the range 1.75 to 3.75 mcs. The output is delivered direct to the RF amplifiers in the RF section on Band OA; to the I.F. section on bands 2B, 4B, 6C, and 8C; and to the balanced modulators in the R.F. section on all other bands.

10. The R.F. Section:

The RF Section consists of a balanced modulator and cascaded linear amplifiers. Final frequency translation is accomplished in the balanced modulator. One input to the balanced modulator arrives from either the IF section or the Mid Frequency section; the second input is a stabilized switch selected frequency of 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, or 30 mcs, from the High Frequency Oscillator circuits.
The balanced modulator is bypassed on band OA.
The RF output is in the range 1.75 to 33.75 mcs.

B. General Signal Tracing Using the Block Diagram, Part 2:

1. This is an introduction to signal tracing in the CHG-2 system, using the block diagram, part 2. No attempt will be made at this time to include details on sidebands, sideband inversions or detailed analysis.

2. For simplicity, it will be assumed that the inputs to the Mid Frequency Circuits are:

   a) a 250 KC carrier from Sideband Exciter Model CBE.

   b) a 2 mc frequency from the CMO-1.

3. Band "0A": (Bandswitch position #1)

   a) S-1 closed.
   b) S-2 open.
   c) S-3 to position #1.
   d) output of the Mid Frequency circuits: 1.75 mcs.
   e) direct to RF amplifier circuits.
   f) R.F. output frequency is 1.75 mcs.

4. Bands "2B", "4B", "6C", "8C":
   (Bandswitch positions #2, #3, #4, and #5.)

   a) S-1 open.
   b) S-2 closed.
   c) S-3 to position #2.
   d) output of Mid Frequency circuits: 1.75 mcs.
   e) applied to I.F. section.
   f) Output of I.F. section: Band 2B: 16.25 mcs.
      4B: 16.25 mcs.
      6C: 16.25 mcs.
      8C: 16.25 mcs.

   g) I.F. output applied to balanced modulator in the R.F. section.

   h) High Frequency Oscillator injection frequencies applied to balanced modulators in R. F. section:

      Band 2B: 20 mcs.
      Band 4B: 22 mcs.
      Band 6C: 24 mcs.
      Band 8C: 26 mcs.

   i) R.F. amplifiers tuned to DIFFERENCE frequency.

j) R. F. output Band 2B: 3.75 mcs.
4B: 5.75 mcs.
6C: 7.75 mcs.
8C: 9.75 mcs.

5. Bands "10C", "12C", "14D", "16D", "18D", "20D", "22D", "24D", "26D", "28D", and "30D":
(Bandswitch positions 6 through 16)

a) S-1 closed.
b) S-2 open.
c) S-3 at position #2.
d) output of mid frequency circuits: 1.75 mcs.
e) R.F. amplifiers tuned to SUM frequency.
f) Table below shows injection frequencies and RF output frequencies.

BAND	MID FREQ	H.F. INJECTION	R.F. OUT
10C	1.75 mcs.	10 mcs.	11.75 mcs.
12C	"	12 mcs.	13.75 mcs.
14D	"	14 mcs.	15.75 mcs.
16D	"	16 mcs.	17.75 mcs.
18D	"	18 mcs.	19.75 mcs.
20D	"	20 mcs.	21.75 mcs.
22D	"	22 mcs.	23.75 mcs.
24D	"	24 mcs.	25.75 mcs.
26D	"	26 mcs.	27.75 mcs.
28D	"	28 mcs.	29.75 mcs.
30D	"	30 mcs.	31.75 mcs.

C. Detailed Analysis of the CHG-2 Circuitry:

1. The detailed analysis of the CHG-2 circuitry will be carried out with the aid of block diagrams, the alignment instructions, and a frequency chart. The block diagrams show all adjustments referred to in the alignment instructions, and the frequency chart shows, for each position of the bandswitch:

   a) the Dial Designation.

   b) the frequency output of the High Frequency Oscillator. (P-2402) (J-2307)

   c) the frequency output of the High Frequency Amplifier circuits; this is the RF injection frequency at C-2776.

   d) the output frequency of the Harmonic Generator, V-2502.

   e) the RF output frequency range of the CHG-2.

2. The 1 mc Circuits:

   a) Refer to:

      (1) Figure 3: Block Diagram, 1 mc circuits.

      (2) Alignment Instructions: 1 mc Circuits.

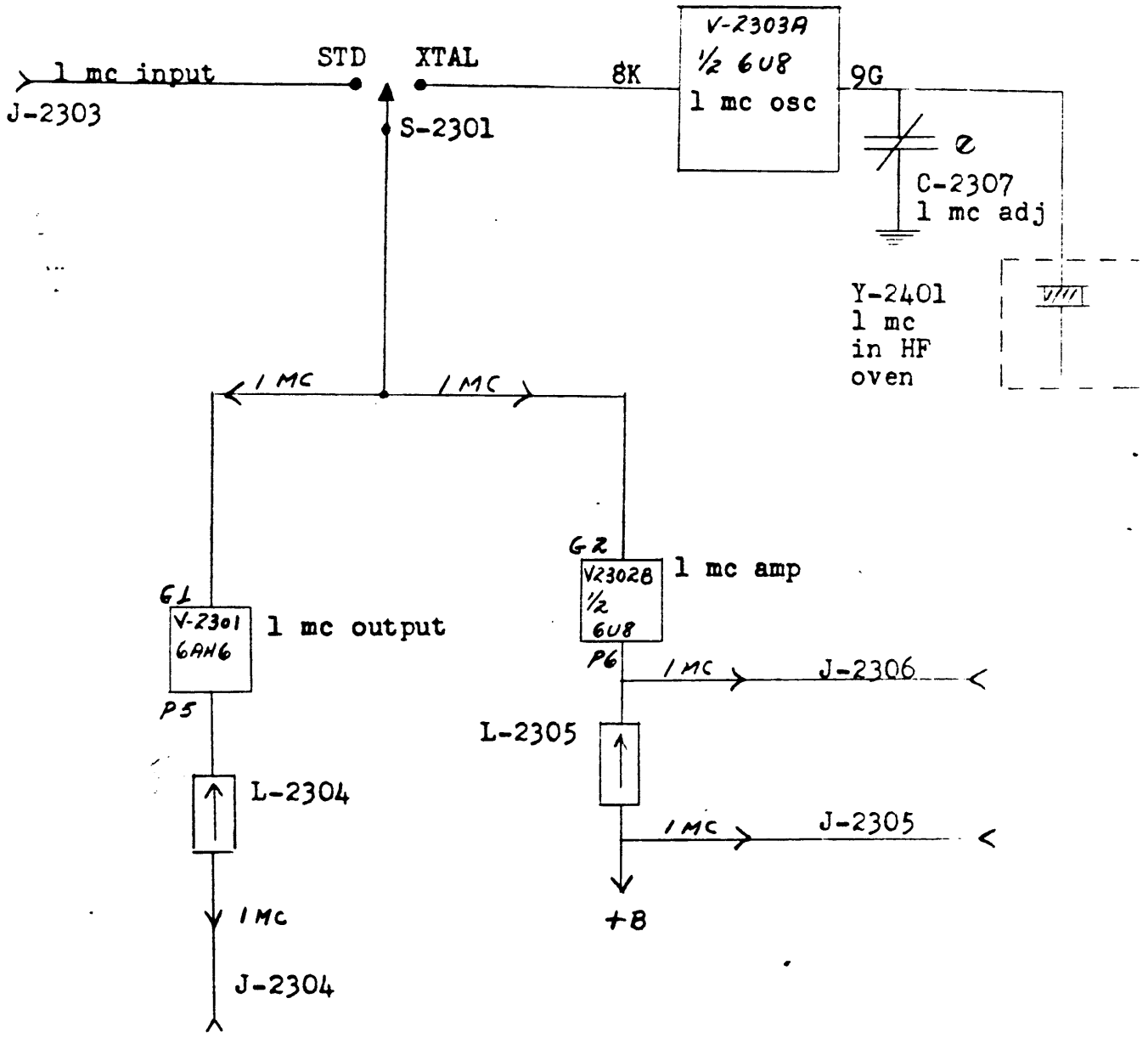
      (3) Figure III(A)-4-2b: Schematic in technical manual.

   b) The 1 mc signal from Frequency Standard Model CSS-1 enters at J-2303, and is conducted to selector switch S-2301. Internal 1 mc oscillator operates when S-2301 is thrown to the "XTAL" position; when S-2301 is in the "STD" position, B Plus is removed from this unit. The 1 mc crystal Y-2401 is contained in the High Frequency Oscillator Oven. Capacitor C-2307 adjusts the frequency of the 1 mc internal oscillator to exactly 1 mc.

   c) In either position of S-2301, a 1 mc signal is applied to two 1 mc amplifiers, V-2301 and V-2302B. Inductors L-2304 and L-2305 are peaked at 1 mc. The 1 mc output at J-2304 is delivered to the Frequency Divider Unit, Model CHL-1. The two 1 mc outputs at J-2305 and J-2306 are applied to the synthesizer circuits and the regenerative divider circuits.

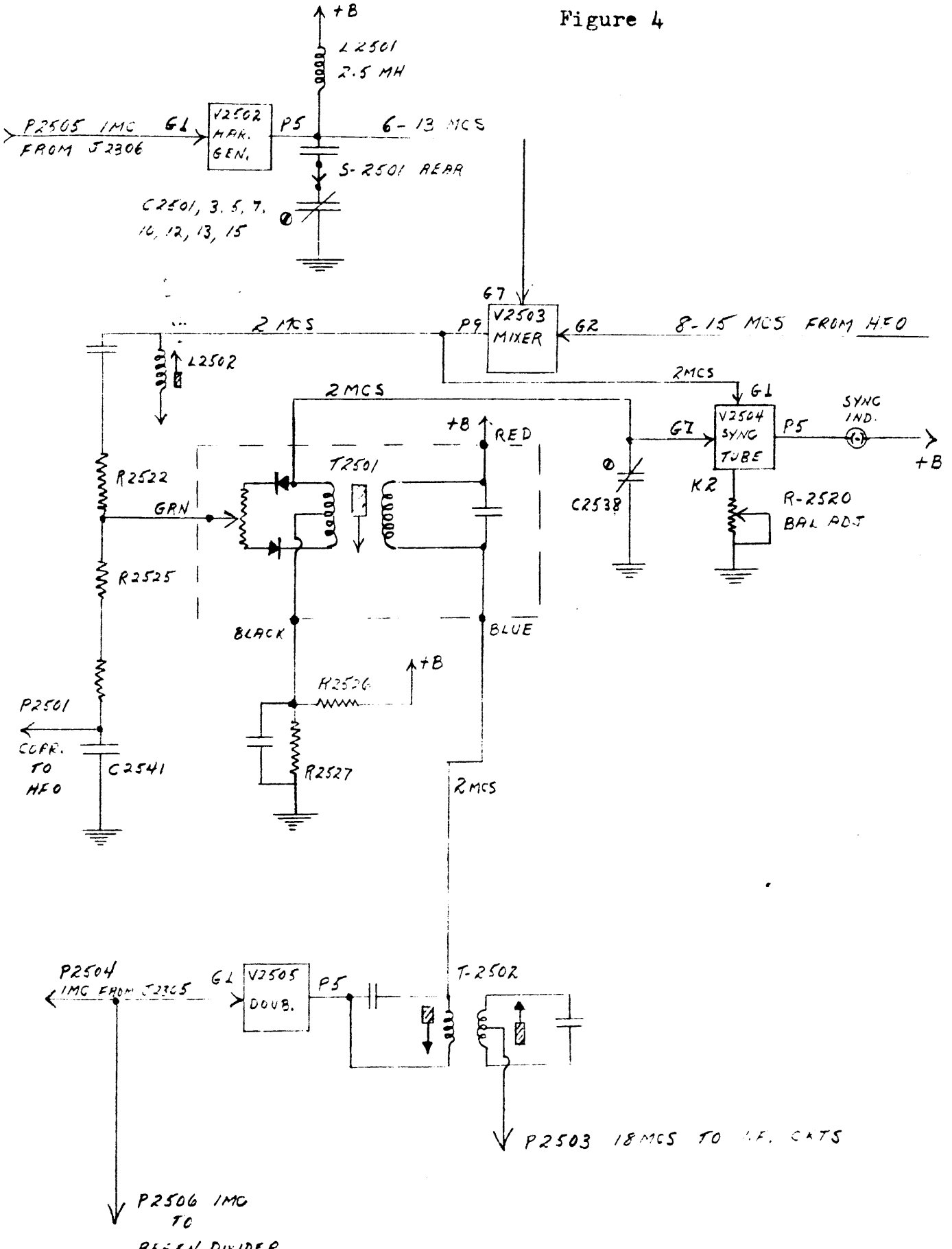
   d) Instructor should now go through the alignment instructions for the 1 mc circuits, with the aid of the block diagram.

Block Diagram: 1 mc Circuits Figure 3



Block Diagram: Synthesizer and Sync Indicator Circuits:

Figure 4



3. Synthesiz r Circuits:

a) Refer to:

(1) Figure 4: Block Diagram, Synthesizer Circuits.

(2) Alignment Instructions: Synthesizer Circuits.

(3) Figure III(A)-4-3b: Schematic in technical manual.

b) A 1 mc signal from the 1 mc circuits enters at P-2504, and is applied to a doubler circuit, V-2505, and to P-2506; the latter output is delivered to the regenerative divider circuits.
Doubler V-2505 doubles the 1 mc input signal; the 2 mc signal at the plate, Pin #5, is applied to the phase detector circuit at the BLUE lead. This is the reference or standard input to the phase detector, since it is locked to an accurate 1 mc standard.

c) A 1 mc signal from the 1 mc circuits enters at P-2505 and is applied to harmonic generator V-2502. In the plate circuit of V-2502, various capacitors are switched in parallel with inductor L-2501 by means of bandswitch section S-2501 (rear). These parallel resonant circuits use trimmer capacitors C-2501, 3, 5, 7, 10, 12, 13 and 15 to adjust th output frequencies as required. Depending on the position of the bandswitch, the output of harmonic generator V-2502 is a frequency of 6, 7, 8, 9, 10, 11, 12 or 13 mcs. This is applied to mixer tube V-2503, at pin #7.

d) The second input to mixer V-2503 at pin #2 is the output frequency of the high frequency oscillator. Depending on the position of the bandswitch, this frequency may be 8, 9, 10, 11, 12, 13, 14 or 15 mcs.

e) It will be noted from the Frequency Chart, Table 1, that, in any position of the bandswitch, the input to mixer V-2503 from the high frequency oscillator circuit is always 2 mc higher than the input from harmonic generator circuit V-2502. Thus, the output of mixer V-2503 is always a 2 mc signal; this signal, is liable to error, since it depends on the high frequency oscillator. The output of mixer V-2503, at pin #9, is applied to the phase detector circuit via the balance adjust pot. L-2502, an inductor in the mixer plate circuit, is peaked at 2 mcs.

Table #1:

Relationships Among:

a) Bandswitch Position.
b) Dial Designation.
c) High Frequency Oscillator Output. (P-2402) (J-2307)
d) High Frequency Amplifier Output to R.F. Circuits at C-2776.
e) Output of Harmonic Generator V-2502.
f) R.F. Output Frequency Range.

BAND SWITCH	DIAL DESIG	OUTPUT HFO	OUTPUT H.F. AMP	OUTPUT HAR. GEN.	OUTPUT RANGE R.F. FREQUENCY
1	0A	10 mc	20 mc	8 mc	1.75 to 3.75 mc
2	2B	10 mc	20 mc	8 mc	3.75 to 5.75 mc
3	4B	11 mc	22 mc	9 mc	5.75 to 7.75 mc
4	6C	12 mc	24 mc	10 mc	7.75 to 9.75 mc
5	8C	13 mc	26 mc	11 mc	9.75 to 11.75 mc
6	10C	10 mc	10 mc	8 mc	11.75 to 13.75 mc
7	12C	12 mc	12 mc	10 mc	13.75 to 15.75 mc
8	14D	14 mc	14 mc	12 mc	15.75 to 17.75 mc
9	16D	8 mc	16 mc	6 mc	17.75 to 19.75 mc
10	18D	9 mc	18 mc	7 mc	19.75 to 21.75 mc
11	20D	10 mc	20 mc	8 mc	21.75 to 23.75 mc
12	22D	11 mc	22 mc	9 mc	23.75 to 25.75 mc
13	24D	12 mc	24 mc	10 mc	25.75 to 27.75 mc
14	26D	13 mc	26 mc	11 mc	27.75 to 29.75 mc
15	28D	14 mc	28 mc	12 mc	29.75 to 31.75 mc
16	30D	15 mc	30 mc	13 mc	31.75 to 33.75 mc

f) The correction voltage developed at the phase detector balance adjust potentiometer is filtered and applied to P-2501, from which point it is delivered to a varicap in the high frequency oscillator circuit, to maintain the output frequency of that unit constant.

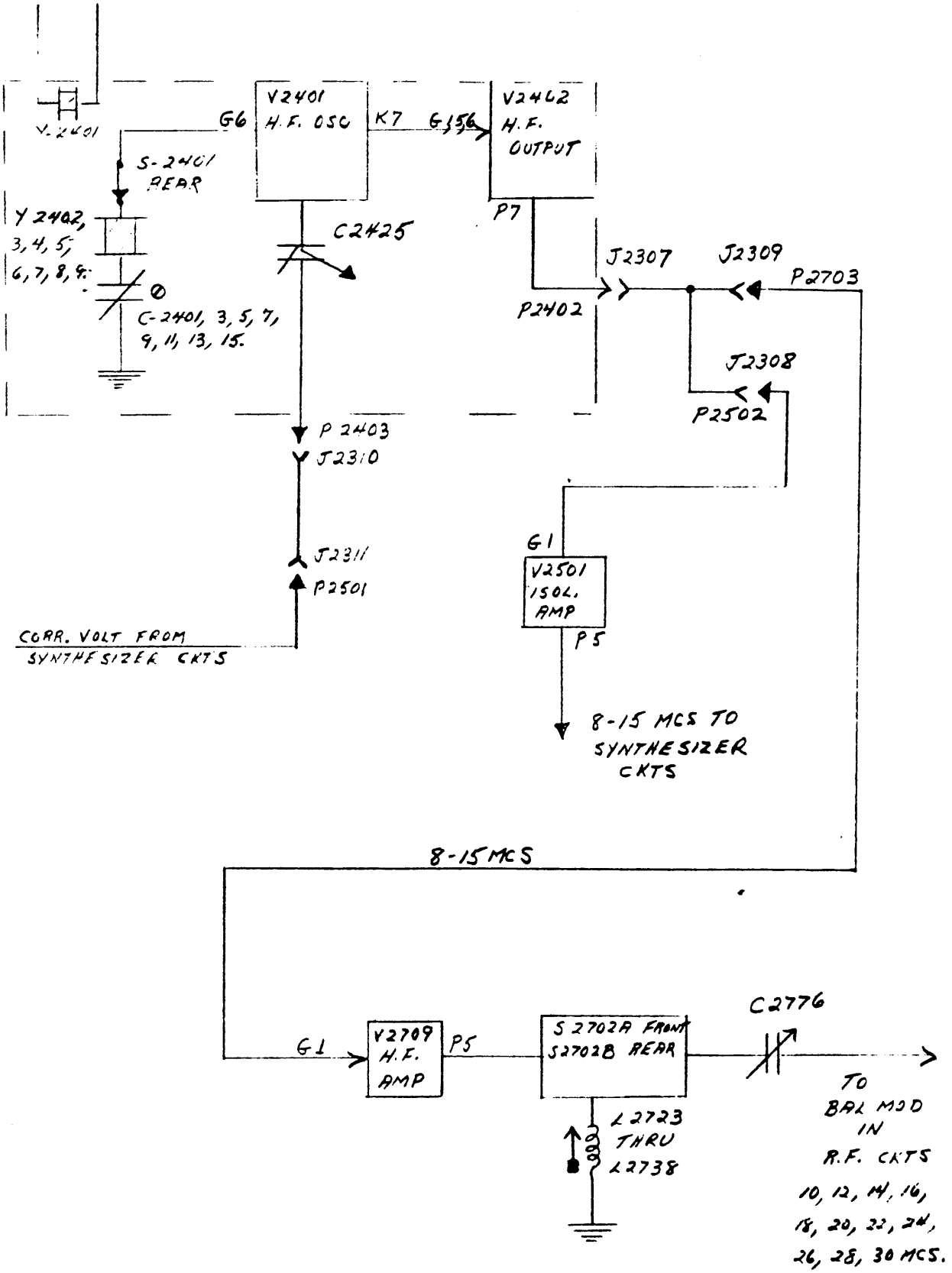
g) T-2502, the double tuned tank in the plate circuit of V-2505, is peaked at 18 mcs. The output from the center tapped secondary is applied to P-2503, from which point the 18 mcs is sent to the I.F. section.

h) The Sync Indicator circuit is included in the synthesizer chassis and its operation will now be discussed. It should be noted, however, that the sync circuit is not adjusted until after the High Frequency oscillator circuits have been aligned.
The 2 mc "standard" input to the phase detector is also applied to grid 3, pin #7 of Sync tube V-2504. The 2 mc difference frequency from mixer V-2503 is applied to grid 1, pin #1 of the sync tube. The two sync tube inputs are applied via phase shifting networks. The phase shift of the signal applied to grid 1, pin #1 of the sync tube may be varied by adjustment of C-2538. The bias on the sync tube is varied by adjustment of R-2520.
When the 2 mc inputs to the phase detector are of the proper phase to "lock in" the high frequency oscillator, the sync tube inputs are in phase, and cause sufficient plate current in V-2504 to ignite I-2102, the front panel sync indicator.

i) The instructor should now go through the alignment instructions for the Synthesizer Circuits, using the block diagram, figure 4, and the Frequency Chart, Table 1.

Block Diagram: High Frequency Oscillator- Amplifier Circuits

Figure 5



4. High Frequency Oscillator - Amplifier Circuits:

a) Refer to:

(1) Figure 5: Block Diagram, High Frequency Oscillator Amplifier Circuits.

(2) Figure 4: Block Diagram, Synthesizer and Sync Indicator Circuits.

(3) Figure III(A)-4-2b: schematic of Oven-Oscillator circuits in technical manual.

(4) Figure III(A)-4-5b: schematic of Mid Frequency and RF Deck subassembly in technical manual.

(5) Alignment Instructions: High Frequency Injection Oscillator, Sync Circuit Indicator, and High Frequency Amplifier.

b) The oven assembly indicated by the dashed outline contains the RF oscillator and output tubes, V-2401 and V-2402. In the oscillator section, bandswitch section S-2401 (rear) selects crystals Y-2402 through Y-2409 and trimmer capacitors C-2401, 3, 5, 7, 9, 11, 13 and 15. Depending on the position of the bandswitch, the output of the oscillator at the cathode, pin #7, is a frequency of 8, 9, 10, 11, 12, 13, 14 or 15 mcs, which is applied to RF output tube V-2402. The output of V-2402, which is broadly tuned, is applied to external circuitry via P-2402 and J-2307. Crystal Y-2401 is the 1 mc crystal employed in the internal 1 mc oscillator circuit already discussed. The correction voltage from the phase detector in the synthesizer circuits arrives at J-2311 and is applied via J-2310 and P-2403 to C-2425, a varicap, which acts to correct the frequency of the oscillator circuit.

c) One of the 8 through 15 mc outputs of the oven circuits is applied via J-2309 and P-2703 to the high frequency amplifier circuits of V-2709 and associated switches S-2702A (front) and S-2702B (rear) in conjunction with inductors L-2723 through L-2738. Depending on the position of the bandswitches, straight through operation or doubling action is utilized. The output of the high frequency amplifier circuits may be a frequency of 10, 12, 14, 16, 18, 20, 22, 24, 26, 28 or 30 mcs. This is delivered to the balanced modulators in the RF circuits via C-2776.

d) The instructor should now go through the alignment procedure for the HF injection oscillator, the Sync circuit indicator and the High Frequency amplifier, using the block diagrams.

5. Medium Frequency Circuits:

a) Refer to:

(1) Figure 2: (Part 2 of general block diagram)

(2) Alignment Instructions: Medium Frequency Circuits.

(3) Figure III(A)-4-5b: Mid Frequency and RF Deck subassembly schematic in technical manual.

b) The analysis of the mid frequency circuits can best be accomplished with the aid of the actual schematic instead of a block diagram.

c) At J-2701, the 250 KC input from the Sideband Exciter, Model CBE, enters. This input, which may be a pure 250 KC carrier, or single, double or independent sideband intelligence with various degrees of carrier reinsertion, is applied in push pull to the grids of balanced modulator V-2701. The band pass at the input is determined by the Model CBE used.

d) The input from the CMO-1 enters at J-2702. This input may be any frequency from 2 to 4 mc synthesized in 100 cycle steps, or continuous without synthesization. It is applied in parallel to the cathodes of V-2701. The output circuits are tuned to the difference frequencies.

e) The output at the secondary of T-2702 is an inverted output; since the injection frequency is higher than the intelligence frequency, the sidebands become inverted in translation. This is not important, because other inversions will cause the final spectrum to be normal.

f) The remainder of the circuitry consists of a tuned amplifier covering the range 1.75 to 3.75 mcs, and a metering circuit.
The dashed line connected to R-2102, C-2711A, C-2711B, C-2716A and C-2716B represents a ganged tuning arrangement, adjusted by the MF TUNING control on the front panel.
A portion of the output is sampled at T-2703 and is applied to meter amplifier V-2703. The output of V-2703 is rectified by CR-2701, is filtered then applied to M-2101, the front panel MID FREQUENCY TUNING meter.

g) At J-2703 an input is provided for "ALDC". This is "Automatic Load and Drive Control". It prevents overdriving the RF stages of an associated transmitter on signal peaks. The output of an RF amplifier in the associated transmitter is rectified and filtered to produce a negative voltage proportional to the peak RF. This varies the bias on balanced modulator V-2701.

h) The instructor should now go through the alignment procedure for the Mid Frequency circuits, using the circuit schematic.

i) The instructor should now refer to the circuit schematic, and trace a signal from the mid frequency circuits to the RF section on bandswitch positions 1, 2 through 5, and 6 through 16, corresponding to Dial Designations 0A, 2B, 4B, 6C, 8C, and 10C through 30D.
The following points should be stressed:

(1) On bandswitch position 1, Dial designation 0A, the Mid frequency signal is sent directly to the first RF amplifier circuit; the IF circuits and the balanced modulator in the RF section are rendered ineffective.

(2) On bandswitch positions 2 through 5, corresponding to dial designations 2B through 8C, the output of the medium frequency circuits is sent to the IF section; the output of the IF section is sent to the balanced modulator in the RF section.

(3) On bandswitch positions 6 through 16, corresponding to dial designations 10C through 30D, the output of the mid frequency section is sent direct to the balanced modulator in the RF section, and the IF section is rendered ineffective.

6. The I.F. Circuits:

a) Refer to:

(1) Figure 2: (Part 2 of General Block Diagram).

(2) Figure III(A)-4-4b: I.F. Section, CHG-2, schematic in the technical manual.

b) The I.F. section consists of two 18 mc amplifiers, a balanced modulator, and four stages of I.F. amplification. The 18 mc signal from the synthesizer circuits is applied at J-2202, and is amplified in tuned amplifiers V-2201 and V-2202. The input from the Mid Frequency Circuits, on bandswitch positions 2,3,4 and 5 arrives at J-2203. Both inputs are applied to a balanced modulator circuit. Since the injection frequency is higher than the intelligence frequency, and the I.F. amplifiers are tuned to the difference frequencies, inversion takes place. The output of the I.F. unit in the range 14.25 to 16.25 mcs, leaves the unit at J-2204.

c) Note that B Plus is applied to the I.F. section on positions 2,3,4 and 5 of bandswitch section S-2403 (front). Thus, the I.F. section is rendered inoperative on all other bandswitch positions.

d) Since each IF assembly is factory adjusted separately from the CHG-2 unit, no IF alignment procedure is contained in the alignment instructions. Should re-alignment become necessary, the following procedure is recommended:

<u>18 mc Amplifiers</u>:

(1) Set bandswitch to position 2, 3, 4 or 5, corresponding to dial designations 2B, 4B, 6C or 8C. This insures that B Plus is applied.

(2) Connect a signal generator set to 18 mcs to J-2202.

(3) Connect a VTVM or oscilloscope to either YELLOW lead of T-2208. Set the balance adjust pot R-2209 to approximate center.

(4) Remove the input from J-2203.

(5) During alignment, reduce the signal generator output to the minimum required for indication on the scope or VTVM, to prevent overloading the 18 mc amplifiers.

(6) Peak both primary and secondary of T-2201 and T-2202 for maximum 18 mc indication on the VTVM or oscilloscope.

(7) The indication on the VTVM or scope should be approximately 0.4 volts RMS for 25 millivolts input at J-2202. RECORD THIS VOLTAGE.

(8) Connect a Ballentine AC VTVM to the BLUE lead of T-2203. Set R-2209 for minimum indication and carefully lock the adjustment. The indication at the BLUE lead should be down 20 db from the indication recorded in step (7) above. This is a voltage ratio of 10:1. If the voltage indication at the YELLOW lead was 0.4 volts RMS, the voltage at the BLUE lead should be .04 volts RMS, or less.

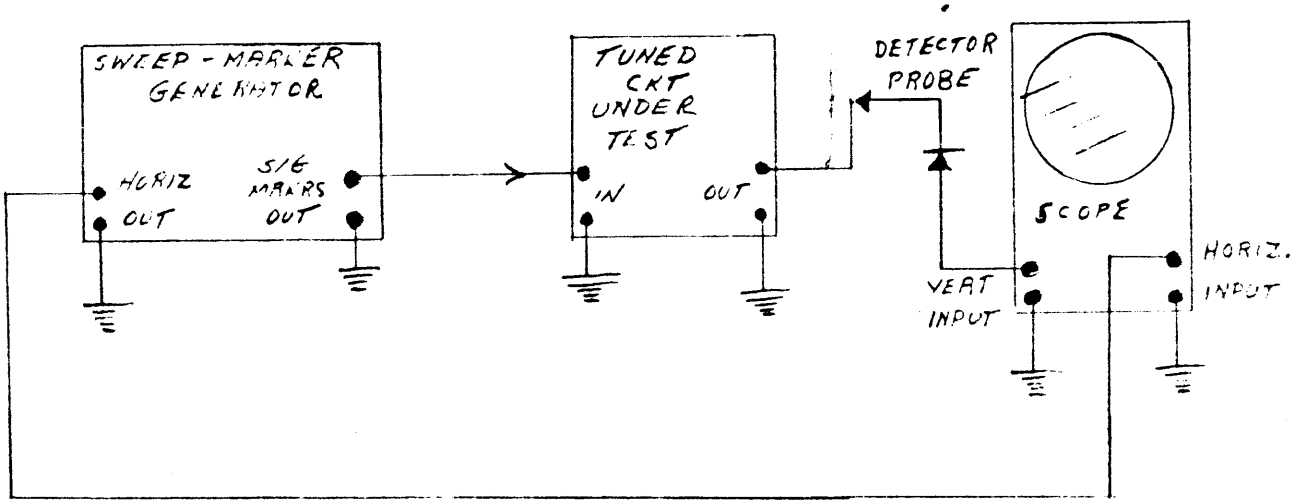
(9) Disconnect all test equipment.

I.F. Amplifiers:

Note: The alignment procedure for the I.F. amplifiers will vary, depending on the degree of misalignment. The following procedure is the most effective, but it requires the use of a Sweep-Marker Generator. A second alignment procedure will be given in case the Sweep-Marker Generator is not available.

I.F. Amplifier Alignment Using Sweep-Marker Generator:

(1) Connect the test equipment as shown below:



(2) Turn on the Sweep-Marker generator, and set the output for a center frequency of 15.25 mcs, and a sweep width of about 3 mcs.

(3) Connect the output of the Sweep Marker generator to pin #1 of V-2203.

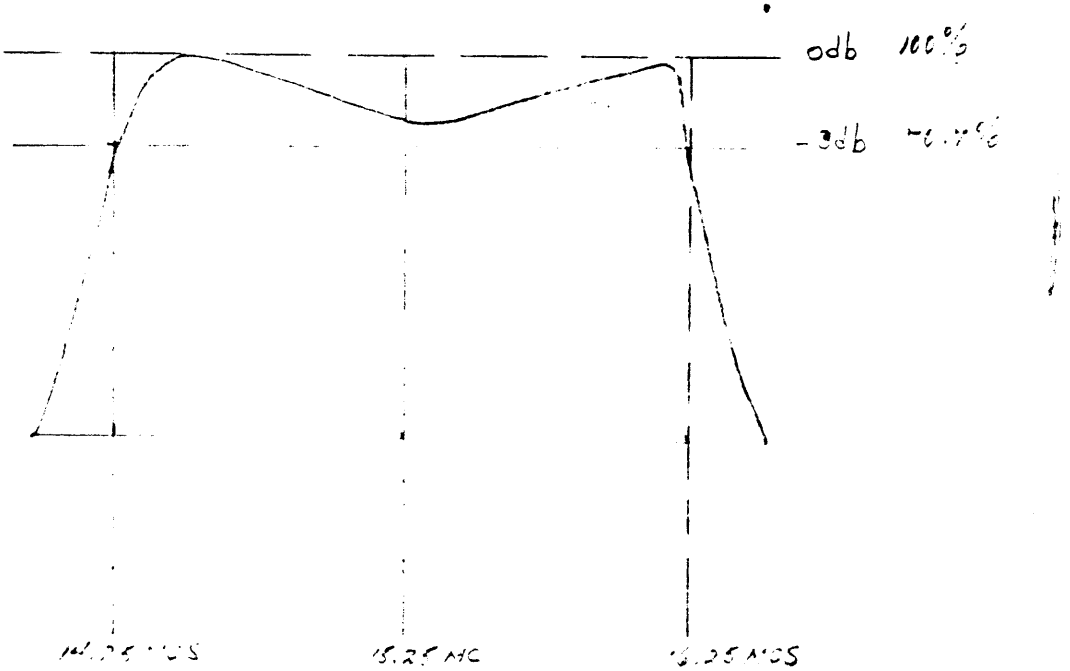
(4) Disconnect the inputs at J-2202 and J-2203.

(5) Connect the detector probe to the output jack, J-2204.

(6) Carefully adjust the Sweep-Marker generator gain, the oscilloscope gain, the sweep width, the horizontal phasing control and other associated controls on the test equipment to obtain a frequency response pattern on the oscilloscope. If no pattern can be obtained, move the detector probe to the control grid of each preceding stage until a pattern can be obtained. Peak the I.F. transformers concerned, until a response curve can be obtained at the output jack, J-2204.

(7) Always reduce the generator output to the minimum value required for an indication on the oscilloscope. Overloading the amplifiers will give a false indication of frequency response.

(8) The sketch below shows the idealized response curve desired.



(9) Peak T-2204, T-2205, T-2206 and T-2207, (lower slug) for maximum indication.

(10) Peak T-2204, T-2205, T-2206 and T-2207, (upper slug) for maximum indication.

(11) Connect the output of the sweep marker generator to either side of R-2209, the balance adjust pot. Tune the slug in T-2203 for maximum gain and best frequency response. It may be necessary to readjust other slugs to obtain the proper frequency response.

I.F. AMPLIFIERS: ALTERNATE ALIGNMENT:

(1) Remove the inputs at J-2202 and J-2203.

(2) Connect an RF signal generator set to 14.1 mcs at approximately 1 volt to either side of the balance adjust pot, R-2209.

(3) Connect the probe of a VTVM or oscilloscope set for maximum sensitivity to the output jack, J-2204. (70 ohm load if not connected to system).

(4) Tune T-2204, T-2205, T-2206 and T-2207, lower slugs, for maximum indication. Reduce the signal generator output as required, to prevent overloading.

(5) Tune the signal generator to 16.35 mcs.

(6) Peak the upper slug of T-2204, T-2205, T-2206 and T-2207 for maximum indication.

(7) Tune the signal generator to 15.25 mcs, and peak T-2203 for maximum indication.

(8) Repeat steps (2) through (6).

(9) Slowly sweep the signal generator frequency from 14.25 to 16.25 mcs, and note the output indication. Record the maximum amplitude, and label this the "zero db reference".

(10) Again sweep the signal generator slowly through the range 14.25 to 16.25 mcs. The indication should not fall below 70.7% of the zero db reference at any point.

(11) Balance 18Mc Balanced Modulator by turning Carrier "OFF" on CBE and connecting scope or VTVM to junction of Diodes CR-2201 and CR-2202 and adjusting R-2209 for minimum indication.

7. R.F. Circuits:

a) Refer to:

(1) Figure 2: Part 2, General Block Diagram.

(2) Alignment Instructions: R.F. Channel.

(3) Table 1: Frequency Chart.

(4) Figure III(A)-8-1b: schematic diagram, Frequency Amplifier Model CHG-2, Sheet 1 of 2.

b) The R.F. circuits consist of a balanced modulator stage (V-2704 and V-2705), three cascaded R.F. amplifier stages, and a metering circuit.

c) The instructor can best explain the circuitry of the RF section by going through the alignment procedure for the R.F. Channel. During this discussion, the following important points should be brought out:

(1) Four tank circuits are arranged between each of the RF stages; these are cut in or out by a four position switch, the positions 1 through 4 corresponding to the dial designations A through D. The output of the balanced modulator is applied to only three tanks, because the signal bypasses the balanced modulator on bandswitch position #1, Dial designation 0A.

(2) Care should be taken to point out the difference between "bandswitch position" and dial designation. For example, in the R.F. Channel alignment instructions, step 21, the order reads: "Set Bandswitch to position 6". This actually corresponds to Dial designation 10C.

(3) An RF gain control, R-2725, is adjustable from the front panel. This control is in the grid circuit of the 1st RF amplifier, V-2706.

(4) A portion of the output RF is sampled at J-2204, and is delivered to a simple meter-rectifier circuit; this provides front panel RF channel monitoring.

8. Regenerative Divider Circuits:

a) Refer to:

(1) Figure 1: Part 2 of General Block Diagram.

(2) Figure III(A)-8-1b: schematic diagram of Frequency Amplifier Model CHG-2, in technical manual.

b) The Regenerative Divider receives an accurate 1 mc signal from the 1 mc circuits, and converts this to an accurate 250 KC sub carrier, which is delivered to the Sideband Exciter, Model CBE.

c) V-2601 operates as a mixer tube. The 1 mc input is received from J-2601 at the control grid, pin #1. A 750 KC signal is received from the plate circuit of tripler V-2602A at grid 3, pin #7. The plate circuit is tuned to the difference frequency, 250 KCS.

d) The 250 KC output at the plate, pin #5 of V-2601 is delivered to the control grid of the output amplifier, V-2606B, whose plate is tuned to 250 KC. The 250 KC output is available at J-2706, for delivery to the Sideband Exciter, Model CBE. The 250 KC output of the mixer, V-2601, is also delivered to the control grid of tripler V-2602A.

e) Tripler V-2602A operates in the following manner:

When power is first applied, plate current in V-2602A commences to flow; this current contains noise at a large number of frequencies. Since the plate circuit is sharply tuned to 750 KCS, this will be the only noise component amplified. This initial 750 KC output of V-2602A is sufficient to mix with the 1 mc input in V-2601, to produce appreciable output in the plate circuit at 250 KCS. Subsequently, V-2602A operates as a tripler, receiving the 250 KC output of mixer V-2601, and tripling this to 750 KCS.

f) Alignment of the Regenerative Divider Circuits:

Tripler Circuit: (disconnect J-2601)

(1) Connect a signal generator set to 750 KC, at 0.2 volts, to pin #9 of V-2602A.

(2) Connect an oscilloscope to pin #1, (plate), of V-2602A. Controls should be set for observing a 750 KC signal.

(3) Tune L-2602 for maximum indication. (1.8V pp approx).

MIXER CIRCUIT:

(1) Connect a signal generator set to 250 KC, at 50 millivolts RMS, to input jack J-2601.

(2) Connect an oscilloscope to the plate, pin #5, of mixer V-2601. Set the controls to observe a 250 KC signal.

(3) Tune L-2601 for maximum indication. It should be approximately 3.3 volts peak to peak.

250 KC Amplifier Circuit:

(1) Connect the 1 mc input from the 1 mc circuits at J-2601.

(2) Connect a 68 ohm dummy load to J-2706.

(3) Connect an oscilloscope set up to observe a 250 KC signal to the dummy load.

(4) Peak L-2603 for maximum indication at 250 KCS.

Alignment of Frequency Amplifier Model CHG-2:

ONE MC STANDARD CIRCUITS:

1. Connect the output of the CSS-1 to J-2303.
2. Set selector switch, S-2301, to external standard position.
3. Connect AC VTVM to J-2305, or standoff.
4. Adjust L-2305 for maximum voltage output. (19 - 24 volts RMS)
5. Connect 70 ohm dummy load to J-2304.
6. Connect AC VTVM to dummy load at J-2304.
7. Peak L-2304 for maximum voltage output. (1.0 volt RMS or greater)
8. Set selector switch S-2301 to XTAL (internal).
9. Connect frequency counter to J-2304.
10. Adjust C-2307 for 1,000,000 cycles, plus or minus 1 cycle. VTVM should read 1.7 volts RMS or more.
11. Lock coils L-2304 and L-2305.
12. Return S-2301 to 1 mc external standard position.

SYNTHESIZER CHASSIS:

1. Set Band Switch to position OA.
2. Connect oscilloscope to Blue Dot, T-2501.
3. Disconnect P-2505 from J-2306.
4. Tune T-2501 for maximum 2 mc signal. It must be at least 120 volts, Pk-Pk. (42 volts RMS). Lock T-2501.
5. Reconnect P-2505 and J-2306.
6. Disconnect P-2504 from J-2305.
7. Connect oscilloscope to top of T-2502. (P-2503)
8. Connect signal generator at 18 mcs, .1 volt RMS, at P-2504.

9. Adjust T-2502 for maximum output, at 18 mcs, both primary and secondary. Lock both ends of T-2502. (1.2to3.0 volts Pk-Pk).

10. Disconnect the signal generator.

11. Connect oscilloscope to junction of R-2522 and R-2525; (green lead of T-2501 to terminal strip)

12. Set Band Switch to position 2.

13. Tune C-2501 and L-2502 for maximum 2 mc signal on the scope. Voltage should be 1.5 volts Pk-Pk or 0.5 volt RMS or greater.

14. Set Bandswitch to position 4; tune C-2503 for maximum 2 mc signal.

15. Set Bandswitch to position 6; tune C-2505 for maximum 2 mc signal.

16. Set Bandswitch to position 8; tune C-2512 for maximum 2 mc signal.

17. Set Bandswitch to position 14; tune C-2507 for maximum 2 mc signal.

18. Set Bandswitch to position 16; tune C-2515 for maximum 2 mc signal.

19. Set Bandswitch to position 18; tune C-2513 for maximum 2 mc signal.

20. Set Bandswitch to position 30; tune C-2510 for maximum 2 mc signal.

21. Reconnect P-2504 and J-2305.

22. Disconnect P-2505 and J-2306.

23. Measure the DC voltage at the junction of R-2526 and R-2527; it must be 4.0 volts or more. (this point is the black lead of T-2501)

24. Connect the DC voltmeter to the junction of R-2522 and R-2525; this is the green lead of T-2501.

25. Set the balance adjust, at the top of T-2501, for the same voltage obtained in step (24), above. Lock the adjustment.

26. Reconnect P-2505 and J-2306.

27. Disconnect all test equipment.

HIGH FREQUENCY INJECTION OSCILLATOR:

1. Set the oscilloscope on DC function, 0.1 Volts/cm deflection.

2. Connect scope probe to junction of R-2526 and R-2527; this is the black lead of T-2501.

3. Adjust vertical positioning control to center the trace at the center of the screen for reference.

4. Without touching oscilloscope controls, place scope probe at the junction of R-2525 and C-2541; this is the terminal strip below and right of T-2501; at the junction of the .01 uf capacitor, the 100 K ohm resistor and the cable.

5. Tune, as per the chart below, to the same horizontal reference line established in step (3), above. When audio oscillation appears, tune toward maximum amplitude until the oscillation disappears, then continue tuning trimmer till the trace appears at the center reference line previously established.

BANDSWITCH POSITION	ADJUST
2	C-2401
4	C-2403
6	C-2405
8	C-2411
14	C-2407
16	C-2415
18	C-2413
30	C-2409

6. Check the following Bandswitch positions; the horizontal line must still be in the center within plus or minus 0.25 volt.
0, 10, 12, 20, 22, 24, 26, and 28.

7. Disconnect the oscilloscope.

SYNC CIRCUIT INDICATOR:

1. Set Bandswitch to position 2.
2. Set C-2538 to just off full capacity.
3. Adjust potentiometer R-2520 fully CW; the sync light should go out.
4. Adjust R-2520 CCW, until the sync light just comes on.
5. Set Bandswitch to position 4; the light must go out between bands.
6. If light is off on position 4 of the Bandswitch, readjust R-2520 until the sync light just comes on.
7. Check all Bandswitch positions; the sync light must come on in all positions, and go off between all positions. Except between 0A and 2B.

HIGH FREQUENCY AMPLIFIER:

1. Connect VTVM (AC), or oscilloscope to the junction of C-2776 and C-2777.
2. Set trimmer C-2776 to approximately mid capacity.
3. Adjust according to the chart below. The output voltages must be at least 1.4 volts Pk-Pk or .5 volt RMS.

BAND SWITCH	TUNE FOR MAXIMUM, THEN LOCK
2	L-2737, L-2738
4	L-2736
6	L-2735
8	L-2734
10	L-2733
12	L-2732
14	L-2731
16	L-2730
18	L-2723
20	L-2724
22	L-2725
24	L-2726
26	L-2727
28	L-2728
30	L-2729

MID FREQUENCY CHANNEL: (Disconnect J-2701 and J-2703)

1. Connect a signal generator to J-2702 at 1.75 mcs, 1.0 volt RMS.
2. Set MF Tuning control to 1.75 mcs.
3. Tune T-2702, L-2703, L-2705 and T-2703 for maximum indication on MF meter.
4. Set signal generator to 3.75 mcs; set MF Tuning to 3.75 mcs.
5. Tune C-2710, C-2712, C-2717 and C-2718 for maximum indication on MF meter.
6. Repeat steps (2,3) and (4,5) until no further peaking can be done.
7. Lock the coils peaked in the preceding steps.
8. Set signal generator to 1.75 mcs; set MF Tuning to 1.75 mcs. Adjust Balance Pot R-2703 for a dip and lock the pot.
9. Connect a signal generator at 250 KC to J-2701.
10. Connect a signal generator at 2 mcs to J-2702.
11. Set MF tuning to 1.75 mcs.
12. Tune T-2701 for maximum indication on MF meter.
13. Set the signal generator connected to J-2702 to 4 mcs.
14. Set the MF tuning control to 3.75 mcs. The MF meter should peak at this point.
15. Lock T-2701.

R.F. CHANNEL:

1. Connect 75 ohm dummy load at J-2704.

2. Set trimmers C-2735, C-2736, C-2737, C-2745, C-2746, C-2747, C-2748, C-2755, C-2756, C-2757, C-2758, C-2769, C-2770, C-2771 and C-2772 to mid capacity.

3. Turn balance adjust pot R-2722 fully clockwise.

4. Turn B PLUS switch to ON.

5. Set Bandswitch to "O" position.

6. Set dial reading to 1.75 mcs.

7. Connect signal generator to balanced modulators V-2704 and V-2705 through C-2729. Set the signal generator to 1.75 mcs, at about 0.1 volt.

8. Adjust T-2718, T-2710 and T-2714 for maximum indication on RF output meter.

9. Set the dial reading to 3.75 mcs.

10. Set the signal generator to 3.75 mcs.

11. Adjust C-2772, C-2758, and C-2748 for maximum indication on the RF output meter.

12. Repeat steps (6) through (11) until no further adjustments are necessary, and lock the coils.

13. Set the Bandswitch to position "2".

14. Set the signal generator to 3.75 mcs.

15. Set the dial reading to 3.75 mcs on Band "B".

16. Tune T-2717, T-2713, T-2709 and T-2706 for peak RF output meter reading.

17. Set signal generator to 7.75 mcs.

18. Set dial reading to 7.75 mcs, Band "B".

19. Tune C-2771, C-2757, C-2747, and C-2737 for meter peak.

20. Repeat steps (14) through (19) until no further adjustments are necessary. Lock the coils.

21. Set Bandswitch to position "6".

22. Set signal generator to 7.75 mcs.

23. Set dial reading to 7.75 mcs, on Band "C".

24. Tune T-2716, T-2712, T-2708 and T-2705 for peak.

25. Set signal generator to 15.75 mcs.

26. Set dial reading to 15.75 mcs, on Band "C".

27. Tune C-2770, C-2756, C-2746 and C-2736 for peak.

28. Repeat steps (22) through (27) until no further adjustment is necessary. Lock the coils.

29. Set Bandswitch to "20" position.

30. Set signal generator to 15.75 mcs.

31. Set tuning dial to 15.75 mcs, on Band "D".

32. Tune T-2715, T-2711, T-2707 and T-2704 for peak.

33. Set signal generator to 33.75 mcs.

34. Set tuning dial to 33.75 mcs. on Band "D".

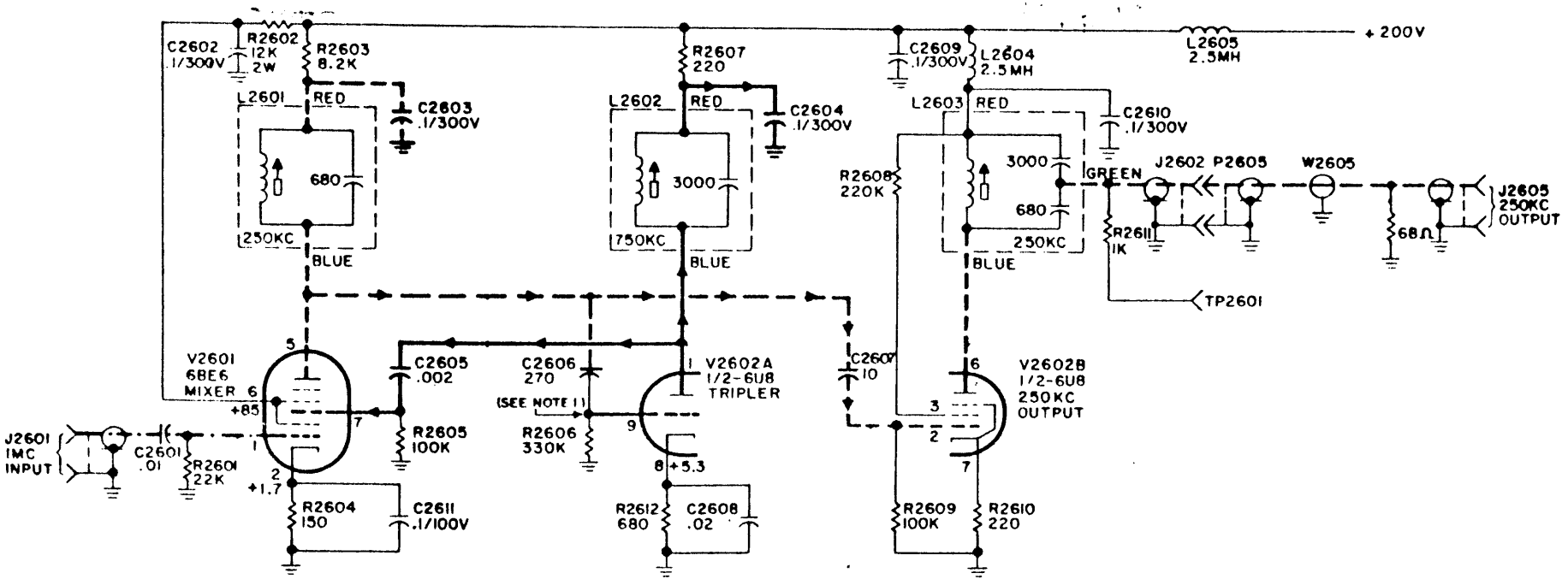
35. Tune C-2769, C-2755, C-2745 and C-2735 for peak.

36. Repeat steps (30) through (35) until no further adjustments are necessary. Lock the coils.

High Frequency Balanced Modulator

1. Turn Band switch to 20D, disconnect J-2701, tune the RF dial to 20 Mc(max. indication), adjust the output control as needed to maintain a output for adjusting balance.
2. Adjust R-2722 (HF balance) for minimum indication on the output meter.

3. Reconnect J-2701.



LEGEND
250KC SIGNAL PATH
750KC SIGNAL PATH
1000KC SIGNAL PATH

NOTES

1. INITIAL INPUT TO V2602A IS NOISE SPECTRUM, SUBSEQUENTLY BY REGENERATIVE INPUT IS 250KC AND V2602A AMPLIFIES THIRD HARMONIC (750 KC).

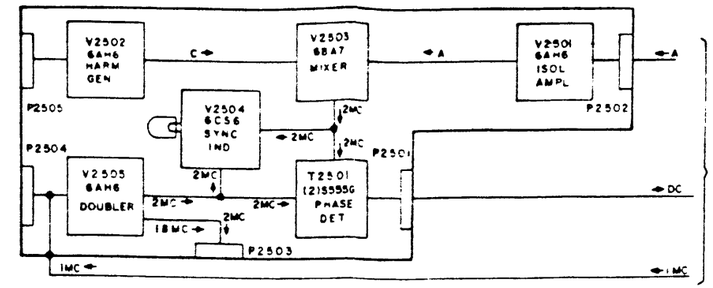
Figure III(A)-4-1b. Schematic Diagram, Regenerative Divider of CHG-2

LEGEND

——— SOLID-1-MC OR HARMONICS OF 1-MC STD (C-MC)
– – – – DOTTED-HFO INPUT (A-MC)
—·—·— DOT/DASH, 2ND HARMONIC OF 1-MC STD
—··—·· DOUBLE DOT/DASH (DC OUTPUT OF PHASE DETECTION)
-x-x-x- 2 MC DIFFERENCE OF A-MC (– – –) AND C-MC (———) SIGNALS

NOTE:
UNLESS OTHERWISE SPECIFIED ALL RESISTANCE VALUES ARE IN OHMS, 1/2 WATT, ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS AND ALL INDUCTANCE VALUES ARE IN MICROHENRIES.

BLOCK DIAGRAM OF SYNTHESIZER



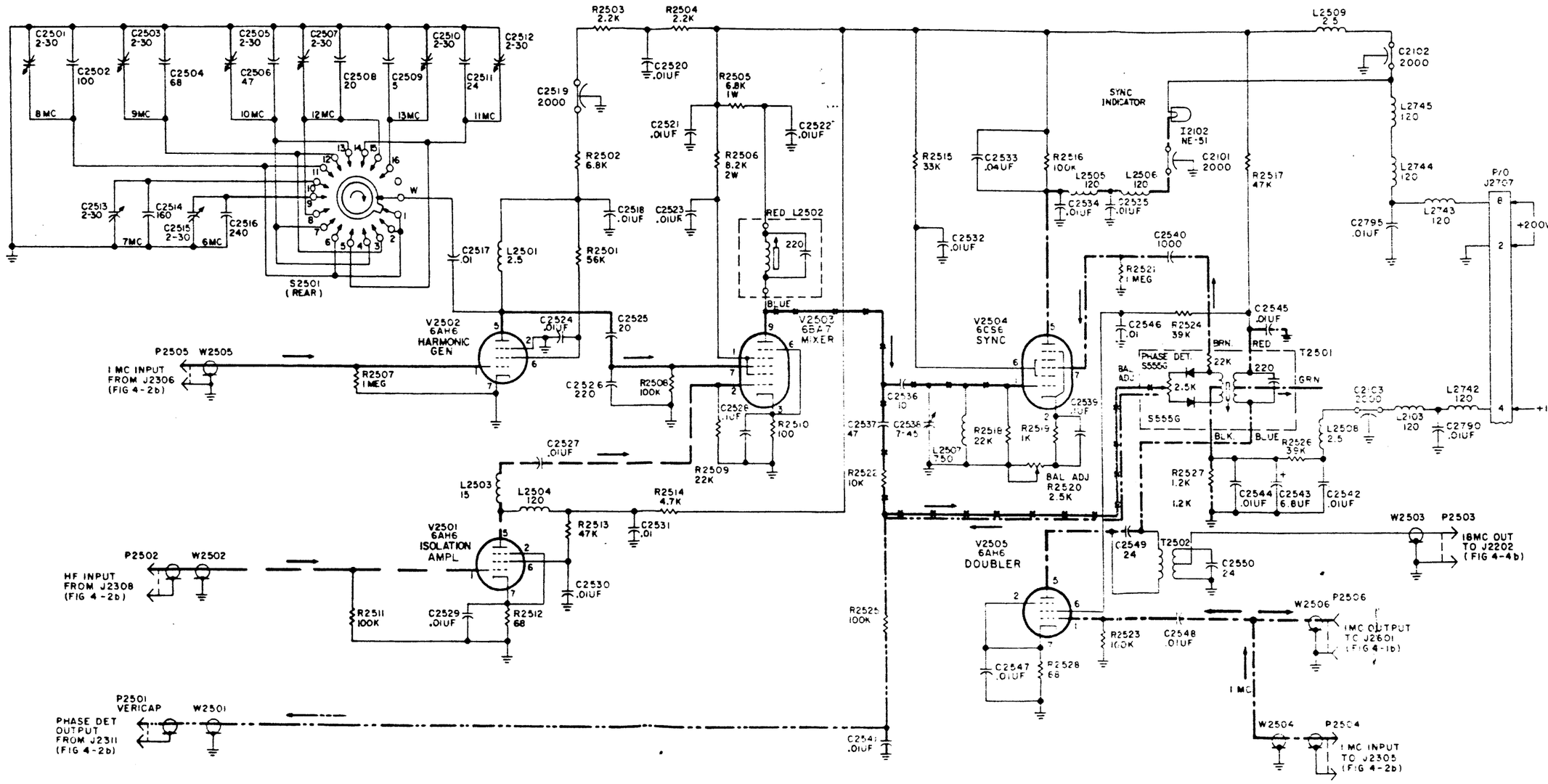
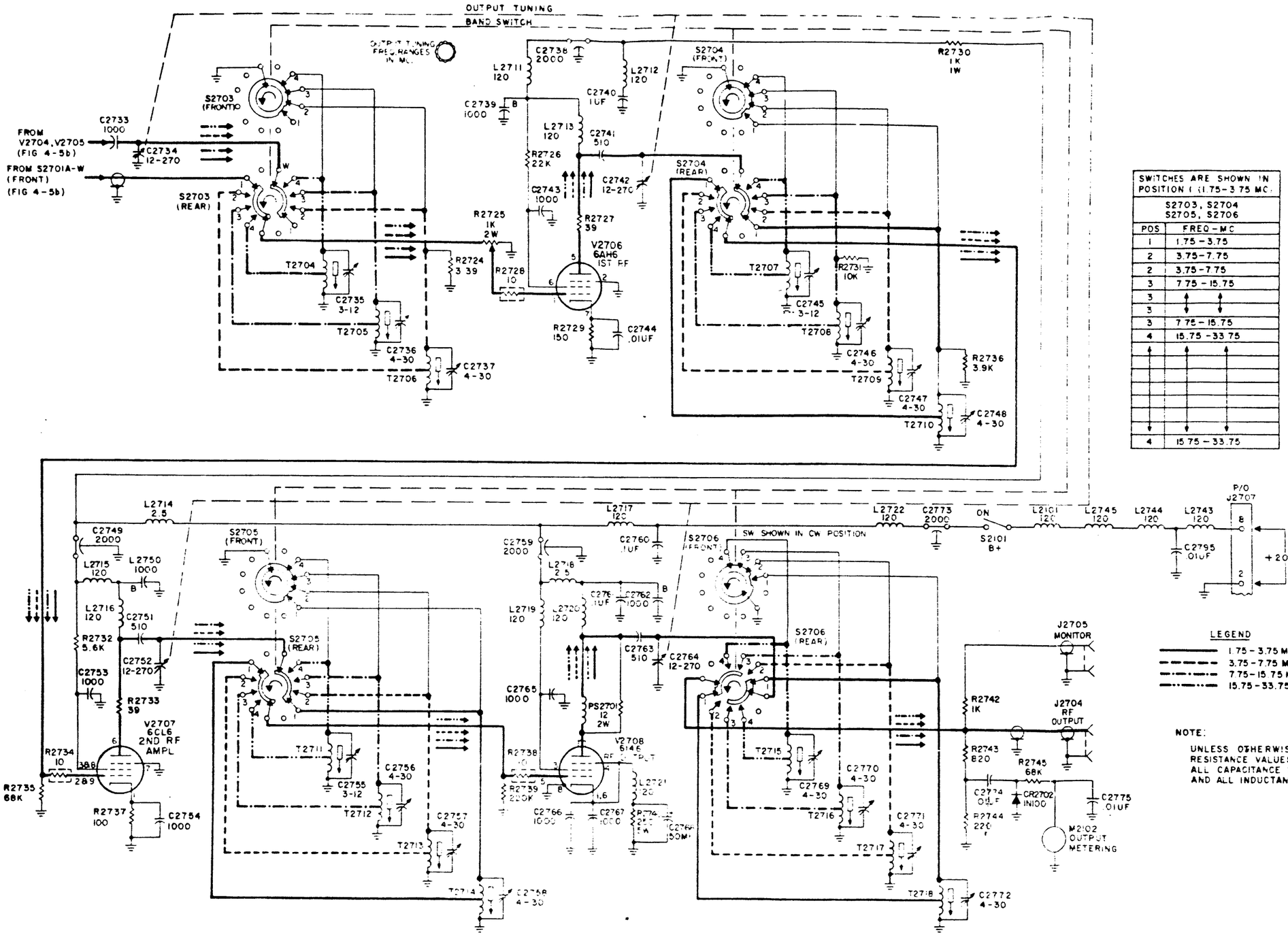


Figure III(A)-4-3b. Schematic Diagram, Synthesizer of CHG-2



SWITCHES ARE SHOWN IN POSITION 1 (1.75-3.75 MC.	
S2703, S2704 S2705, S2706	
POS	FREQ - MC
1	1.75 - 3.75
2	3.75 - 7.75
2	3.75 - 7.75
3	7.75 - 15.75
3	↕ ↕
3	↕ ↕
3	7.75 - 15.75
4	15.75 - 33.75
↕	↕ ↕ ↕
4	15.75 - 33.75

NOTE:

UNLESS OTHERWISE SPECIFIED ALL RESISTANCE VALUES ARE IN OHMS, 1/2 WATT, ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS AND ALL INDUCTANCE VALUES ARE IN MICROHENRIES.

Figure III(A)-4-6b. Schematic Diagram, RF Deck of CHG-2

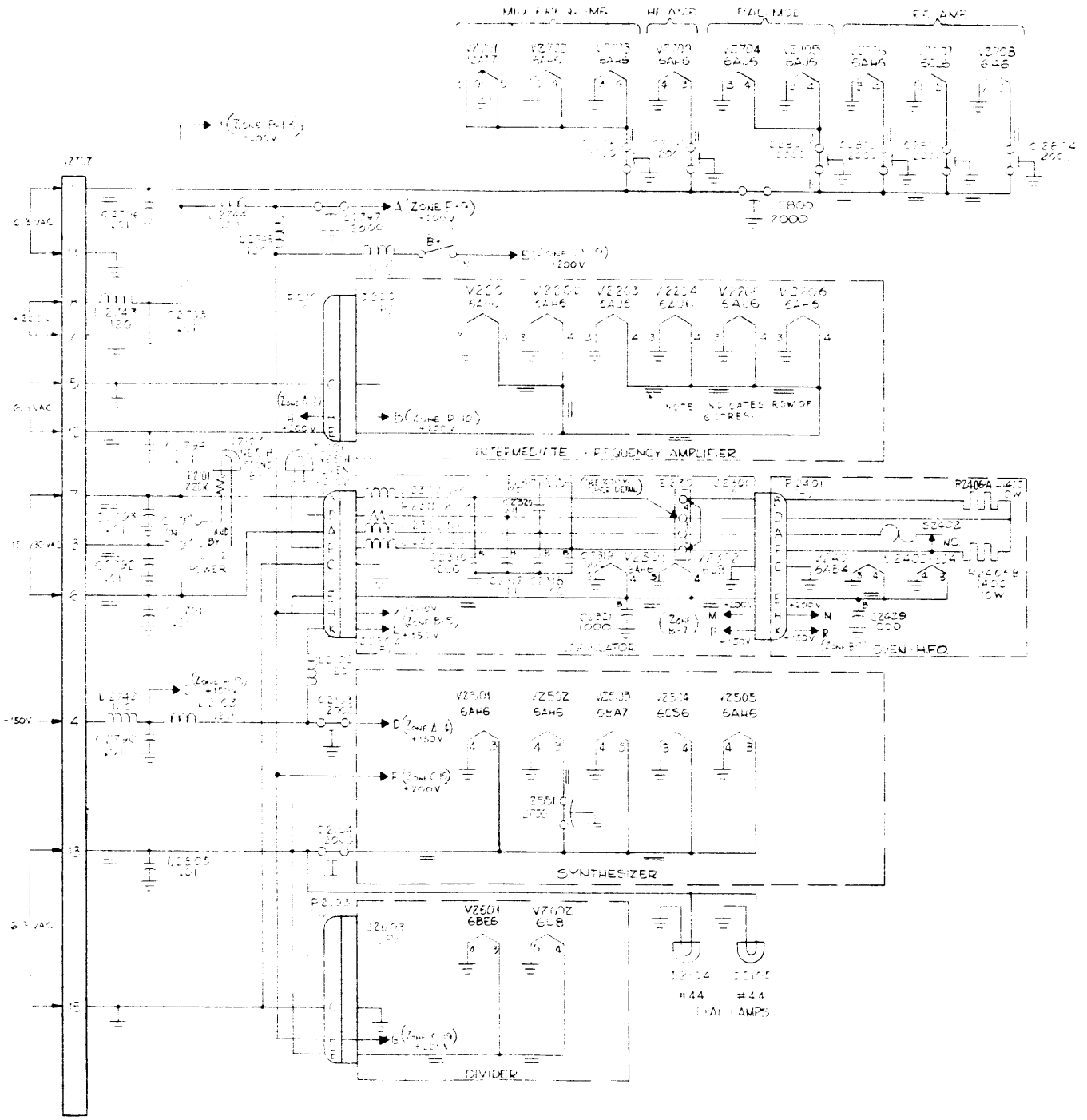
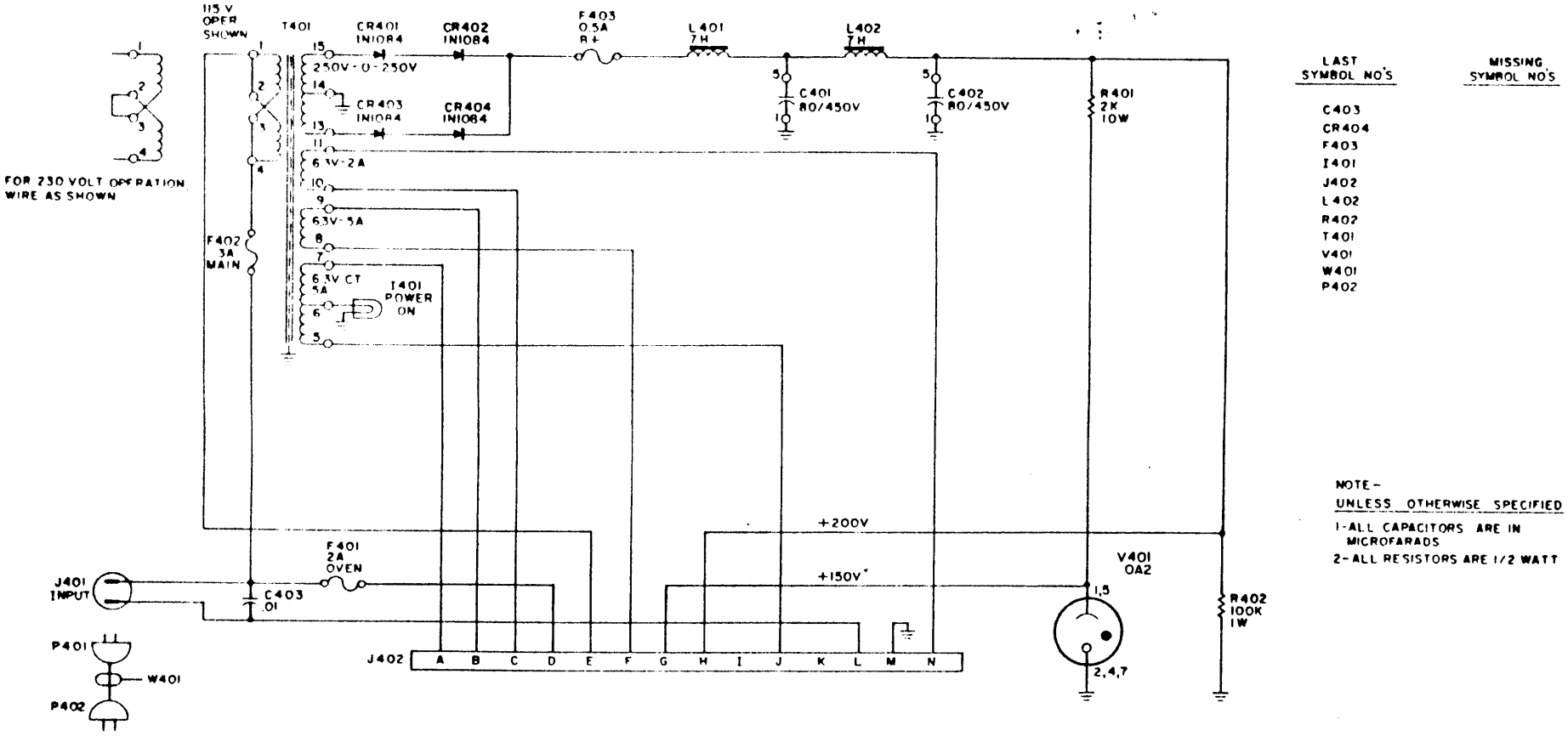


Figure III(A)-8-1b. Schematic Diagram, Frequency Amplifier, CHG-2 (Sheet 2 of 2)



LAST SYMBOL NO'S	MISSING SYMBOL NO'S
C403	
CR404	
F403	
I401	
J402	
L402	
R402	
T401	
V401	
W401	
P402	

NOTE-
UNLESS OTHERWISE SPECIFIED
1-ALL CAPACITORS ARE IN MICROFARADS
2-ALL RESISTORS ARE 1/2 WATT

Figure III(A)-8-2a. Schematic Diagram, Power Supply, CPP-1

FOR 230V OPERATION OF T401

1 - REMOVE JUMPERS MARKED *** FROM TERMINALS 1,2 & 3,4.

2 - ADD JUMPER MARKED - - - BETWEEN TERMINALS 2 & 3.

FOR 50~ OPERATION OF T401

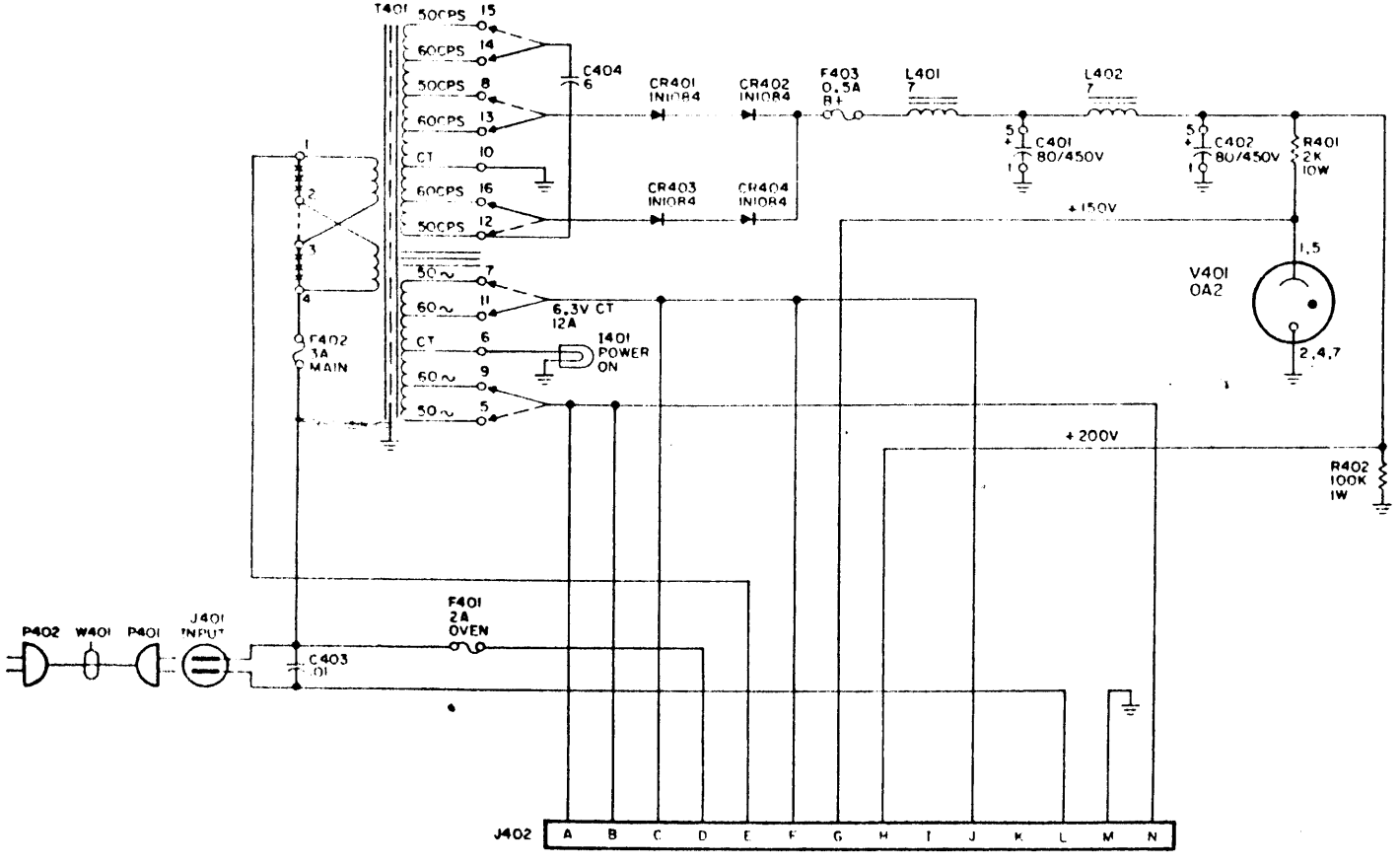
1 - REMOVE LEAD FROM TERMINAL 14 AND CONNECT IT ON TERMINAL 15.

2 - " " " " 13 " " " " " 8.

3 - " " " " 16 " " " " " 12.

4 - " " " " 11 " " " " " 7.

5 - " " " " 9 " " " " " 5.



UNLESS OTHERWISE SPECIFIED

ALL CAPACITORS ARE IN MICROFARADS.
ALL RESISTORS ARE 1/2 WATT.
ALL COILS ARE IN HENRIES.

LAST SYMBOLS	MISSING SYMBOLS
C404	
CR404	
F403	
I401	
J402	
L402	
P402	
R402	
T401	
V401	
W401	

Figure III(A)-8-2b. Schematic Diagram, Power Supply, CPP-5

SECTION 8

Title: Operation of the Synthesized Sideband Generator System

Objectives:

a) To discuss the operation of the Synthesized Sideband Generator system. It is assumed that the individual units making up the system have been studied.

b) To trace out the three signal paths in the 16 positions of the Bandswitch on Frequency Amplifier CHG-2.

c) To discuss sideband inversions and frequency translations occuring in the system.

d) To enumerate the steps required to tune the system to any given RF output frequency.

e) To correlate information already disseminated on the individual units.

References:

a) All lesson plans on the individual units comprising the system.

b) Complete schematic, Frequency Amplifier Model CHG-2.

c) Technical Manual, Sideband Generator Model SBG-1 or 2.

Training Aids:

a) Complete synthesized sideband generator system, set up for operation.

b) Two tone generator, or audio source.

c) Panalyzer, Model AN/GRM-33.

d) 70 ohm dummy load for Frequency Amplifier Model CHG-2.

Introduction:

In order to intelligently service the Synthesized Sideband Generator system, it is important that servicing personnel understand the operation of the system, and be aware of its capabilities and limitations. This lesson plan will attempt to correlate information already presented on individual units with information on tuning, translations, inversions and signal paths. Servicing personnel will then be armed with sufficient background information to pinpoint many difficulties using front panel indications.

Presentation:

A. General Discussion of the Three Signal Paths in the CHG-2 system.

1. The following figures are included:

a) Figure 1 shows a block diagram of the Sideband Exciter and Mid Frequency circuits of the CBE and CHG-2, respectively.

b) Figure 2 shows a block diagram of the signal path from Mid Frequency circuits to the first RF amplifier circuit.
Bandswitch position 1, Dial designation OA.

c) Figure 3 shows a block diagram of the signal path from the Mid Frequency circuits, through the I.F. circuits, to the balanced modulator circuit of the R.F. section. Bandswitch positions 2,3,4 and 5, Dial designations 2B, 4B, 6C and 8C.

d) Figure 4 shows a block diagram of the signal path from the Medium Frequency circuits to the balanced modulator circuit of the R.F. section.
Bandswitch positions 6 through 16, Dial designations 10C through 30D.

2. As noted previously, the upper sideband filter in the CBE filters out the UPPER sideband, and the lower sideband filter filters out the LOWER sideband. This causes sideband inversion at the output of the CBE. This is a deliberate inversion, made necessary by the configuration of the circuits that follow. The circuits that follow may contain an odd number of inversions, or they may be tuned to "sum" frequencies instead of the usual "difference" frequency tuning. In any event, the final RF output of the CHG-2 is not inverted.

3. The output of the Model CBE is an inverted sideband signal at a nominal frequency of 250 KCS, with the degree of carrier insertion controlled by R-236, the "Carrier Insert" control on the front panel of the CBE.

Block Diagram of Signal Path from Sideband Exciter Input to Output of Mid Frequency Amplifier:

FIGURE 1

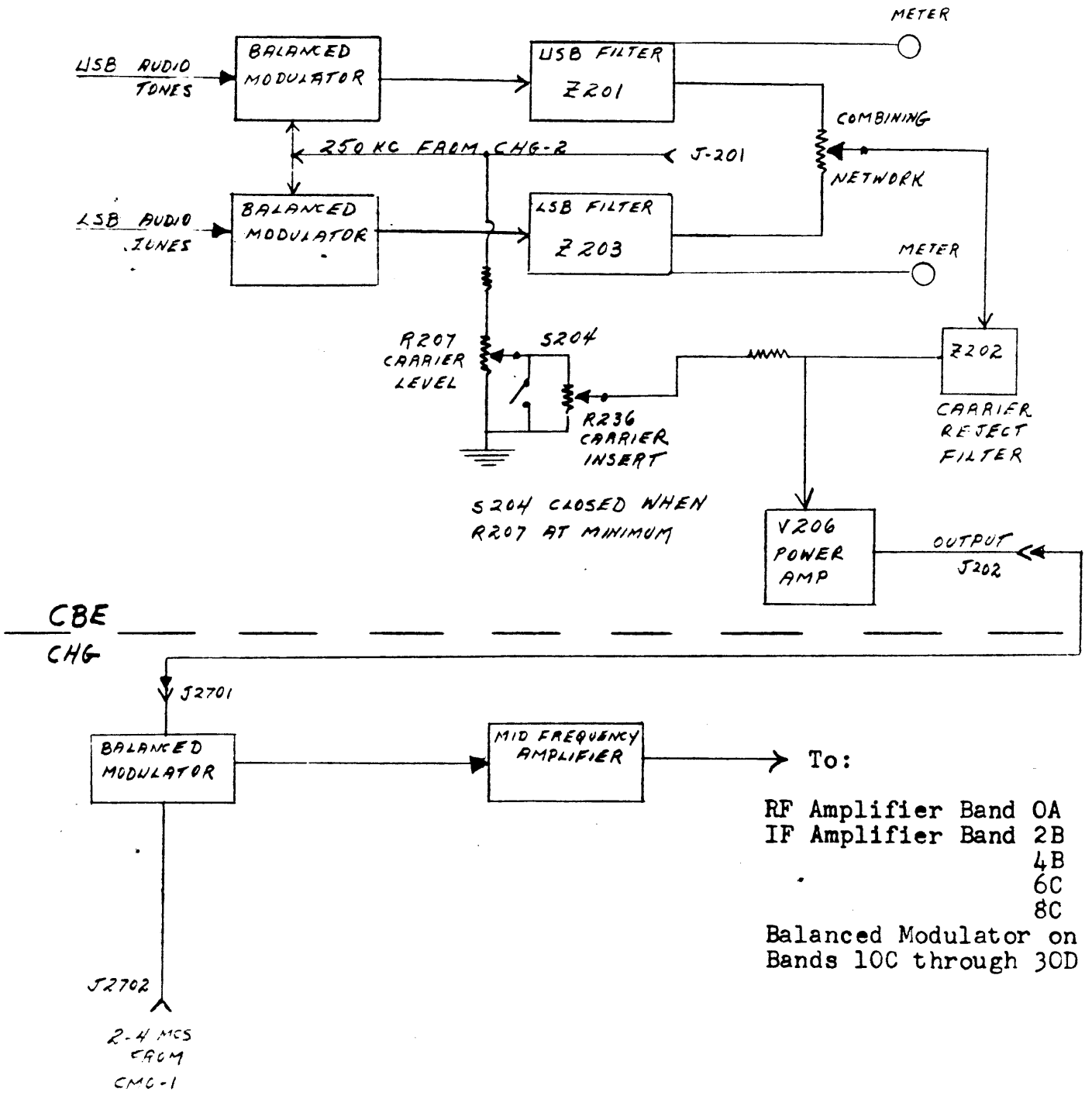
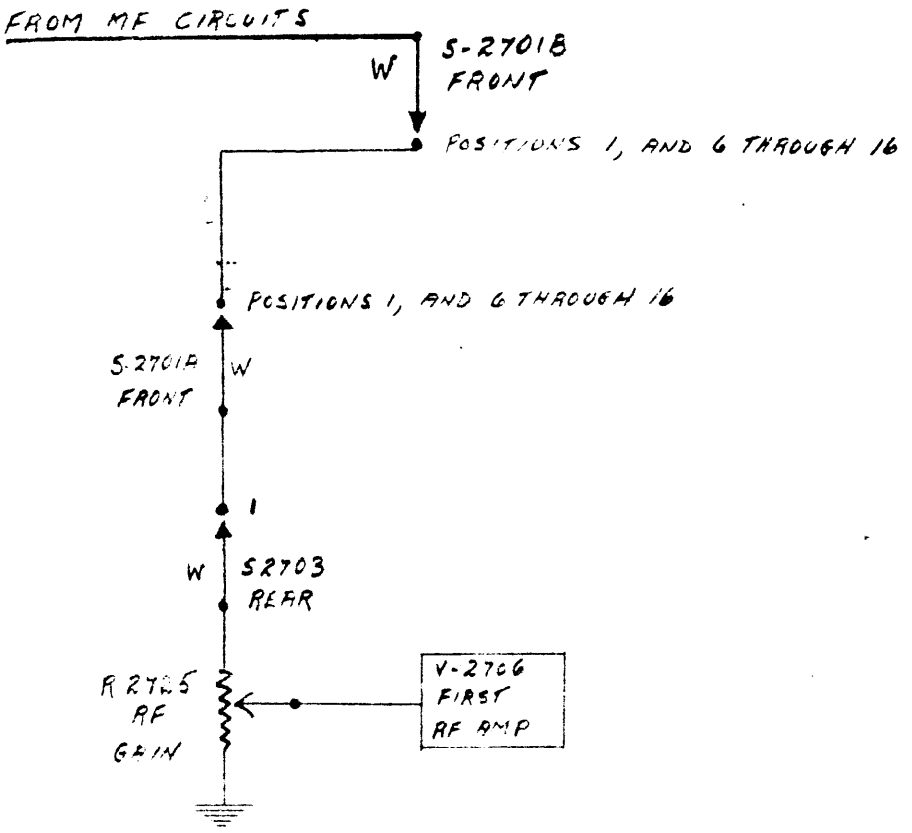


Figure 2

Block Diagram of Signal Path from Output of Mid Frequency Circuits to R.F. Circuits on Bandswitch Position #1, Dial Designation OA:

Final Balanced Modulator output is disabled by S-2703 (rear), only in position #1.



Block Diagram of Signal Path from Output of Mid Frequency Circuits to R.F. Amplifiers:

Bandswitch Position	Dial Designation	R.F. Injection
2	2B	20 mcs
3	4B	22 mcs
4	6C	24 mcs
5	8C	26 mcs

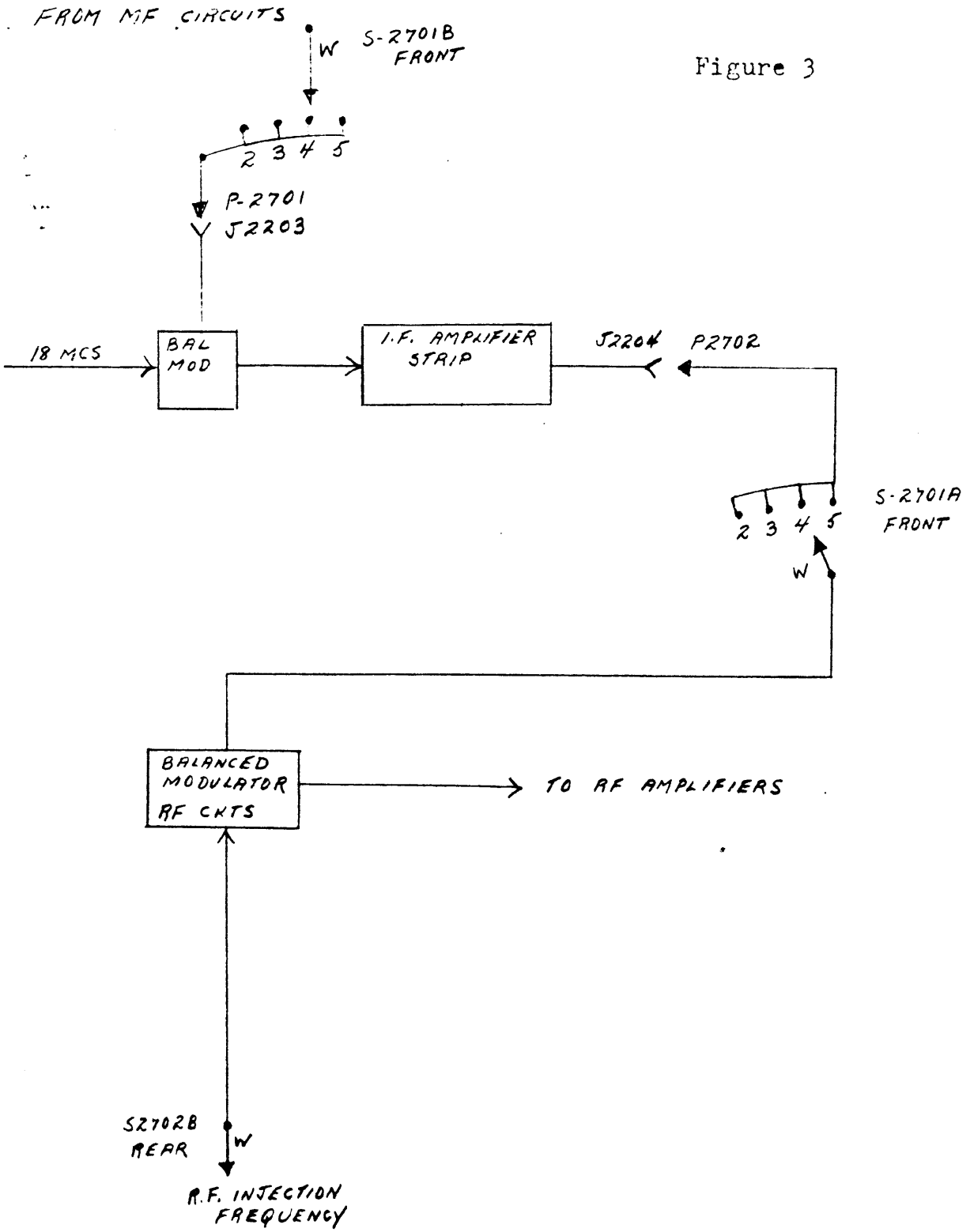
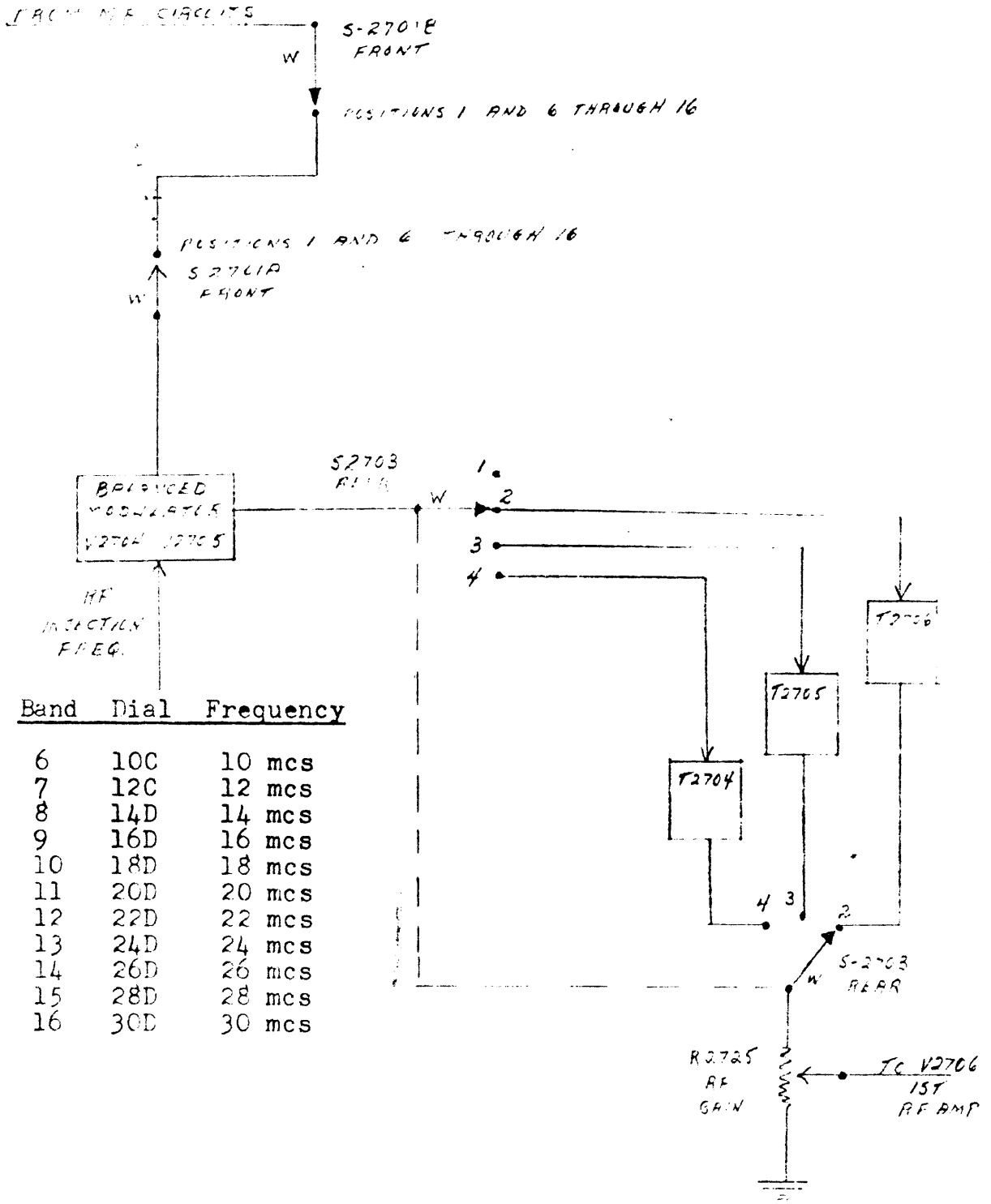


Figure 3

Block Diagram of Signal Path from Output of Mid Frequency Circuits to R.F. Amplifiers in Bandswitch Positions 6 through 16, corresponding to Dial Designations 10C through 30D.

Figure 4



Band	Dial	Frequency
6	10C	10 mcs
7	12C	12 mcs
8	14D	14 mcs
9	16D	16 mcs
10	18D	18 mcs
11	20D	20 mcs
12	22D	22 mcs
13	24D	24 mcs
14	26D	26 mcs
15	28D	28 mcs
16	30D	30 mcs

4. The Sideband Exciter output is fed to a balanced modulator in the Mid Frequency circuits of the Model CHG-2. The second input to this balanced modulator is the output of Controlled Master Oscillator, Model CMO-1, in the range 2 to 4 mcs. The CMO-1 output may be synthesized in 100 cycle steps, or it may be continuous without synthesization. The tuning controls and counter of the CMO-1 are calibrated 250 KCS below the actual CMO-1 output frequency.

5. The Mid Frequency amplifier circuits are tuned to the difference frequencies. Thus, the output of the Mid Frequency circuits is always in the range 1.75 to 3.75 mcs, regardless of the position of the bandswitch in the CHG-2.

6. The Mid Frequency, and CMO-1 Dial-Counter setting, is derived, in EVERY CASE, as follows:

   SUBTRACT THE DIAL NUMERIC OF THE CHG DIAL FROM THE DESIRED RF OUTPUT FREQUENCY OF THE CHG TO OBTAIN THE MID FREQUENCY. THIS IS ALSO THE DIAL - COUNTER SETTING OF THE CMO-1.

7. Thus, by offsetting the tuning controls of the CMO-1 by 250 KCS, one step in determining control settings is eliminated. This reduces the chances of tuning the system to an incorrect frequency.

8. The following examples, one taken from each of the three different signal paths in the system, will serve to illustrate the foregoing.

   Example #1: The RF output frequency desired is 2.45 mcs.

   For an output frequency in this range, the CHG-2 bandswitch is set to position 1, corresponding to a Dial designation of OA. The CHG-2 tuning dial is set to 2.45 mcs, Band A.
   Since, on Band OA, the output of the Mid Frequency circuits is fed directly to the RF amplifiers, the RF output frequency is also the Mid Frequency.

Mid Frequency:	2.45 mcs.
CBE Frequency:	.25 mcs.
CMO-1 Frequency:	2.70 mcs.
CMO-1 Counter:	2.45 mcs.

Apply the Rule:	R.F. Output Frequency:	2.45 mc
	minus Dial Numeric	0
	CMO-1 Counter and Mid Frequency	2.45 mc

Example #2: The RF output frequency desired is 5.63 mcs.

For an RF output frequency in this range, the CHG-2 bandswitch is placed in position 2, corresponding to a Dial designation of 2B. The CHG-2 tuning dial is set to 5.63 mcs, Band B.

The RF injection frequency to the final balanced modulator is 20 mcs.

The RF amplifiers following the balanced modulator are tuned to the difference frequencies; therefore, the I.F. input to the final balanced modulator must be 20.000 mc minus 5.630 mcs, or 14.370 mcs.

The Mid Frequency must be 18.000 mc minus 14.370 mcs, since the Mid Frequency beats with 18 mcs in the balanced modulator of the I.F. system, and the I.F. circuits are tuned to the difference frequency.

I.F. injection frequency	18.000 mcs.
I.F. Frequency	- 14.370 mcs.
Mid Frequency	3.630 mcs.

To produce a Mid Frequency of 3.630 mcs, the CMO-1 frequency must be 250 KC above the Mid Frequency, or: 3.880 mcs.

Since the Dial-Counter of the CMO-1 are set 250 KCS below the actual CMO-1 frequency, the CMO-1 dial and counter will read 3.630 mcs.

Apply the Rule:

R.F. Output Frequency	5.630 mcs.
CHG-2 Dial Numeric	- 2.000
CMO-1 Counter and Mid Frequency	3.630 mcs.

Example #3: The RF output frequency desired is 12.000 mcs. For an RF output frequency in this range, the CHG-2 bandswitch is placed in position 6, corresponding to a Dial designation of 10C. The CHG-2 tuning dial is set to 12.000 mcs, Band C.

The RF injection frequency to the final balanced modulator is 10 mcs.

From this point on, for the remaining positions of the CHG-2 bandswitch, the RF circuits are tuned to the SUM frequencies.

The Mid Frequency must be 12.000 mc minus 10.000 mcs, or 2.000 mcs.

The actual CMO-1 output frequency must be 2.250 mcs, and the CMO-1 Dial - Counter must read 2.000 mcs.

Apply the Rule:

R.F. Output Frequency:	12.000 mcs.
CHG-2 Dial Numeric	- 10.000 mcs.
CMO-1 Dial-Counter, and Mid Freq.	2.000 mcs.

9. On Band OA, the inverted CBE output mixes in the Medium Frequency balanced modulator, which inverts the signal again. This normally dispersed signal is fed direct to the RF amplifiers. Thus, the final RF output on Band OA is not inverted.

10. On Bands 2B, 4B, 6C and 8C, the CBE output, an inverted signal, mixes in the Medium Frequency balanced modulator, which inverts the signal again. This normally dispersed signal is fed to the balanced modulator in the IF circuits, which again inverts the signal. The output of the I.F. circuits is fed to the final balanced modulator which again inverts, causing the output signal to be normally displaced in the frequency spectrum.

11. On Bands 10C through 30D, the inverted CBE output mixes in the Medium Frequency Balanced modulator, which again inverts the signal. This normally dispersed signal is fed to the final balanced modulator. The RF circuits are now tuned to the SUM frequencies, and no inversion takes place.

3. Steps Required to Tune the Synthesized Sideband Generator System to any RF Output Frequency, with Carrier Only.

Refer to Figure I-3-1, pages 3-7 and 3-8 of the Technical Manual for SBG-1 and 2.

1. Place the STANDBY - ON switch (45) on the CSS-1 to the ON position. This energizes the circuits of the Primary Frequency Standard.

2. Place the STANDBY - POWER switch (63) on Model CPP-2 power supply to the POWER position. After a 60 second time delay, this unit furnishes power to the CHL-1, the CMO-1 and the CLL-1 units.

3. While waiting for the 60 second delay, adjust the CBE controls as follows:

   a) Set Channel 1 and Channel 2 selector switches, (6) and (10), to the OFF position.

   b) Place USB and LSB gain controls, (7) and (9), to the extreme CCW position.

   c) Place the ON - OFF switch, (11), to the ON position.

   d) Set the Carrier Level Control, (8), to the 0 db position.

   The CBE is now set up to deliver a 250 KC subcarrier to the Mid Frequency Circuits of the CHG-2. Since the initial tuning is always accomplished with carrier only, the audio circuits have been disabled.

4. Adjust the CHG-2 controls as follows:

   a) Turn the POWER switch, (14), to ON.

   b) Leave the B PLUS switch, (16), in the OFF position.

   c) Set the Bandswitch, (22), to the appropriate position in accordance with the RF output frequency desired. The frequency range and Dial Numeric will appear in the MCS window, (21), above the bandswitch control.

   d) Set the Output Tuning Control, (23), to the RF output frequency desired on MCS dial, (18).

   e) Subtract the Dial Numeric from the RF output frequency. The result is the Mid Frequency and the CMO-1 Dial and Counter setting. Note this figure carefully.

   f) Set the pointer of the MF Tuning control, (24), to the MF setting determined in the step above.

g) Turn the RF Output control, (25) to the Minimum position.

h) Determine that a 70 ohm dummy load is connected to the RF output jack of the CHG-2, at J-27C4.

5. After the 60 second time delay, turn the CLL-1 monitor scope selector switch, (40), through positions L-1, L-2 and L-3 and observe that a stationary rectangle appears on the monitor scope, (39), in all positions. Return the selector switch to the L-3 position. Move the KILOCYCLES control, (38), and the HUNDREDS control, (41), through their ten positions and observe that the rectangle remains stationary.

6. Set the KILOCYCLES control and the HUNDREDS control to the positions corresponding to the kilocycles and hundreds digits of the Mid Frequency and CMO-1 counter reading previously determined.
For example:
If the CMO-1 counter reading determined in step 4e is 2652.000 mcs, set the KCS and HUNDREDS controls to positions 2,0.

7. Adjust the CMO-1 controls as follows:

a) Place the OPERATE - CAL switch, (29), in the CAL position.

b) Unlock the counter knob, (35), with the locking knob, (37).

c) Set the CMO-1 counters to a reading 50 KCS below the counter reading determined in step 4e. Approach this setting from a lower frequency.

d) Unlock knob (32a), and adjust calibration knob (32b) for a zero beat indication on Calibration Beat indicator (28). Lock knob (32a).

e) Carefully turn the counter knob, (35), to the setting previously determined in step 4e. Lock the Counter knob.

f) Turn the Output Control knob, (36), to mid position.

g) Adjust the Tuning KCS control, (33), for maximum indication on the TUNE FOR MAX meter, (30).

h) Adjust the Output control knob, (36), until the indication on the TUNE FOR MAX meter reaches approx. 3 on scale.