TECHNICAL MANUAL

for

RADIO RECEIVING SET

AN/FRR-85(V)1

THE TECHNICAL MATERIEL CORPORATION
MAMARONECK, N.Y. OTTAWA, CANADA

TECHNICAL MANUAL

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NOTICE

THE TECHNICAL MATERIEL CORPORATION
COMMUNICATIONS ENGINEERS
700 FENIMORE ROAD MAMARONECK, N. Y.

Warranty

The Technical Materiel Corporation, hereinafter referred to as TMC, warrants the equipment (except electron tubes,* fuses, lamps, batteries and articles made of glass or other fragile or other expendable materials) purchased hereunder to be free from defect in materials and workmanship under normal use and service, when used for the purposes for which the same is designed, for a period of one year from the date of delivery F.O.B. factory. TMC further warrants that the equipment will perform in a manner equal to or better than published technical specifications as amended by any additions or corrections thereto accompanying the formal equipment offer.

TMC will replace or repair any such defective items, F.O.B. factory, which may fail within the stated warranty period, PROVIDED:

1. That any claim of defect under this warranty is made within sixty (60) days after discovery thereof and that inspection by TMC, if required, indicates the validity of such claim to TMC's satisfaction.

2. That the defect is not the result of damage incurred in shipment from or to the factory.

3. That the equipment has not been altered in any way either as to design or use whether by replacement parts not supplied or approved by TMC, or otherwise.

4. That any equipment or accessories furnished but not manufactured by TMC, or not of TMC design shall be subject only to such adjustments as TMC may obtain from the supplier thereof.

Electron tubes*furnished by TMC, but manufactured by others, bear only the warranty given by such other manufacturers. Electron tube warranty claims should be made directly to the manufacturer of such tubes.

TMC's obligation under this warranty is limited to the repair or replacement of defective parts with the exceptions noted above.

At TMC's option any defective part or equipment which fails within the warranty period shall be returned to TMC's factory for inspection, properly packed with shipping charges prepaid. No parts or equipment shall be returned to TMC, unless a return authorization is issued by TMC.

No warranties, express or implied, other than those specifically set forth herein shall be applicable to any equipment manufactured or furnished by TMC and the foregoing warranty shall constitute the Buyers sole right and remedy. In no event does TMC assume any liability for consequential damages, or for loss, damage or expense directly or indirectly arising from the use of TMC Products, or any inability to use them either separately or in combination with other equipment or materials or from any other cause.

*Electron tubes also include semi-conductor devices.

PROCEDURE FOR RETURN OF MATERIAL OR EQUIPMENT

Should it be necessary to return equipment or material for repair or replacement, whether within warranty or otherwise, a return authorization must be obtained from TMC prior to shipment. The request for return authorization should include the following information:

1. Model Number of Equipment.
2. Serial Number of Equipment.
3. TMC Part Number.
4. Nature of defect or cause of failure.
5. The contract or purchase order under which equipment was delivered.

PROCEDURE FOR ORDERING REPLACEMENT PARTS

When ordering replacement parts, the following information must be included in the order as applicable:

1. Quantity Required.
2. TMC Part Number.
3. Equipment in which used by TMC or Military Model Number.
4. Brief Description of the Item.
5. The *Crystal Frequency* if the order includes crystals.

PROCEDURE IN THE EVENT OF DAMAGE INCURRED IN SHIPMENT

TMC's Warranty specifically excludes damage incurred in shipment to or from the factory. In the event equipment is received in damaged condition, the carrier should be notified immediately. Claims for such damage should be filed with the carrier involved and not with TMC.

All correspondence pertaining to Warranty Claims, return, repair, or replacement and all material or equipment returned for repair or replacement, within Warranty or otherwise, should be addressed as follows:

THE TECHNICAL MATERIEL CORPORATION
Engineering Services Department
700 Fenimore Road
Mamaroneck, New York

RECORD OF CORRECTIONS MADE

Change No.	Date of Change	Date Entered	Entered By

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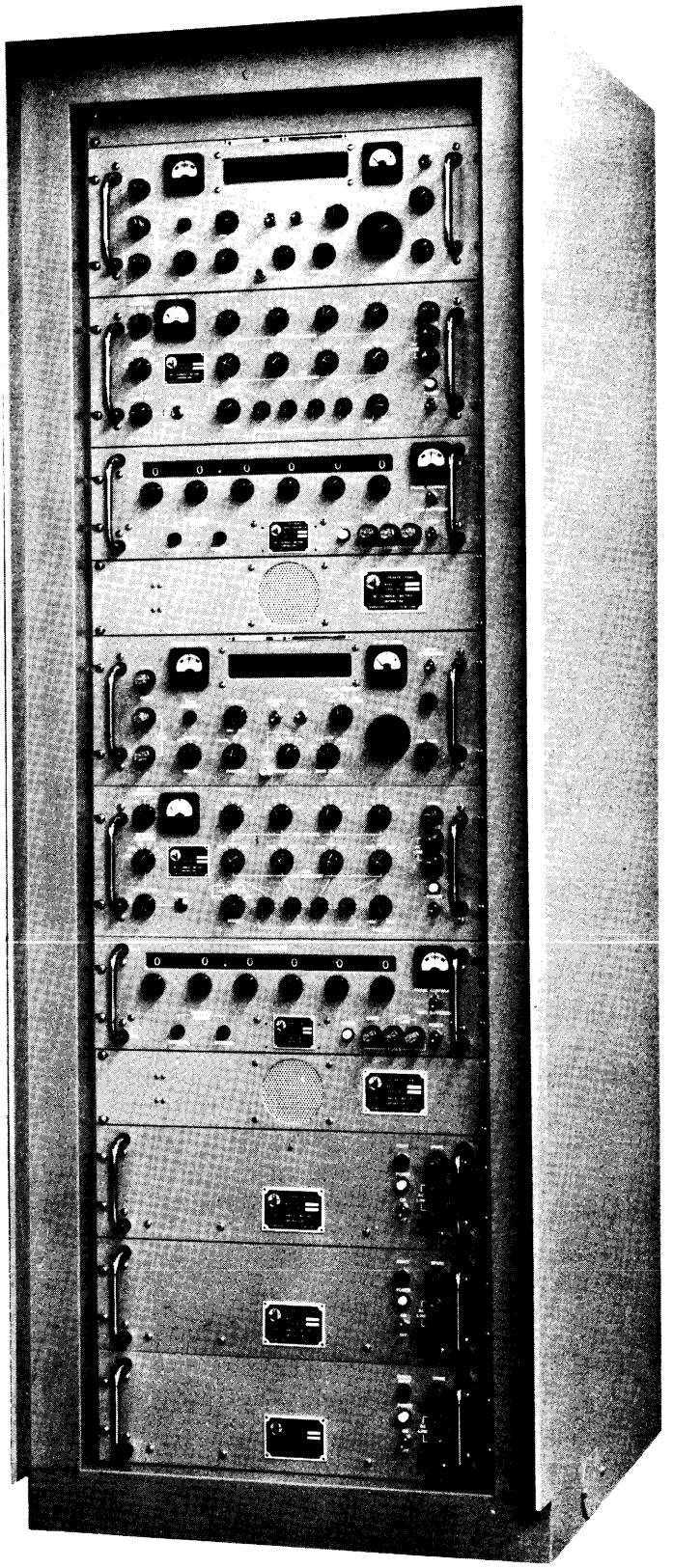


Figure 1-1. Radio Receiver Model AN/FRR-85(V)

SECTION 1
GENERAL INFORMATION

1-1. SCOPE

The context of this manual covers Radio Receiving Set AN/FRR-85(V)1. AN/FRR-85(V)1 is a dual receiver essentially consisting of two single receivers. Except as otherwise indicated, text in this manual refers to a single receiver.

1-2. GENERAL DESCRIPTION (see figure 1-1)

Each receiver is a superheterodyne independent sideband receiver, tunable through a 2-32 MHz frequency range; each receiver may be tuned manually or by teletype coded signal via conventional teletype linkage from a remote control station. Up to fifty receivers can be controlled individually from a single teletype channel. Reception is for four ISB (independent sideband) channels, consisting of 3.0-KHz direct (A1 and B1) and translated (A2 and B2) in the upper and lower sidebands (see figure 1-2). In lieu of sideband reception, the receiver includes a reception channel for a 2.5- or 6.0-KHz bandwidth, symmetrical about the carrier, for CW, MCW or AM transmissions (see figure 1-3). Controls for this channel include an adjustable (±3KHz) BFO for CW receptions.

Each of the four ISB channels may contain voice, a combination of voice frequency tone telegraph channels, FAX (facsimile) channels, data transmissions or any type of information that may be contained within 250-3,040 Hz (direct channels) and 350-3,040 Hz (translated channels).

There are three frequency stabilization control modes: (1) LOCAL (local oscillator), (2) SYNthesized and (3) AFC (automatic frequency control). The receiver may be set for any of the three in a manual tuning; in a remote tuning it may be set for SYNthesized mode; remote AFC operation is possible, when initially assisted by a local operator. LOCAL oscillator frequency control affords continuous tuning throughout the 2-32 MHz range with the frequency stability referenced to the local oscillator. In synthesized frequency control, tuning is accomplished in 100-Hz steps and the stability is maintained by locking to an internal 1-MHz frequency standard, stable to within one part in 1×10^8 per day; there is a connection for an external 1-MHz standard of higher stability if preferred, with automatic emergency switching between the two standards. An automatic frequency tuning section, working from digital information, speeds synthesized tuning in either manual or remote control. For relatively unstable transmissions with a partial carrier, the AFC circuitry locks to the carrier and corrects injection frequencies for the drifting signal.

Receiver gain may be controlled either manually (local operation only) or set up for AGC (automatic gain control; either local or remote operation). In AGC, feedback source and attack-and-decay time may be set individually for each channel. The AGC system maintains a constant* audio output level through an antenna input range of 1 uv to 1 volt.

The frequency for which the receiver is tuned is displayed in a six-digit (02.0000 to 32.0000) frequency counter on the front panel. This display represents an actual count of the receiver tuned frequency (as a function of local oscillator frequency) and is also referenced to the 1-MHz standard. A front panel jack and switch permits use of the counter for measuring an external 0.1-MHz to 35-MHz frequency if desired, when the receiver is not in use.

Remote control circuitry includes a teletype readback of pertinent front panel controls and tuning status to the remote operator from each receiver.

1-3. DESCRIPTION OF UNITS

a. GENERAL - Each Receiving Set comprises modular units and interconnecting cabling, mounted in a single rack as shown in figure 1-1. All unit circuitry is solid state design, with printed circuit plug-in boards throughout. All units are on tilt-lock slides and lock in the up or down position for servicing; each unit contains its own power supply and includes forced air cooling systems, with removable air filters, where required. Unit panels are finished in light gray enamel per MIL-E-15090. Text in paragraphs 1-3b through 1-3g describe individual units and their functions. Block diagrams (figure 1-4 and 1-5) show unit functioning in the various receiver modes.

b. PERMANENT MAGNET LOUDSPEAKER, LS-588/U - The LS-588/U provides audio monitoring for the receiver.

c. RADIO FREQUENCY TUNER, TN-525/FRR - The TN-525/FRR tunes the 2-32 MHz input into four bands and displays the tuned frequency on a digital

* ±1.5 dB

indicator driven by a computer-type decade counter, to the .0001-MHz increment. The tuner is a superheterodyne type employing a local oscillator and two i-f stages, a 4-band selector switch and a continuous tuning knob. Within the first i-f stage there is a separate i-f for each band in order to minimize mixer crossings. In synthesized operation (remote or manual) the bands are electrically selected and the tuning is performed by servo from the KY-661/URR. The TN-525/FRR includes circuitry for receiver AFC operation.

d. DEMULTIPLEXER, TD-969/FRR - The TD-969/FRR converts the 250-KHz stage from the TN-525/FRR into audio in isolated channels. Demultiplexing of the two translated sideband channels occurs within this unit. AGC channel feedback source selection and attack-and-decay speed are selected by front panel control (the latter may be selected remotely). The TD-969/FRR receives the carrier re-supply injection frequency from the TN-525/FRR for the sideband product detectors.

e. REFERENCE SIGNAL GENERATOR, 0-1510/URR - The 0-1510/URR provides a .2-3.2 MHz stabilized frequency (referenced to its stable 1-mc standard) to the TN-525/FRR in synthesized operation of the receiver. It also supplies the 1-MHz standard output to the TN-525/FRR as reference for all receiver frequencies. The stabilized .2-3.2 MHz is used to lock the TN-525/FRR local oscillator. In remote or manual operation, 0-1510/URR control information is used to servo-tune the TN-525/FRR. The 0-1510/URR includes the 1-MHz standard and automatic switching circuitry for internal/external standards. A phase comparator meter is included to check phase differences between the two standard sources.

f. COMMAND SIGNAL DECODER, KY-661/URR - The KY-661/URR receives each set of addressal function (control location) and action function (control position) codes from an associated converter-storer (see table 1-2) and routes signals to the intended controls on the receiver for tuning action. The KY-661/URR also includes the tuning servo circuitry for tuning the TN-525/FRR via the 0-1510/URR setting and includes the readback transmitter, in order to send, from the receiver, a readback of control positions to the remote operator.

g. SIGNAL DATA CONVERTER-STORER, CV-2520(V)/URC - A CV-2520(V)/URC (used with Receiving Set AN/FRR-85(V)1) receives the coded teletype tuning message from the remote operator, converts the serial teletype pulses into parallel charges for each character, and stores them in a memory section. When a "receiver tune" code is received at the end of the message, the CV-2520(V)/URC releases the message, code-by-code, to the Command Signal Decoder (KY-661/URR) in one of the receivers.

1-4. REFERENCE DATA

Table 1-1 lists quick-reference technical data on Receiving Set AN/FRR-85(V)1 and includes the nominal specification figures defining a receiver. Table 1-2 lists teletype input codes required to tune a receiver from a remote site. Table 1-3 lists "equipment selector" codes available for a single receiver; the selector code is individual to each receiver in order to ensure that a message sent to a particular receiver enters only the intended receiver from a common teletype channel. Table 1-4 lists the readback codes issuing from a receiver and their significance in control positions.

TABLE 1-1. TECHNICAL SPECIFICATIONS, AN/FRR-85(V)1

Frequency range:	2-32 MHz
Modes of reception:	SSB, 2-channel ISB, 4-channel ISB, (direct channel 250-3,040 Hz, translated channel 350- 3,040 Hz) or symmetrical channel (CW, MCW and AM symmetrical about carrier); FSK, FAX, and Data, with suitable terminal equipment.
Channel widths (nominal):	CW, MCW, AM: 2.5/6.0KHz Sideband: 3KHz ea.
Tuning:	Remote/synthesized or local/synthesized: In 100-Hz steps over 4 bands Local/non-synthesized: continuous over 4 bands
Band divisions:	Band 1 2-4MHz 2 4-8MHz 3 8-16 MHz 4 16-32MHz
Intermediate Frequencies:	.625MHz, 1.25MHz, 2.5MHz, 5.0MHz, 250kHz

TABLE 1-1. TECHNICAL SPECIFICATIONS, AN/FRR-85(V)1 (cont)

250-KHz IF Channel Selectivity: -	Sideband (at -3dB pts):	Direct 2.79KHz Translated 2.69KHz
	CW, MCW (at -3db pts): 2.5KHz AM (at -3db pts): 6.0KHz	
AFC:		For non-synthesized reception of signal with partial carrier, drift compensator circuit reduces error in audio to within 1 Hz. Operates to maximum drift of ±1000 Hz and to a maximum drift rate of 10 Hz per second, at 1 uv input.
Antenna input impedance:		50 ohms (nominal), unbalanced.
Sensitivity vs. noise:		Sensitivity is 0.5uv minimum for 10db signal plus noise to noise ratio.
Intermodulation (in-channel):		Down at least 40db with 2-tone r-f input of 2 uv to 20,000 uv.
Channel cross-talk:		Down at least 55db from level of signal in desired channel.
Signal-to-hum ratio: in output:		At least 40db.
Harmonic Distortion:		1% maximum (SSB).
Image ratio:		At least 80db when referenced to a 1 uv input signal.
IF rejection:		At least 100db when referenced to a 1 uv input signal.
Translated channel sub-carrier:		250 kHz ±6.29 kHz
Gain Control:		Panel control at r-f stage provides a variation of 120db for r-f and i-f stages.
AGC:		Maintains constant* output with input at antenna varying from 1 uv to 1 volt. Individual control for each channel.
BFO:		BFO adjustment range for CW reception is ±3KHz.
IF monitor outputs:		Four channel -47dbm outputs at 250-KHz stage for 50 ohm loads. Type BNC connectors.
Audio outputs:		a. Four sideband channels and one symmetrical channel. Each channel delivers +10dbm into a 600 ohm (±10%) load. MS3102A24-28S Connector. Balanced or unbalanced. b. One output for a 4 ohm speaker MS3102-A14S-2S connector. May be switched to monitor any channel. c. One output to a headphone jack mounted on front panel. Suitable for mating with a standard type PJ-055B plug. May be switched to monitor any channel.
Audio Level adjustments:		a. Each sideband or symmetrical channel is continuously adjustable between -36dbm and +10dbm (when 0dbm = 1mw into a 600 ohm load). b. Speaker and headphone output continuously adjustable by front panel knob.

* ±1.5 dBm at 1 mw (0 dBm) output.

TABLE 1-1. TECHNICAL SPECIFICATIONS, AN/FRR-85(V)1 (cont)

Frequency stability:	For synthesized reception, receiver frequency stability is within 1 part in 10^8 for a channel in ambient temperature within the limits of 0° to 50° C over a 24-hr. period.
Remote control and readback:	Remote teletype code control (with manual override) is provided for the following receiver controls: - a. Frequency tuning, in 100-Hz increments (includes band change). b. Synthesized/AFC mode selection. c. 4-Channel/Symmetrical mode selection. d. Symmetrical mode channel (CW/AM, 2.5/6.0KHz) e. AGC time constant per channel. Readback is provided for all above control positions with receiver status and AFC alarm codes, in addition.
Remote tuning input:	From teletype loop, 60ma or 20ma, neutral or polar. 5-level codes (adaptable up to 8-level* transmission equipment) with 74.2-baud transmission speed. Codes per table 1-2 and 1-3.
Control position readback output:	5-bit codes in serial teletype wet (mercury) contact keying from polar relay. 5-level codes (adaptable up to 8-level* transmission equipment) with 74.2-baud transmission speed. Codes per table 1-4.
Power supply:	115VAC ±10%VAC, 47-63Hz, single phase. 725 watts max consumption.
Ambient temperature and humidity:	0 to 50° C and up to 95% relative humidity.
Automatic tuning time:	10 seconds (maximum) from receipt of complete message.
Frequency Counter input: (used as test counter)	0.1-35.0 MHz @ 250 mv RMS. Jack on front panel suitable for mating with a standard type plug.

* In 6-, 7-, or 8-level pattern, code is in first 5 bits. Speed of transmission not to exceed 60 WPM for 8-level pattern; 5-level pattern to be used for transmission from punched tape.

TABLE 1-2. REMOTE TUNING INPUT CODES

CHARACTER RECEPTION ORDER*	ADDRESSAL FUNCTION	ACTION FUNCTION	5-BIT CODE BIT 12345	TELETYPE CHARACTERS	
				CCIT	ASCII**
1	Receiver Selector		2 codes (see table 1-3)		
2	0-1510/URR 10 MHz switch		11000	A	C
3		0	01000	Line Feed	B
		1	00100	Space	D
		2	01100	I	F
		3	00010	Carriage Return	H
4	0-1510/URR 1 MHz switch		10100	S	E
5		0	01000	Line Feed	B
		1	00100	Space	D
		2	01100	I	F
		3	00010	Carriage Return	H
		4	01010	R	J
		5	00110	N	L
		6	01110	C	N
		7	00001	T	P
		8	01001	L	R
		9	00101	H	T
6	0-1510/URR 100 KHz switch		11100	U	G
7		0-9	Same as 5th Character		
8	0-1510/URR 10 KHz switch		10010	D	I
9		0-9	Same as 5th Character		
10	0-1510/URR 1 KHz switch		11010	J	K
11		0-9	Same as 5th Character		

* Except for the 1st and 26th character, characters may be received in any order, as long as the corresponding character follows its addressal function character. However, quickest tuning results (about 7 seconds) are obtained by the reception of the characters in the order shown.

** Only the first 5 bits of 7-bit code transmitted are utilized by the receiver.

TABLE 1-2. REMOTE TUNING INPUT CODES (cont)

CHARACTER RECEPTION ORDER	ADDRESSAL FUNCTION	ACTION FUNCTION	5-BIT CODE BIT 12345	TELETYPE CHARACTERS	
				CCIT	ASCII*
12	0-1510/URR .1 KHz		10110	F	M
13		0-9	Same as 5th Character		
14	TD-969/FRR MODE switch		11110	K	O
15		AM 2.5 KC	01000	Line Feed	B
		AM 6 KC	00100	Space	D
		CW 2.5 KC	01100	I	F
		CW 6 KC	00010	Carriage Return	H
		ISB	01010	R	J
16	TD-969/FRR AGC TIME CONSTANT switch, channel SYM/B2		10001	Z	Q
17		SLOW	01000	Line Feed	B
		MEDIUM	00100	Space	D
		FAST	01100	I	F
18	TD-969/FRR AGC TIME CONSTANT switch, channel B1		11001	W	S
19			Same as 17th character		
20	TD-969/FRR AGC TIME CONSTANT switch, channel A1		10101	Y	U
21			Same as 17th character		
22	TD-969/FRR AGC TIME CONSTANT switch, channel A2		11101	Q	W
23			Same as 17th character		

* Only the first 5 bits of 7-bit code transmitted are utilized by the receiver.

TABLE 1-2. REMOTE TUNING INPUT CODES (cont)

CHARACTER RECEPTION ORDER	ADDRESSAL FUNCTION	ACTION FUNCTION	5-BIT CODE BIT 12345	TELETYPE CHARACTERS	
				CCIT	ASCII*
24	TN-525/FRR FUNCTION switch		10011	B	Y
25		SYNTH	01000	Line Feed	B
		AFC	00100	Space	D
26	Receiver tune		10000	E	A
**	Clear		01111	V	↑

* Only the first 5 bits of 7-bit code transmitted are utilized by the receiver.

** "Clear" code, received at any time before "Receiver tune", will delete codes from receiver memory.

TABLE 1-3. REMOTE TUNING INPUT CODES, EQUIPMENT SELECTOR

EQUIPMENT SELECTED		5-BIT CODE BITS 12345	TELETYPE CCIT	CHARACTERS ASCII*
Block	A	10101	Y	U
	B	10110	F	M
	C	11010	J	K
	D	11001	W	S
	E	10011	B	Y
Receiver	1	00010	Carriage Return	H
	2	01010	R	J
	3	01100	I	F
	4	01000	Line Feed	B
	5	00100	Space	D
	6	01101	P	V
	7	00101	H	T
	8	00011	O	X
	9	00111	M	
	10	01011	C	Z

* Only the first 5 bits of 7-bit code transmitted are utilized by the receiver.

TABLE 1-4. REMOTE TUNING READBACK OUTPUT CODES

CHARACTER TRANSMISSION ORDER	CONTROL OR CONDITION	POSITION INDICATED	CODE BITS	
			1	2345
1	To reset remote readback indicator for new cycle.		1	0000
2	0-1510/URR 10 MHz switch	0		1111
		1		0111
		2		1011
		3		0011
	Receiver "tuning/ready/fault" status	see note*		
3	0-1510/URR 1 MHz switch	0		1111
		1		0111
		2		1011
		3		0011
		4		1101
		5		0101
		6		1001
		7		0001
		8		1110
		9		0110
	Receiver "tuning/ready/fault" status	see note*		
4	0-1510/URR 100 kHz switch	0-9, same as 0-1510/URR 1 MHz sw.		
	Equipment selected	selected	1	
		not selected	0	
5	0-1510/URR 10 kHz switch	0-9, same as 0-1510/URR 1 MHz sw.		
	CV-2520(V)/URC power	off	1	
		on	0	
6	0-1510/URR 1 kHz switch	0-9, same as 0-1510/URR 1 MHz sw.		

* Readback of receiver tuning status is contained in bit #1 of codes #2 and #3 combined: -

Bit #1

Code #2	Code #3	Status
0	1	tuning
1	0	ready
1	1	fault

TABLE 1-4. REMOTE TUNING READBACK OUTPUT CODES (cont)

CHARACTER TRANSMISSION ORDER	CONTROL OR CONDITION	POSITION INDICATED	CODE BITS	
			1	2345
6 (cont)	automatic tuning set up	no	1	
		yes	0	
7	0-1510/URR .1 kHz switch	0-9, same as 0-1510/URR 1 MHz sw.		
	AFC alarm	alarm	1	
		no alarm	0	
8	TN-525/FRR FUNCTION switch	SYNTH	1	1000
		LOCAL	0	1000
9	TN-525/FRR FUNCTION switch	AFC	1	1000
		LOCAL	0	1000
10	TD-969/FRR MODE switch	2.5 kHz AM	0	1110
		6 kHz AM	0	0110
		2.5 kHz CW	0	1010
		6 kHz CW	0	0010
		ISB	0	1100
11	TD-969/FRR AGC TIME CONSTANT switches, SYM/B2 and B1	SLOW and SLOW	0	1111
		SLOW and MED	0	1101
		SLOW and FAST	0	1110
		MED and SLOW	0	0111
		MED and MED	0	0101
		MED and FAST	0	0110
		FAST and SLOW	0	1011
		FAST and MED	0	1001
		FAST and FAST	0	1010
12	TD-969/FRR AGC TIME CONSTANT switches, A2 and A1	SLOW and SLOW	0	1111
		SLOW and MED	0	1101
		SLOW and FAST	0	1110
		MED and SLOW	0	0111
		MED and MED	0	0101
		MED and FAST	0	0110

TABLE 1-4. REMOTE TUNING READBACK OUTPUT CODES (cont)

CHARACTER TRANSMISSION ORDER	CONTROL OR CONDITION	POSITION INDICATED	CODE BITS	
			1	2345
12 (cont)	TD-969/FRR AGC TIME CONSTANT switches, A2 and A1	FAST and SLOW	0	1011
		FAST and MED	0	1001
		FAST and FAST	0	1010
13	Receiver Identification*	Rcvr #1	0	1111
		2	0	0111
		3	0	1011
		4	0	0011
		5	0	1101
		6	0	0101
		7	0	1001
		8	0	0001
		9	0	1110
		10	0	0110

* Individual code per receiver.

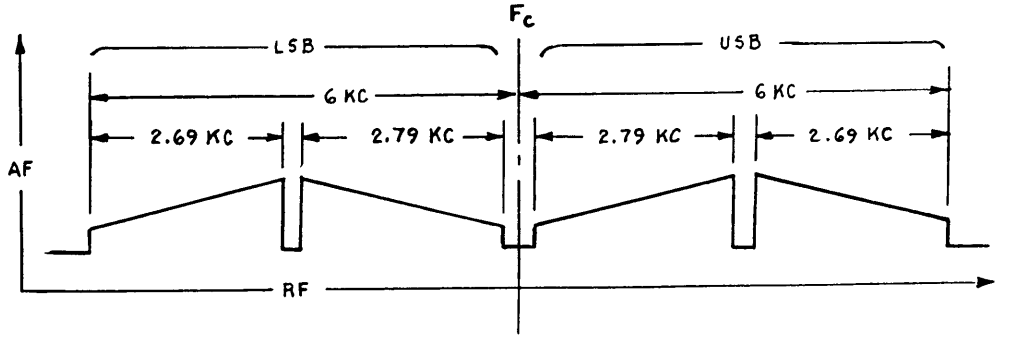


Figure 1-2. Input Signal Spectrum, 4-Channel ISB

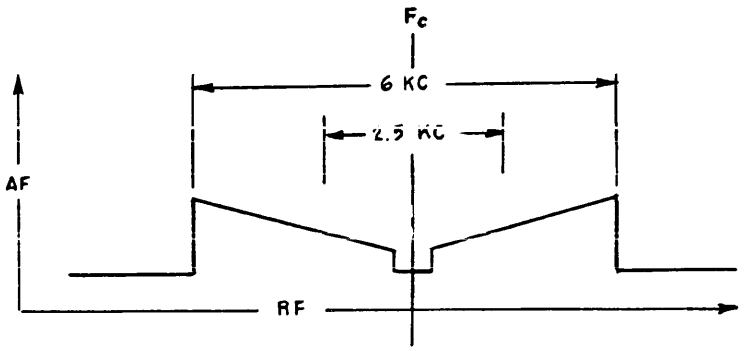
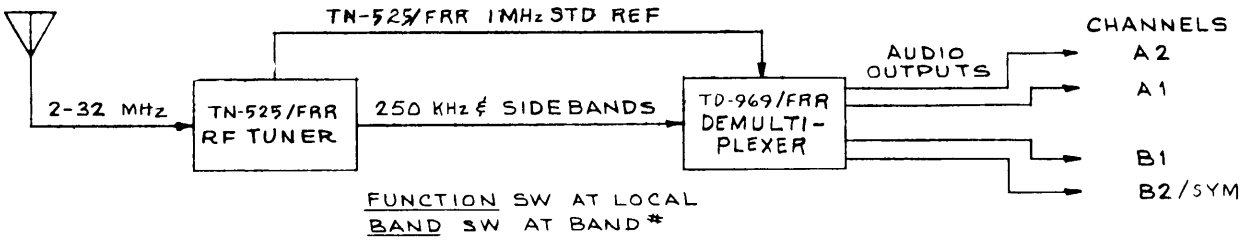
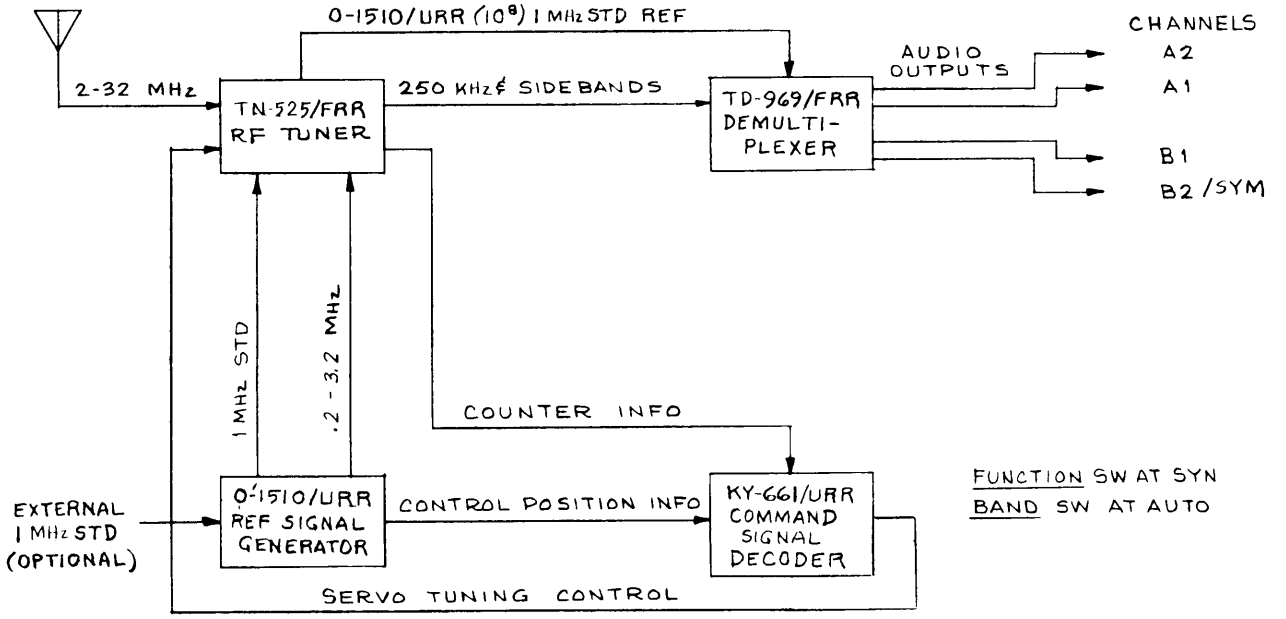


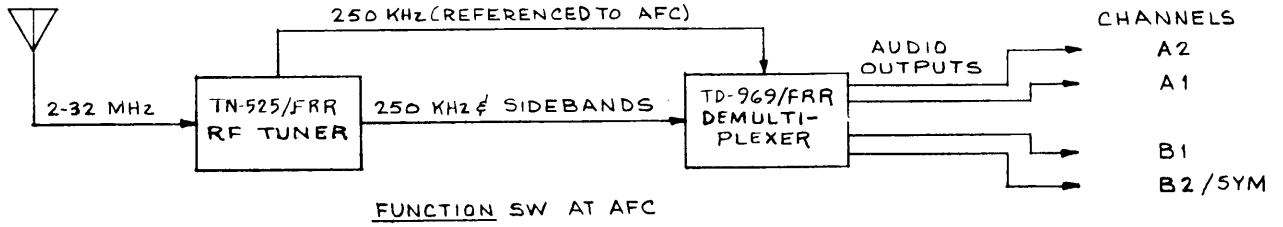
Figure 1-3. Input Signal Spectrum, Symmetrical Channel



A. MANUAL / LOCAL

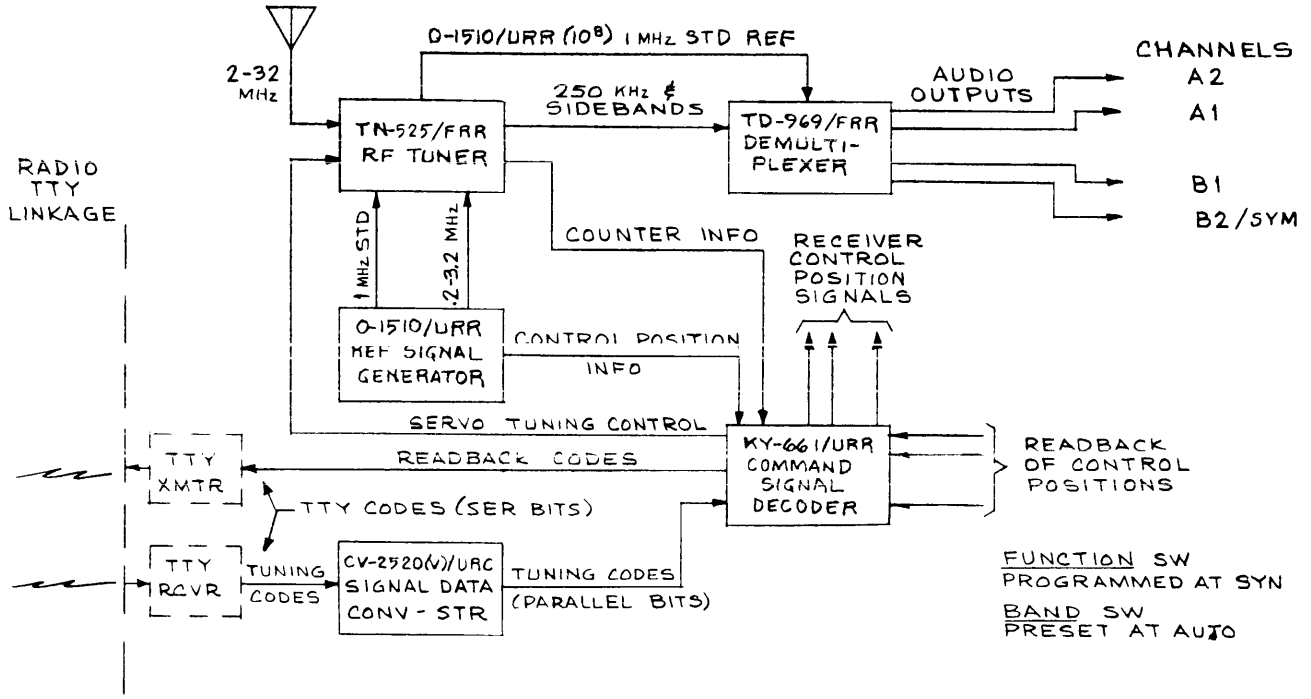


B. MANUAL / SYNTH

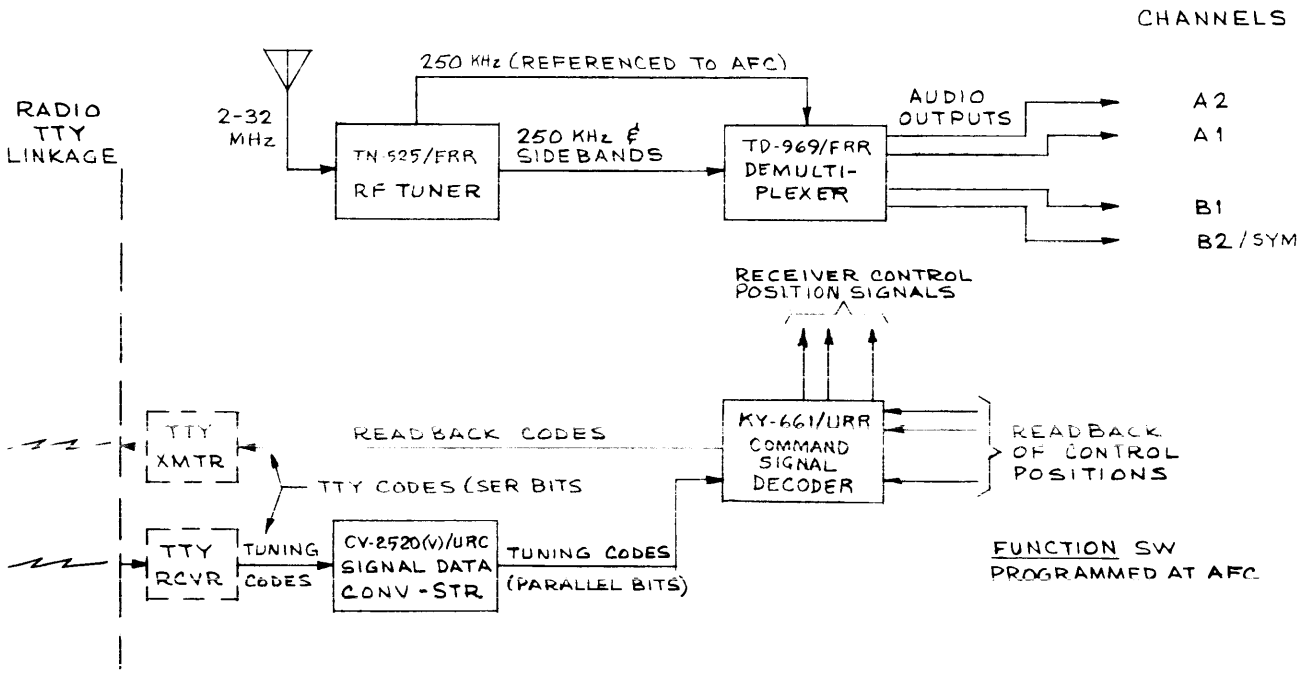


C. MANUAL / AFC

Figure 1-4. Functional Block Diagram, Modular Units, Manual Tuning, Single Receiver



A. REMOTE / SYNTH



B. REMOTE / AFC

Figure 1-5. Functional Block Diagram, Modular Units, Remote Tuning, Single Receiver

SECTION 2
INSTALLATION

2-1. UNPACKING AND HANDLING

Inspect the AN/FRR-85(V)1 packing cases for possible damage when they arrive at the operating site. With respect to damage to equipment for which the carrier is liable, the Technical Material Corporation will assist in describing methods of repair and the furnishing of replacement parts.

2-2. POWER REQUIREMENTS

Each Receiving Set leaves the factory wired to operate from a 115-VAC 50/60 cps, single phase power source. The receiver can be rewired for operation from a 220-VAC 50/60 cps single phase source by changing transformer primary winding jumper leads in each rack modular unit (TN-525/FRR, TD-969/FRR etc.). Refer to figure 2-1 for typical primary connections. In units including a blower or other motor, ensure that 115 VAC is maintained across the motor as shown. Transformers involved are: 1T1, 2T1, 3T1, 4T1, 5T1, 6T1, 7T1, 8T1, and 10T1*.

2-3. SITE SELECTION

The Receiving Set may be located in any enclosure (room, deck or van) with sufficient clearances as depicted in figure 2-2. Allow a minimum of two feet above the rack for adequate heat dissipation and to prevent back pressure in the cooling air exhaust stream. Because the Receiving Set is normally operated from a distant remote control station (rather than locally), access to front panel controls may be kept at a minimum. The Receiving Set is designed for fixed station, transportable or ship installation. Remote tuning is by means of conventional teletype linkage by a cable from the teletype loop current supply. The connector (MEMORY INPUT) for this cable is located at the upper interface panel located at the rear of the rack. The length of the cable should be consistent with the loop current supply so as to prevent line drop (see paragraph 2-4d(3)).

2-4. INSTALLATION REQUIREMENTS

a. ASSEMBLY OF RECEIVING SET - Install modular units and blank panels into the rack as shown in figure 1-1. Connect modular unit interconnecting cabling within the rack as shown in figure 5-1.

All modular units are slide-mounted on tilt-lock drawer slides. The external part of the slide mount arrives pre-installed in the rack; the internal part arrives pre-installed on the modular unit. To install a unit, refer to figure 2-3 and proceed as follows:

CAUTION

If rack is not yet bolted to the floor during this phase, start by installing bottom units first in order to avoid rack tipping over from extended center of gravity.

(1) Pull the center section of the rack-mounted (external) portion of the slide-mount out until it locks in an extended position.

(2) Position the unit-mounted (internal) portion of the slide-mount in the tracks of the external portion and ease the modular unit into the rack until the release buttons engage the holes in the track.

(3) Depress the release buttons and slide the modular unit completely into the rack.

(4) Secure the modular unit front panel to the rack flange with machine screws and fiber washers supplied in the shipment.

In the receiver there are duplications of some modular units (see figure 1-1) and these units are interchangeable. Unit numbers (example: 1 or 5 for Radio Frequency Tuner TN-525/FRR) are marked on the rack front and rear facings adjacent to the modular unit bay location but are not marked on the modular units themselves. When locating these units, either one may be mounted in either bay.

Unit numbers form the prefixes for receptacle "J" reference symbol numbers as they appear in figure 5-1; these prefixes, however, are not marked on the modular unit chasses. This arrangement is to preserve interchangeability of units. The rack cabling is assigned prefix number "9". Reference symbol numbers for plugs (part of the cabling) contain these prefixes as they appear in figure 5-1 but cable markers (adjacent to the plugs) do not contain them. Cable destination markers, however, do contain the unit prefixes (example: "1J1" for 9W1P1) in the same way as they appear in figure 5-1.

b. EXTERNAL WIRING CONNECTIONS - All system wiring shall be connected to the Receiving Set at the receiver (upper and lower) interface panels located at the rear of the rack (see figure 2-2). Figures 2-4 through 2-9 contain wire-run information for constructing individual cables to

* Of Unit 10, associated CV-2520(V)/URC.

each connector on an interface panel. Since the Receiving Sets are designed to function in a variety of systems, however, an analysis should be made as to necessary connections before proceeding to make up the cables. This analysis may be made from information contained in the following sub-paragraphs.

Each Receiving Set may be installed in a single installation or as part of an array, in relation to the remote tuning input and remote readback output lines. In an array, all the Receiving Sets work from a common remote tuning input teletype channel and the individual receiver readback outputs are brought out to a common teletype channel for each block of ten receivers.

For the remote tuning and readback feature, a Signal Data Converter-Storer (RTMU-41B) must be added at the bottom of the rack. In an array only one Converter-Storer is required for every ten receivers.

(1) Single Installation (figure 2-4) - Necessary connections for a single AN/FRR-85(V)1 installation are: an antenna input for each receiver, a 4-channel audio output for each receiver, a common remote tuning input and a common readback output (both to teletype linkage equipment) and a "remote interface" cable. If it is preferred to use a 1-mc standard of higher stability than the receiver's 1-mc standard (with 1 part in $1X10^8$ stability), an external connection must be made. With such a connection, there is an automatic switching feature, built into each receiver, that switches in the alternate standard (internal or external) upon the failure of the normal standard.

(2) Array (figure 2-5) - Necessary connections for an array of receivers (working from a common TTY data channel each for remote tuning and readback) is the same as for a single installation with the following additions. Up to fifty receivers may be operated from one channel. For this it is required that there be one Converter-Storer for every block (ten receivers). Equipment selector codes (see table 1-3) from the remote control site are available for five blocks (A-E) with ten receivers (1-10) per block.

The connection for the common remote tuning and readback data channels is at the same point (the MEMORY INPUT connector on the upper interface panel) in the receiver rack containing the Converter-Storer as for the single Receiving Set installation. However, remote interface cable extensions, running between the Converter-Storer and interface panels of the other receiver racks in a block, are required as shown.

An array involving more than ten receivers (or more than one Converter-Storer) requires a current loop adjustment at the associated teletype keyer (refer to paragraph 2-4d(3)) for the common remote tuning input teletype data channel. Each block (of ten receivers) requires a separate data channel for readback.

c. RECEIVER RECOGNITION AND IDENTIFICATION - Receiver block selection (in remote tuning) and receiver identification (in readback) are accomplished by plug-in print circuit (P/C) boards. Referring to table 1-3, the A-E code is passed by a hand-wired matrix in P/C board A3 in the Converter-Storer for the block; this board is appropriately marked "A", "B", "C", "D", or "E" for identity. The following code (1-10) is passed by code gates in the Converter-Storer and the interface cabling to each receiver. Receiver identification in the readback is determined by handwiring on P/C board A2 in the Command Signal Decoder for the particular receiver. This board is appropriately marked (i.e.: "1", "2", or "3", etc.).

The P/C board (A3) in each Converter-Storer and the P/C board (A2) in each Command Signal Decoder should be inspected to ascertain that they are consistent with the installation plan and the interface cable wiring (figure 2-7). The receivers should then be identified by means of marking or decals along the front mounting flanges of the Receiving Set racks. The P/C boards may be ordered prewired from TMC or they may be wired on installation. Figure 2-10 contains instructions for the X-Y matrix wiring for letters A through E in Converter-Storer P/C board A3. Figure 2-11 contains wiring instructions for the "1-10" wiring of P/C board A2 in the Command Signal Decoder.

d. ADJUSTMENTS TO VARIATIONS IN TELETYPE LINKAGE EQUIPMENT

(1) General - Although the remote tuning input and remote readback output circuitries in the Receiving Set are designed to operate with 75 baud (100 WPM) teletype linkages, these circuits are designed to adapt to a variety of baud ratings, current loops and code levels in the teletype linkage equipment.

(2) Baud Rating

NOTE

Baud (or WPM) rating capacity of the Receiving Set is based on the clock timing circuit in the remote tuning input. The timing circuit is designed to match pulse widths within each code. The tuning codes themselves may enter at any rate desired, but not to exceed a 60 WPM typing speed when transmitting from a punched tape.

The baud rating at the remote tuning input is determined by plug-in P/C board A2 in the Converter-Storer; that of the remote readback output is determined by plug-in P/C board A3 in the Command Signal Decoder. In Receiving Set AN/FRR-85(V)1 these boards are designed for a 75-baud operation; 45-baud (60 WPM) P/C boards are also available.

(3) Current Loop - In the remote tuning input, the teletype equipment output current loop operates through isolation keyer P/C board A1 in the Converter-Storer. The keyer will operate from a 20 ma (low level) or 60 ma (high level) loop. When working from a 60 ma loop, however, there may be a bypass of resistor R5 on P/C board A1 by adding a strap around it at terminals provided on the board (see figure 2-7). A slight adjustment at the potentiometer in the teletype output should then be made to bring 6 volts across the isolation keyer at the points indicated. This latter adjustment should also be performed for an installation containing more than one Converter-Storer on the same teletype current loop.

(4) Code Levels - Although the AN/FRR-85(V)1 uses a 5-level code at the remote tuning input and readback output, shift registers in the receiver are paced for adaptability to up to an 8-level teletype linkage equipment. No adjustments are necessary for the adaption.

e. CHECKOUT PROCEDURE - Initial checkout will encompass a single receiver section only; merely repeat the procedure for the remaining receiver section.

Checkout will simply ascertain AC power input to each unit by means of visual pilot lamp and readout indications, and will verify signal flow through the receiver.

Refer to figure 3-1, and proceed as follows:

(1) Place all POWER switches on all units to the ON position.

(2) Ascertain that pilot lamps (marked POWER, ON, or similar notation) on all units except the TN-525/FRR are lit; the TN-525 unit has no pilot lamp per se, but the readout indicator will illuminate, indicating AC power input.

NOTES

a. IF NO POWER INDICATORS ARE LIT: ensure that AC power connections have been made to the entire equipment rack. Check such areas as main wall-mounted power switches, circuit breakers, and/or fuses at the installation site itself. Be certain that power mains into the receiver carry 50/60 Hz AC, at the proper voltage (115/230 VAC, dependent upon internal power transformer wiring, per figure 2-1).

b. IF SOME POWER INDICATORS ARE LIT: the equipment rack itself is receiving supply voltage. If an AC input wiring change was made, ensure that all units have been properly modified to operate on the same AC input, and ensure that such AC input is actually present at all power receptacles at the rear of the rack. Check to see that all units are plugged into the rack's AC power strip, and that all POWER switches are set to ON.

c. IF EITHER OF THE ABOVE CASES: check all fuse indicators on all units; if an indicator is lit, replace the associated fuse (fuses are located directly behind indicators: twist indicator CCW and pull straight out; replace fuse, reinsert indicator/holder, and twist CW to lock). If fuses continue to open-circuit, STOP: a trouble-shooting procedure is indicated. Do not replace further, until the trouble has been remedied. NEVER replace with fuses of a higher current rating than indicated on the open fuse.

(3) Set the 0-1510/URR to 10.0000 MHz.

(4) Set TN-525/FRR controls as follows:

CONTROL	POSITION
POWER	STANDBY
FUNCTION*	SYN
COUNTER MODE	REC
BAND SWITCH	AUTO
METER FUNCTION	RF - HIGH
SILENCER ON	down
RF GAIN	AGC
INPUT ATTENUATOR	down

(5) Set TD-969/FRR controls as follows:

CONTROL	POSITION
METER SENSITIVITY	0
MONITOR SELECTOR	SYM
LOCAL GAIN	full CCW
AGC TIME CONSTANT (SYM-B2)*	FAST
MODE*	AM-6kc

(6) Set TN-525 POWER switch to ON; TUNE knob should rotate, and frequency readout should change, approaching 10.0000 MHz. As the TN-525 nears 10 MHz, TUNE knob should slow, then stop. Simultaneously, SYNC INDICATOR lamp should light.

(7) Advance TD-969 LOCAL GAIN control CW to a comfortable listening level; depending upon location, propagation conditions, and time of day, station WWV (U.S. National Bureau of Standards' official station) may be heard; even if WWV is not being received, background noise should be apparent. This will indicate signal flow through the receiver.

(8) IF WWV is being received well, an additional (AFC) check may be made: rotate TN-525 FUNCTION switch clockwise to AFC position, and depress AFC TUNE switch, if SYNC INDICATOR

*NOTE: All controls marked above with an asterisk should be rotated in a CW direction ONLY. Controls not listed may be left in any position.

lamp does not light hold down AFC TUNE switch, and slowly adjust FINE TUNE control until sync indication is achieved. Immediately release AFC TUNE switch; continued reception of WWV indicates AFC operability. AFC corrective action can be observed on the TN-525's PHASE DIFFERENCE meter.

(9) Remote checkout may be accomplished by presetting receiver controls per section 3-2(a)2 and table 3-3, and following section 3-2(a)4. Fastest tuning results by proceeding from left to right on the FUNCTION row of programmer C-7775/UR.

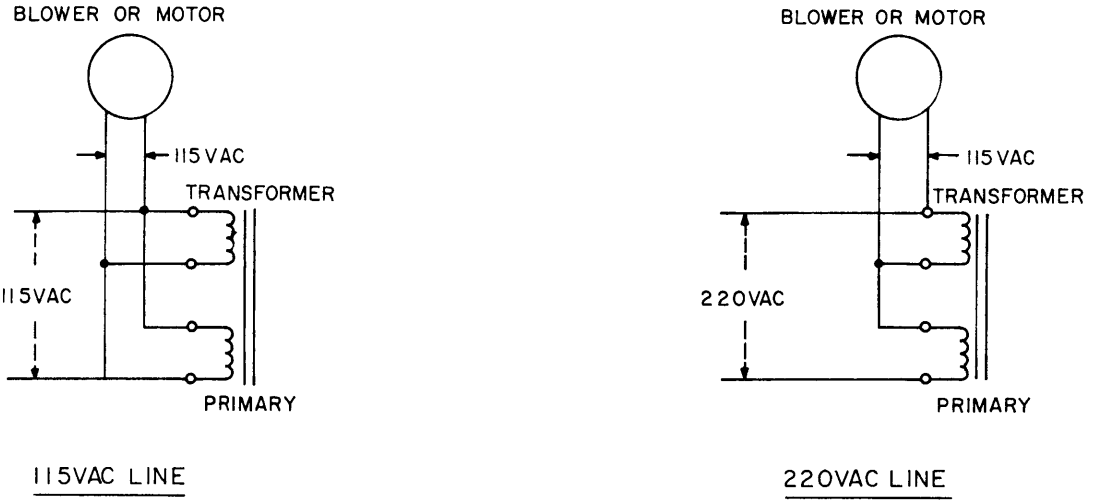


Figure 2-1. 115-220 VAC Conversion

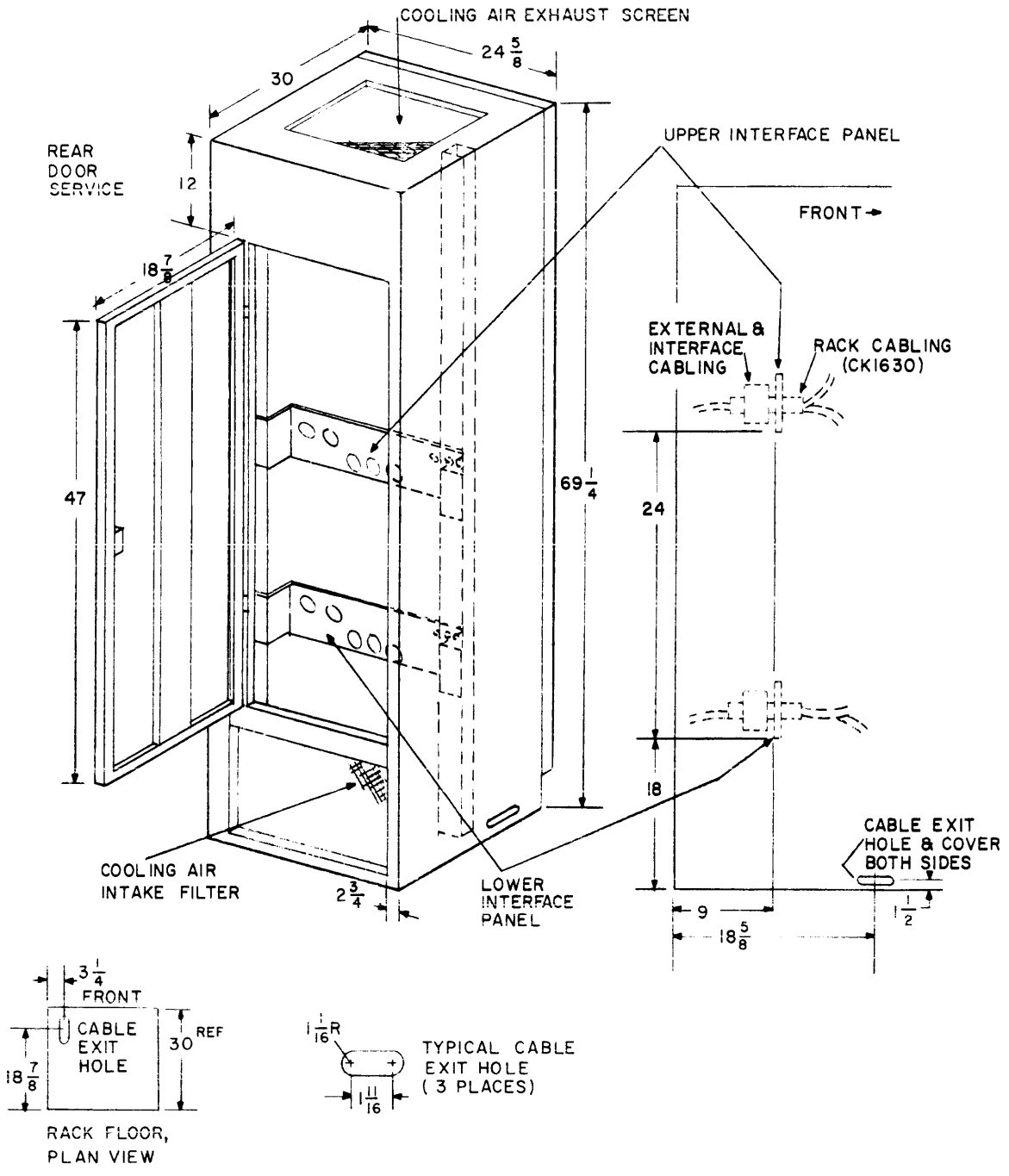
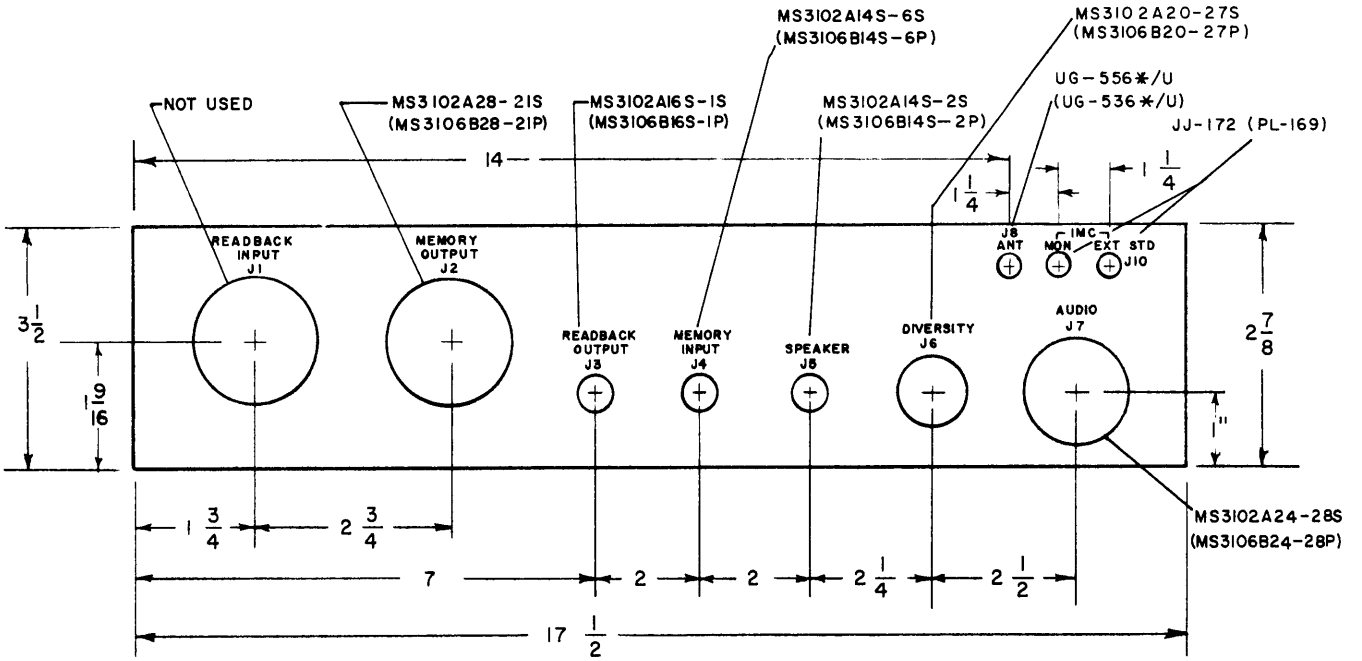


Figure 2-2. Outline and Installation Dimensions, AN/FRR-85(V)1 (Sheet 1 of 2)



NOTE: MATING CONNECTORS SHOWN IN PARANTHESES( ), SUPPLIED IN SHIPMENT.

INTERFACE PANEL DIMENSIONS AND MATING CONNECTORS

Figure 2-2. Outline and Installation Dimensions, AN/FRR-85(V)1 (Sheet 2 of 2)

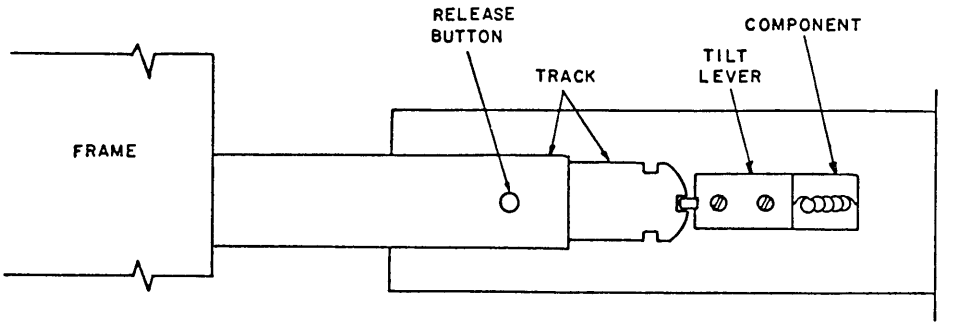


Figure 2-3. Slide Mounting Details

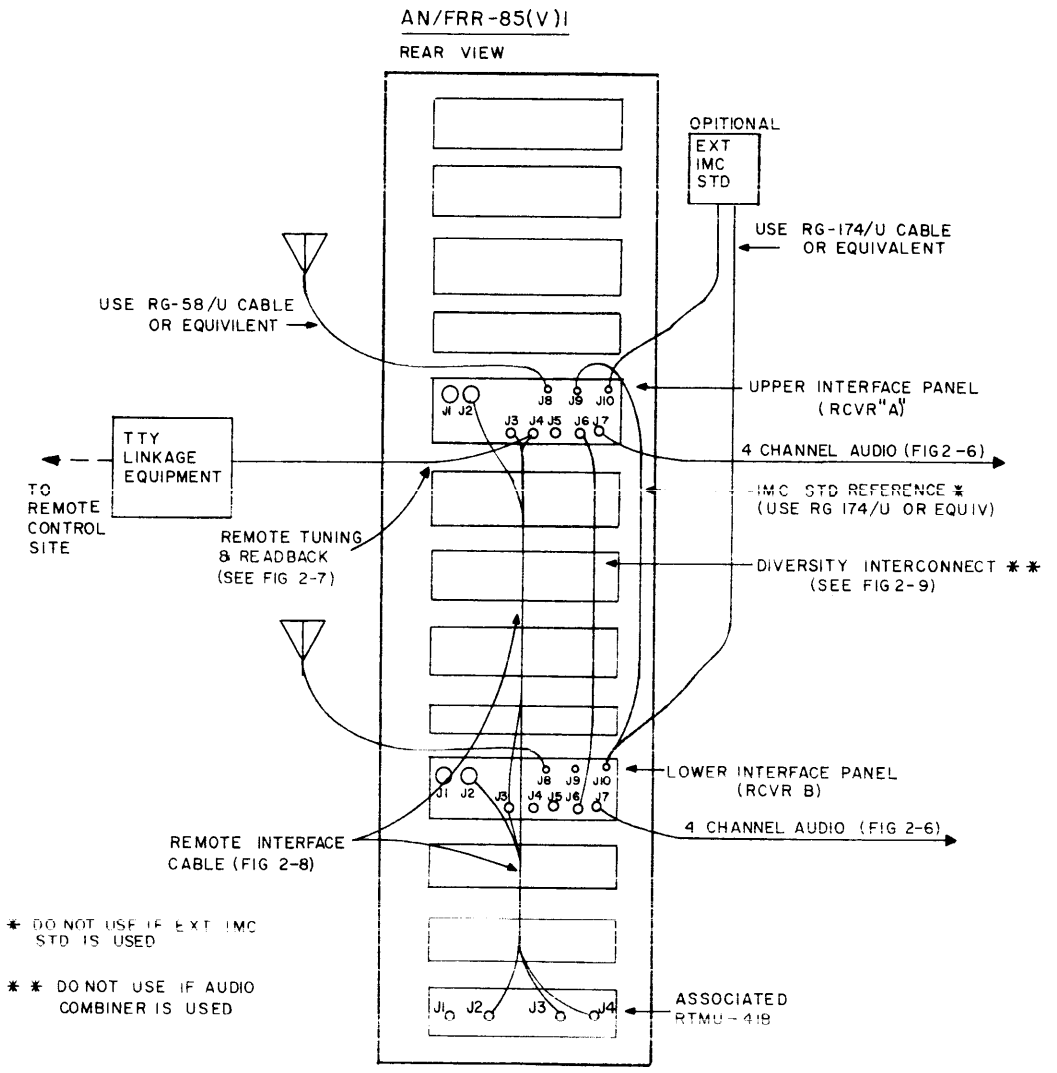


Figure 2-4. External Wiring Connections, Single Installation AN/FRR-85(V)1

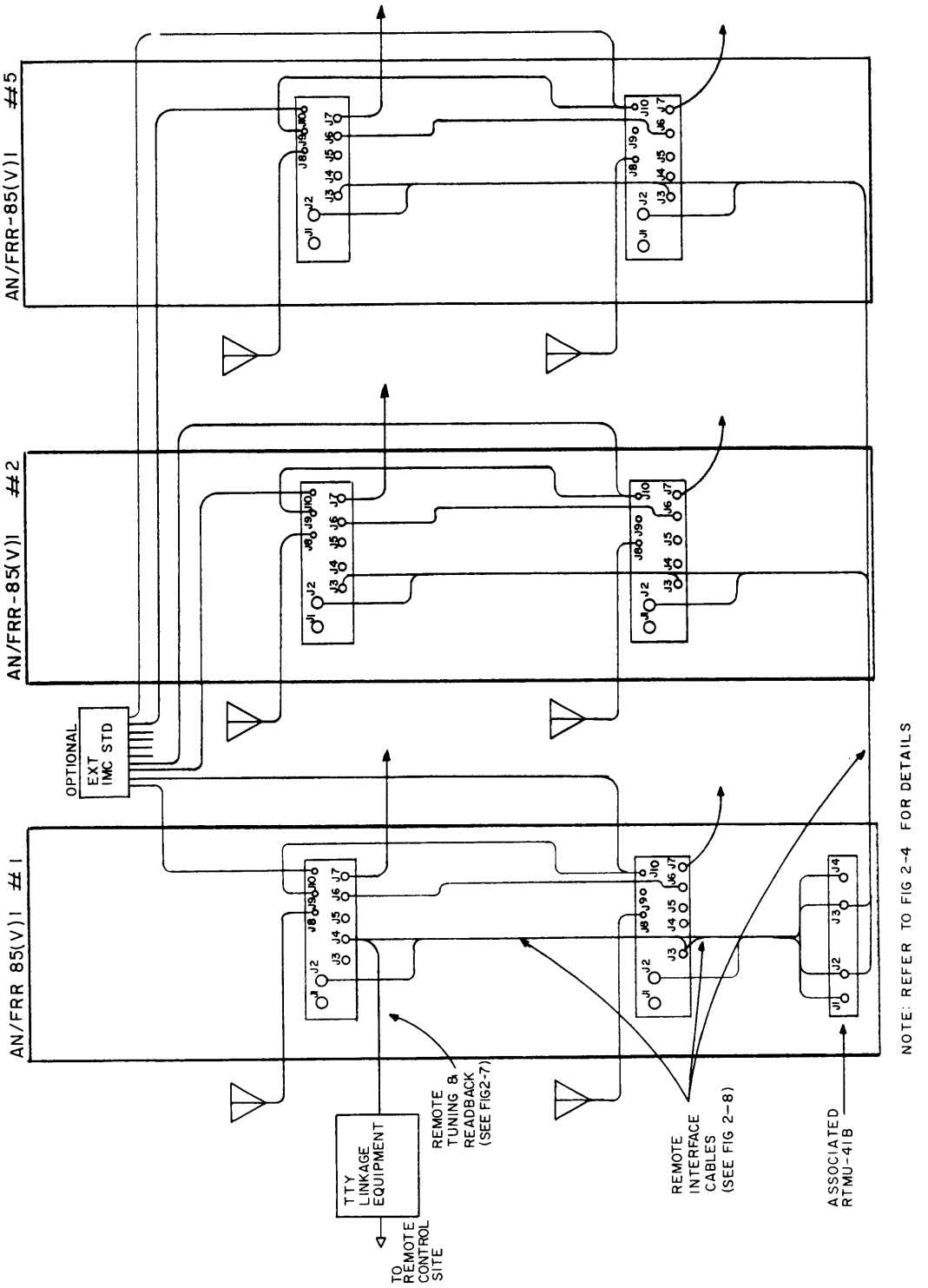


Figure 2-5. External Wiring Connections, Multiple Installation, AN/FRR-85(V)1

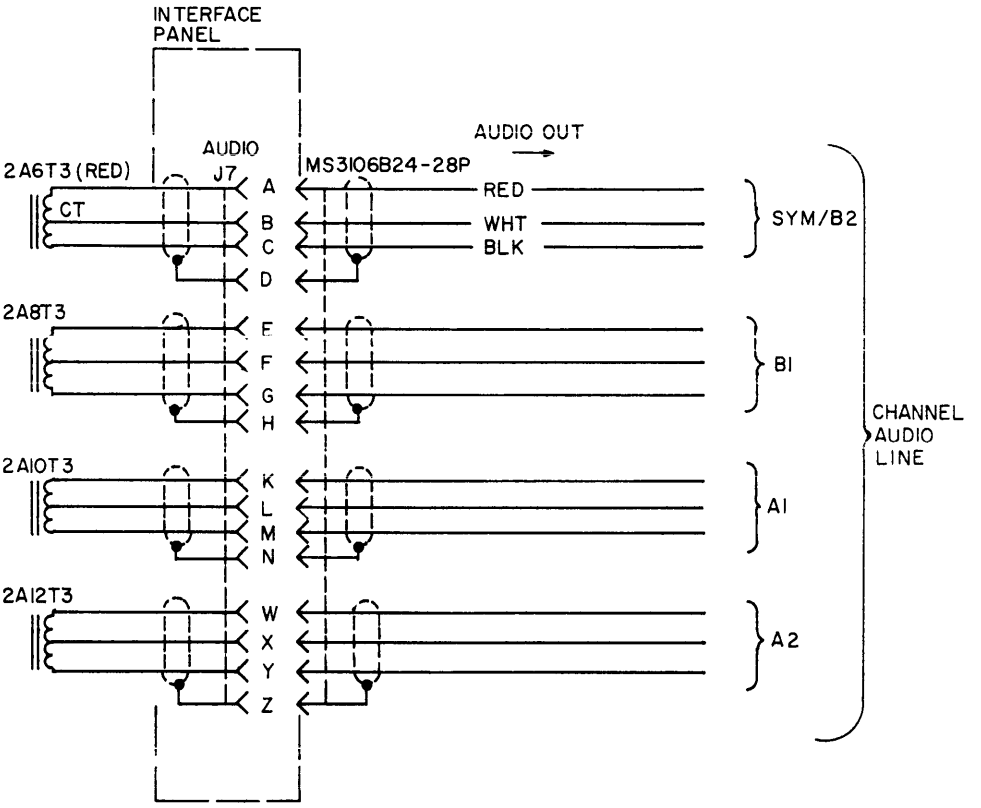


Figure 2-6. Audio Output Cable Wiring

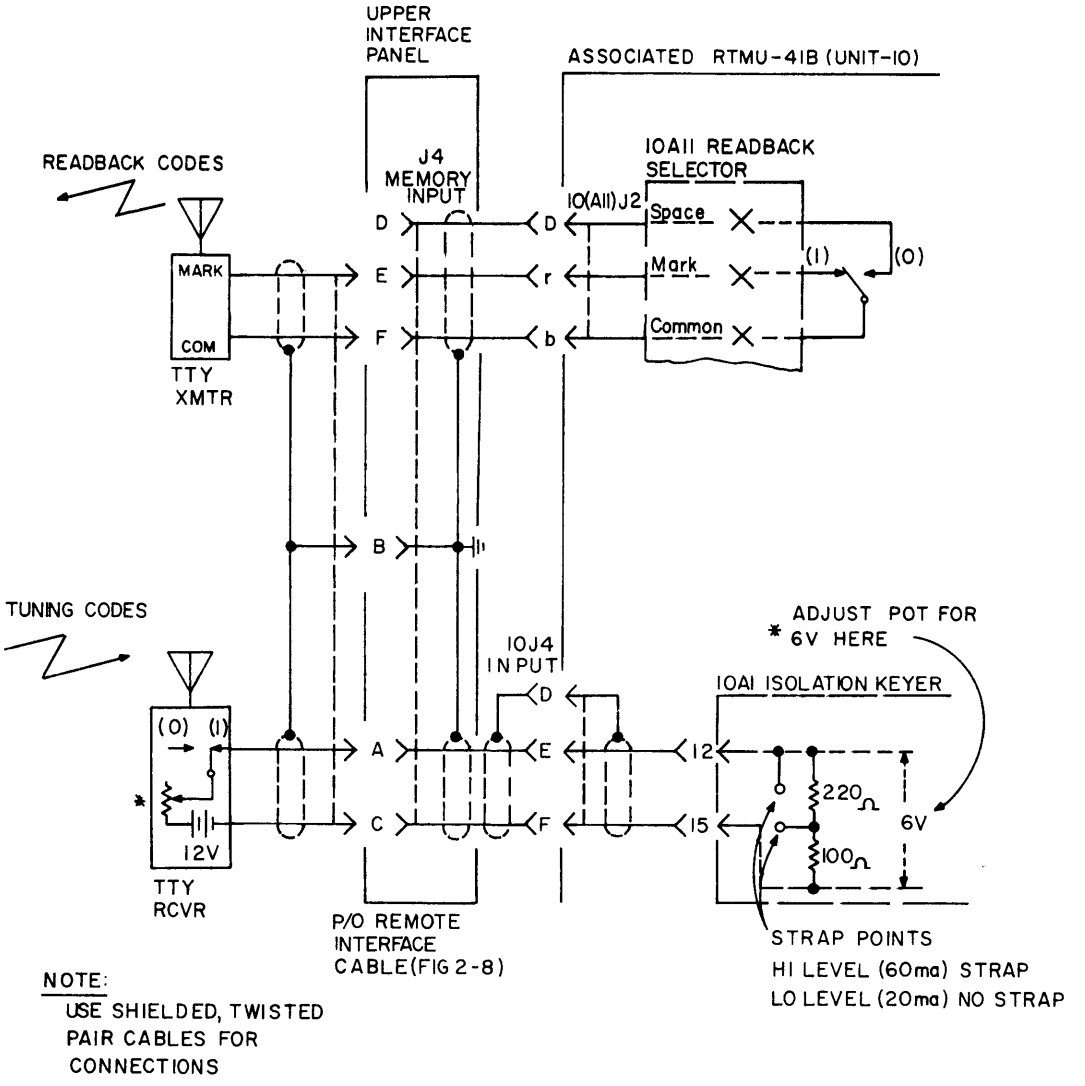


Figure 2-7. Remote Tuning and Readback Wiring

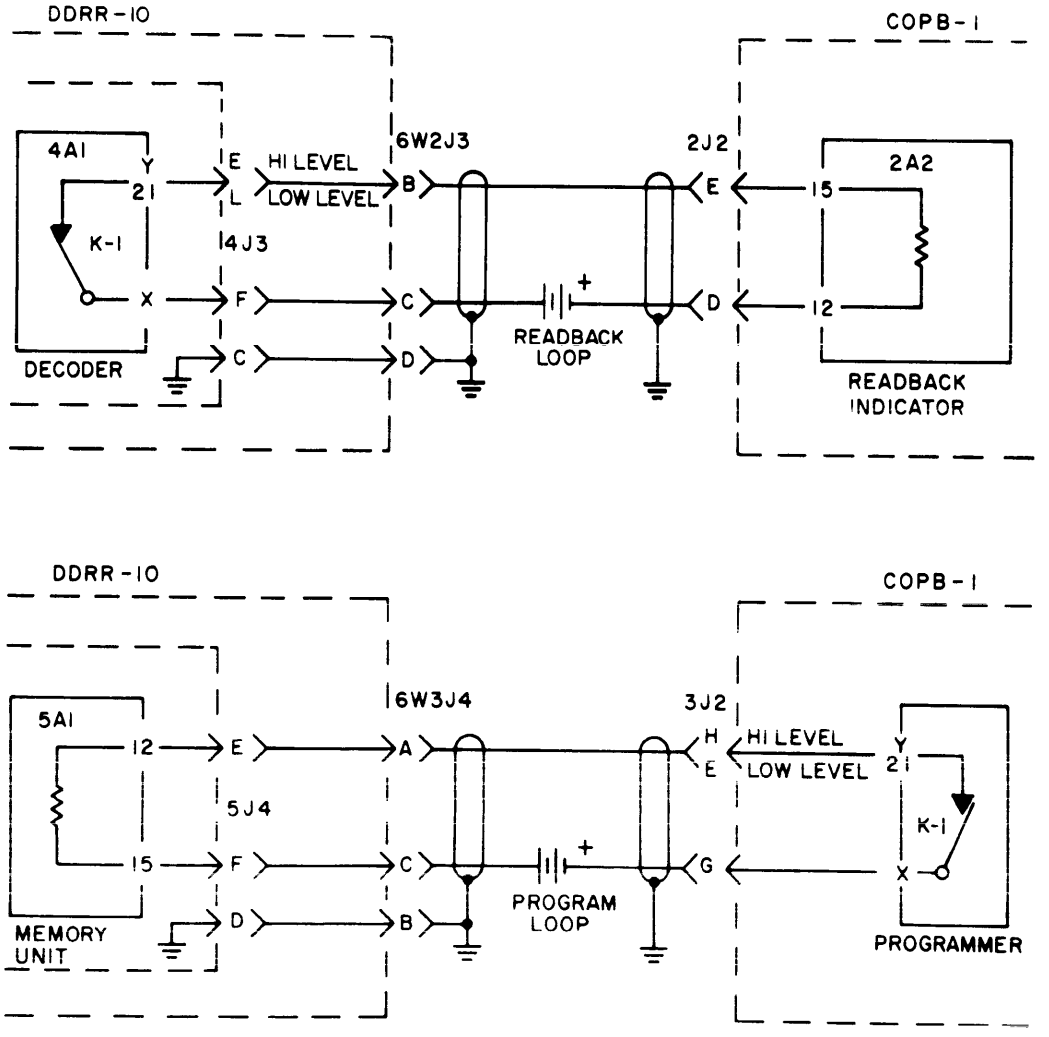


Figure 2-8. Interface Cable Wiring

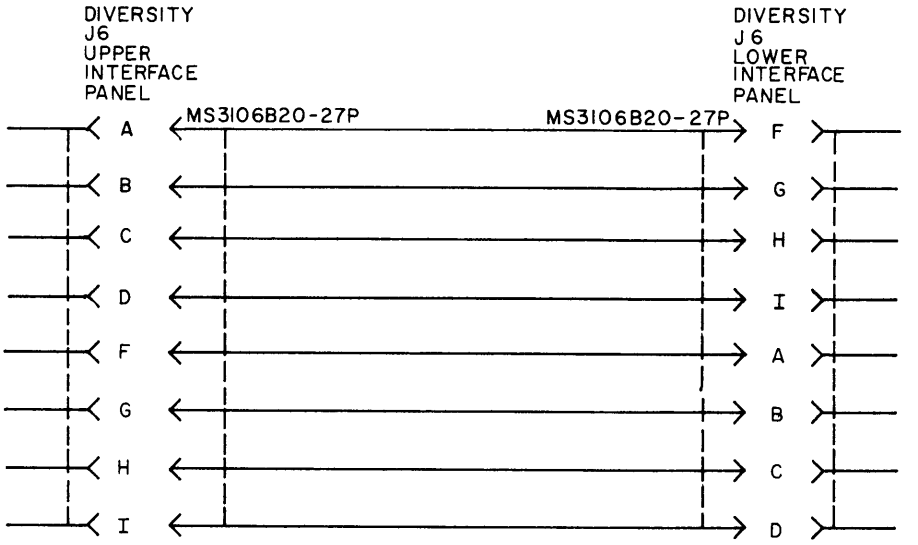
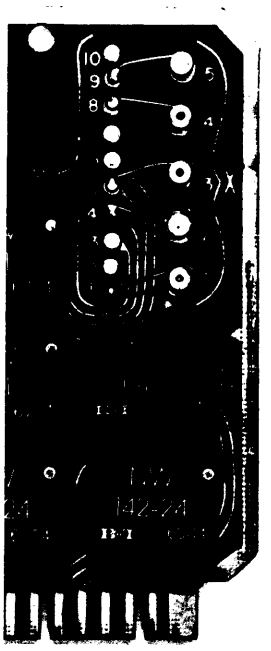


Figure 2-9. Diversity Quieter Cable Wiring

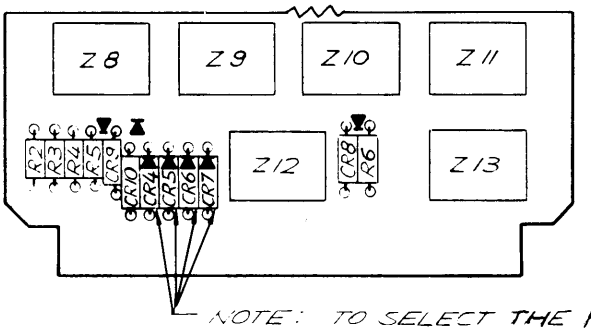


SHOWN IN POSITION
EQUIPMENT SELECTION A
(SEE CHART)

EQUIPMENT SELECTION JUMPER GUIDE

EQUIPMENT	JUMPER X				
	1	2	3	4	5
A	Y1	Y4	Y5	Y8	Y9
B	Y1	Y4	Y5	Y7	Y10
C	Y1	Y3	Y6	Y7	Y10
D	Y1	Y3	Y6	Y8	Y9
E	Y1	Y4	Y6	Y7	Y9

Figure 2-10. A-E Block Selection Wiring of P/C Board 10A3



NOTE: TO SELECT THE PROPER CODES FOR READBACK ON THE RSSA - USE CHART.

RSSA READBACK SELECTION CHART					
TMC PT. NO.	RCR	CR7	CR6	CR5	CR4
A4517-1	1	✓	✓	✓	✓
A4517-2	2	✓	✓	✓	*
A4517-3	3	✓	✓	*	✓
A4517-4	4	✓	✓	*	*
A4517-5	5	✓	*	✓	✓
A4517-6	6	✓	*	✓	*
A4517-7	7	✓	*	*	✓
A4517-8	8	✓	*	*	*
A4517-9	9	*	✓	✓	✓
A4517-10	10	*	✓	✓	*

* DENOTES REMOVAL OF DIODES

Figure 2-11. 1-10 Readback Identification Wiring of P/C Boards 4A2 and 8A2

SECTION 3

OPERATION

3-1. FUNCTIONAL OPERATION

a. GENERAL - Capabilities of each receiver include four channel reception modes, three frequency control modes and two tuning modes. These are: channel reception: SSB, 2- or 4-channel ISB, and symmetrical channel; frequency control: synthesized, AFC, and local tuning; tuning: remote and manual. Modes that can be used together are indicated in table 3-1.

b. CHANNEL RECEPTION MODES - 4-Channel ISB reception is used when two direct sideband channels (A1 and B1) and two translated channels (A2 and B2) are transmitted on single carrier reference Fc (see figure 1-2). The procedure is to tune the receiver to Fc (in the 2-32 MHz range) and set it for 4-channel ISB reception. This prepares the receiver to receive SSB (upper or lower sideband), two-channel ISB or four-channel ISB. There are individual channel controls for audio output level and AGC attack-and-decay speed and source. AGC SOURCE controls may be positioned to feed the AGC output of any one channel to any other channel or to its own channel input. In addition, manually adjusted gain may be inserted in each channel, in lieu of AGC, as set up by the RF GAIN control on the RF Tuner TN-525/FRR.

Symmetrical channel reception is used for AM, CW, or MCW transmission (see figure 1-3). In AM reception, the receiver is set for reception of the entire 6-kHz width of frequencies, symmetrical about Fc; in this case, one channel of audio appears in the output. In CW reception, controls are set to receive a 2.5-kHz width, symmetrical about Fc. Setting controls for AM routes the signal into an envelope detector to produce audio; a CW setting processes the signal through a product detector, and an adjustable BFO control is used to produce the desired audio frequency output. For MCW (carrier modulated by a keyed audio tone), the controls are positioned for AM reception at 2.5-kHz width to produce the audio. AGC output of the symmetrical channel is fed back into the channel input, with a selection of three attack-and-decay speeds. As in the 4- channel mode, manual gain control at the TN-525 may be substituted. The B2 channel output (of the ISB Mode) is utilized for symmetrical channel reception.

All channel reception modes, described above, are selected at Demultiplexer TD-969/FRR control panel.

c. MANUAL TUNING AND OPERATION MODES - Module performance for the three operation modes in manual tuning is shown in figure 1-4. In local operation (figure 1-4A), RF Tuner TN-525/FRR and Demultiplexer TD-969/FRR are used alone to receive the signal. Receiver frequency stability is maintained by an internal 1-MHz standard in the TN-525/FRR. For synthesized operation (figure 1-4B) receiver frequencies are held stable by a 1-MHz standard in Reference Signal Generator 0-1510/URR. In this mode, the 0-1510/URR is set for the carrier frequency (in 100-Hz steps) and RF Tuner TN-525/FRR is automatically (or manually) tuned to synchronize with the 0-1510/URR by means of servo tuning in Command Signal Decoder KY-661/URR. In automatic tuning, when the 0-1510/URR carrier frequency controls are thus positioned, a comparison is made in the KY-661/URR between 0-1510/URR control positions and receiver frequencies as indicated by the TN-525/FRR digital frequency counter. The KY-661/URR then issues an error control signal to a servo motor in the TN-525/FRR and a servo tuning action takes place until the TN-525/FRR is synchronized with the 0-1510/URR. When the synchronization point has been reached, the

TABLE 3-1. OPERATING CAPABILITIES, SINGLE RECEIVER

TUNING MODE	FREQUENCY CONTROL MODE	CHANNEL RECEPTION MODE			
		SSB	2-CHANNEL ISB	4-CHANNEL ISB	SYMMETRICAL CHANNEL
MANUAL	SYN	X	X	X	X
	AFC	X	X	X	X
	LOCAL	X	X	X	X
REMOTE	SYN	X	X	X	X
	AFC	Requires local operator assist.			
	LOCAL	Local oscillator control mode not possible from remote site.			

0-1510/URR locks the receiver frequencies to the same stability (within 1 part in 10^8) as its 1-MHz standard. If a higher stability is required, an external 1-MHz standard may be used; the internal standard then becomes phase-locked to the external. In this case, the 0-1510/URR includes an automatic switching device between the two standards which will switch in the alternate standard upon failure of the normal standard. For AFC (automatic frequency control) operation (figure 1-4C), receiver frequencies are made to track the drift in the incoming carrier from the transmitter. This is possible in a transmission containing a partial (30 db suppressed) carrier and is generally required if the transmitter frequencies are unstabilized. The result of the tracking action is to maintain fidelity and stability in the audio output frequencies.

d. REMOTE TUNING AND OPERATION MODES - Module performance for the two operation modes in remote tuning of the single receiver is shown in figure 1-5. In synthesized operation (figure 1-5A), receiver frequencies are held stable by the 0-1510/URR 1-MHz standard, as in the manual/synthesized mode. Remote tuning is accomplished by TTY (teletype) code transmission from the remote control station. Codes enter associated Signal Data Converter-Storer CV-2520(V)/URC and are stored in a memory section. Upon receipt of the "E" (receiver tune) code, the stored codes proceed into Command Signal Decoder KY-661/URR which sends information to each receiver control, moving it to its programmed position. When the 0-1510/URR carrier frequency controls are thus positioned, a comparison is made in the KY-661/URR between 0-1510/URR control positions and receiver frequencies as indicated by the TN-525/FRR digital frequency counter. The KY-661/URR then issues an error control signal to a servo motor in the TN-525/FRR and a servo tuning action takes place until the TN-525/FRR is synchronized with the 0-1510/URR. For AFC operation, the receiver is first tuned for synthesized operation, to center it on the expected carrier. When the signal transmission (for which the receiver was tuned) begins, the receiver is tuned for AFC by a separate tuning code message (figure 1-5B). The TN-525/FRR picks up the carrier component in the incoming signal and is then tuned locally, until the AFC circuit captures the incoming carrier.

As many as fifty single receivers may be remotely controlled by one teletype channel transmission line, each message containing different tuning instructions, and the messages sent one-by-one. For this purpose each message contains, as its first two codes, an "equipment selector" double-code combination (see table 1-3). The first code is a letter (A-E) and the second a number (1-10). This represents the full quota of fifty receivers, composed of five blocks (A-E) of receivers, with ten receivers (1-10) in each block. An individually wired matrix on plug-in P/C board A3 in the commonly-shared Signal Data Converter-Storer functions to "unlock" its memory upon receiving the correct alpha-numeric combination, so that the subsequent tuning instruction codes may be stored.

In remote tuning modes, sending the "equipment selector" codes also triggers a readback from the selected receiver. The receiver then transmits a continuous cycling of control position readback codes (in TTY form) back to the remote control station for monitoring purposes. This readback includes the position of each of the remotely operated controls and includes status codes to indicate when tuning has been accomplished for a particular message, and whether or not the receiver is ready for a new message.

Receiver status readback codes include the following information to the remote operator (terminology is that generally appearing in remote readout panel): -

Terminology	Significance
Tuning	Tuning is in process. Either servo motor is still moving or controls are still moving.
Ready	Tuning and/or control moving process has been completed. Synchronization has been achieved.
Fault	Complete tuning and control repositioning has failed to take place within fifteen seconds from the time of the receipt of the "receiver tune" code.
Decoder Power Off	Signal Data Converter-Storer has lost its ac power input.
Non-automatic	Local operator has disconnected servo-tuning capabilities. This prevents a remote tuning.
Equipment Selected	Indicates that the intended receiver has received the "equipment selector" codes and has opened its memory section to receive the message.

A drift alarm readback is also included, when the receiver is operating on AFC, to indicate that the incoming carrier component is about to drift outside the AFC hold-in range.

3-2. OPERATING PROCEDURES

a. REMOTE CONTROL - Complete step-by-step procedure for the remote tuning of the receiver may be found in the separate instruction manual accompanying the remote control console. Necessary procedures for remote tuning as listed in this (the receiver site) manual includes only the initial set-up of certain controls to prepare the receiver for remote tuning and a generalized description of procedure followed by the remote operator.

(1) Description of Controls - Table 3-2 lists functions of front panel controls for a single receiver as they appear in figure 3-1, Front Panel Controls. The "R" and "M" symbols, in the REMOTE/MANUAL column, opposite each control in table 3-2 indicate "remote" and "manual" controls, respectively.

TABLE 3-2. CONTROL FUNCTIONS, SINGLE RECEIVER

UNIT	CONTROL	FUNCTION	REMOTE(R) MANUAL(M)
RF Tuner TN-525/FRR	PHASE DIFFERENCE meter	Meter indicates synchronization status of TN-525/FRR with 0-1510/URR (for SYN mode) and with AFC circuit (for AFC mode).	M
	MEGAHERTZ digital display	Indicates frequency count of h-f (local) oscillator in terms of carrier for which it is tuned. Displays 2.0000 to 32.0000-MHz figure in .001-MHz increments.	M
	RF/AFC LEVEL meter	Monitors incoming signal level in r-f stage or incoming carrier level in AFC. Reading controlled by METER FUNCTION switch.	M
	INPUT ATTENUATOR switch	Switches in attenuator at antenna input for strong signals. Up position inserts attenuator manually. Down position sets receiver for automatic insertion of attenuator when antenna signal rises above 30mv.	M
	SYNC INDICATOR lamp	Light indicates synchronization point has been reached for TN-525/FRR with 0-1510/URR (for SYN mode) or with AFC circuit (for AFC mode).	R, M
	RF GAIN knob	Adjusts gain for r-f and i-f stages in TN-525/FRR or sets unit for agc.	M
	SILENCER	ON position inserts noise silencer circuit for deleting impulse noise.	M
	AFC TUNE switch	Momentary switch prepares AFC circuit to "capture" incoming carrier.	R, M
	METER FUNCTION switch	Selects input to RF/AFC LEVEL meter. RF LOW position connects weak level signal directly to meter. RF HIGH position connects strong level signal to meter. AFC CARRIER connects captured carrier level (in AFC circuit) to meter.	M
	POWER switch	Connects power to TN-525/FRR in two stages. STANDBY position connects power to local oscillator oven only. ON position connects power to entire TD-525/FRR unit. OFF position disconnects all power to TN-525/FRR.	M
	FUNCTION switch (see *CAUTION)	SYN position places receiver in synthesized operation. AFC position places receiver in AFC operation. LOCAL position places receiver in non-synthesized operation with continuous tuning.	R, M R, M M
	COUNTER MODE INPUT jack	Input for external 0.1-35 MHz frequency to be measured by counter MEGAHERTZ display.	M

TABLE 3-2. CONTROL FUNCTIONS, SINGLE RECEIVER (cont)

UNIT	CONTROL	FUNCTION	REMOTE(R) MANUAL(M)
TN-525/FRR (cont)	COUNTER MODE switch	HIGH position measures external frequency to four places beyond decimal. LOW position measures external frequency to five places beyond decimal. REC position measures receiver frequency to four places beyond decimal.	M
	BAND SWITCH	Selects one of four r-f bands in TN-525/FRR input or sets units for automatic tuning. 2-4 pos. selects 2-4 MHz band. 4-8 pos. selects 4-8 MHz band. 8-16 pos. selects 8-16 MHz band. 16-32 pos. selects 16-32 MHz band. AUTO pos. sets TN-525/FRR for automatic tuning.	M
	TUNE knob	Continuous tuning adjustment of r-f band and h-f oscillator for incoming carrier frequency. Adjustment point displayed in MEGAHERTZ digital display.	R, M
	LOCK knob	Locks TUNE knob against movement.	M
	FINE TUNE knob	Used in conjunction with TUNE knob for fine tuning adjustment.	R, M
Demultiplexer TD-969/FRR	METER SENSITIVITY switch	Adjusts LINE-DBM meter sensitivity. 0 position, used for normal level audio, gives true reading on meter db scale. -10 position, is used for low level audio. Meter is read by subtracting 10 db. +10 position is used for high level audio. Meter is read by adding 10 db.	M
	LINE-DBM meter	Indicates db level of audio channel output as selected by MONITOR SELECTOR switch.	M
	SYM-B2 AGC SOURCE switch	Selects source of gain input for symmetrical channel (when MODE switch is in a symmetrical position) or for B2 channel (when MODE switch is in ISB position). For symmetrical mode, B2, B1, A1 or A2 position feeds symmetrical channel agc output back into its input. MAN position connects gain input so as to be controlled by TN-525/FRR RF GAIN knob. For ISB mode, B2, B1, A1 and A2 positions select these channels as a source of agc feedback into channel B2. MAN position connects gain input so as to be controlled by TN-525/FRR RF GAIN knob.	M

TABLE 3-2. CONTROL FUNCTIONS, SINGLE RECEIVER (cont)

UNIT	CONTROL	FUNCTION	REMOTE(R) MANUAL(M)
TD-969/FRR (cont)	B1 AGC SOURCE switch	Selects source of gain input for channel B1. B2, B1, A1 and A2 positions select these channels as a source of agc feedback into channel B1. MAN position connects gain input so as to be controlled by TN-525/FRR RF GAIN knob.	M
	A1 AGC SOURCE	Selects source of gain input for channel A1. B2, B1, A1 and A2 positions select these channels as a source of agc feedback into channel A1. MAN position connects gain input so as to be controlled by TN-525/FRR RF GAIN knob.	M
	A2 AGC SOURCE switch	Selects source of gain input for channel A2. B2, B1, A1 and A2 positions select these channels as a source of agc feedback into channel A2. MAN position connects gain input so as to be controlled by TN-525/FRR RF GAIN knob.	M
	MONITOR SELECTOR switch	Selects audio channel to be monitored at LINE-DBM meter, PHONE jack or speaker. SYM, B2, B1, A1 and A2 positions select channels; OFF positions turns off monitor circuit.	M
	SYM-B2 AGC TIME CONSTANT switch (see *CAUTION)	Selects attack-and-decay speed for agc output from symmetrical channel (when MODE switch is in a symmetrical position) or from B2 channel (when MODE switch is in ISB position). SLOW, MEDIUM and FAST positions select corresponding decay speeds.	R, M
	B1 AGC TIME CONSTANT switch (see *CAUTION)	Selects attack-and-decay speed for agc output from B1 channel.	R, M
	A1 AGC TIME CONSTANT switch (see *CAUTION)	Selects attack-and-decay speed for agc output from A1 channel.	R, M
	A2 AGC TIME CONSTANT switch (see *CAUTION)	Selects attack-and-decay speed for agc output from A2 channel.	R, M
	LOCAL GAIN knob	Adjusts audio level to PHONE jack or speaker.	M
	PHONE jack	Used for headset connection in monitoring channel selected by MONITOR SELECTOR switch.	M
	MODE switch (see *CAUTION)	Selects either 4 channel (ISB) reception mode or symmetrical reception mode. Within symmetrical mode, selects for CW or AM mode at 2.5-kHz or 6-kHz bandwidths.	R, M

TABLE 3-2. CONTROL FUNCTIONS, SINGLE RECEIVER (cont)

UNIT	CONTROL	FUNCTION	REMOTE(R) MANUAL(M)
TD-969/FRR (cont)	SYM/B2 LINE LEVEL ADJUST knob	-40 dbm to +12 dbm adjustment to symmetrical channel audio output (when MODE switch is in a symmetrical position) or to B2 channel (when MODE switch is in the ISB position). Actual adjustment is read on LINE DBM meter.	M
	B1 LINE LEVEL ADJUST knob	-40 dbm to +12 dbm adjustment to B1 channel audio output. Actual adjustment is read on LINE DBM meter.	M
	A1 LINE LEVEL ADJUST knob	-40 dbm to +12 dbm adjustment to A1 channel audio output. Actual adjustment is read on LINE DBM meter.	M
	A2 LINE LEVEL ADJUST knob	-40 dbm to +12 dbm adjustment to A2 channel audio output. Actual adjustment is read on LINE DBM meter.	M
	SYM BFO knob	Used in symmetrical CW mode. Adjusts BFO injection frequency ±3 kHz.	M
	POWER lamp	Light indicates TD-969/FRR is receiving line voltage.	M
	POWER switch	Connects line voltage TD-969/FRR.	M
Reference Signal Generator 0-1510/URR	10 MEGAHERTZ switch and window dial (see *CAUTION)	0, 1, 2, 3, positions tune 0-1510/URR for 10-MHz component in incoming carrier.	R, M
	1 MEGAHERTZ switch and window dial (see *CAUTION)	0-9 positions tune 0-1510/URR for 1-MHz component in incoming carrier.	R, M
	0.1 MEGAHERTZ switch and window dial (see *CAUTION)	0-9 positions tune 0-1510/URR for 100-kHz component in incoming carrier.	R, M
	0.01 MEGAHERTZ switch and window dial (see *CAUTION)	0-9 positions tune 0-1510/URR for 10-kHz component in incoming carrier.	R, M
	0.001 MEGAHERTZ switch and window dial (see *CAUTION)	0-9 positions tune 0-1510/URR for 1-kHz component in incoming carrier.	R, M
	0.0001 MEGAHERTZ switch and window dial (see *CAUTION)	0-9 positions tune 0-1510/URR for 0.1-kHz component in incoming carrier.	R, M
	PHASE COMPARATOR/FREQ DIFFERENCE meter and switch	Meter and switch display differences in frequency or phase between internal and external 1-MHz standards.	M

TABLE 3-2. CONTROL FUNCTIONS, SINGLE RECEIVER (cont)

UNIT	CONTROL	FUNCTION	REMOTE(R) MANUAL(M)
Reference Signal Generator 0-1510/URR (cont)	EXTERNAL STANDARD FAILURE lamp	Lamp indicates failure of external 1-MHz standard (when used).	M
	INTERNAL STANDARD FAILURE lamp	Light indicates failure of internal 1-MHz standard (in 0-1510/URR).	M
	POWER lamp	Light indicates 0-1510/URR is receiving line voltage.	M
	POWER switch	Connects line voltage to 0-1510/URR.	M
Command Signal Decoder KY-661/URR	FAULT lamp and button combination	FAULT light indicates failure of KY-661/URR servo to lock TN-525/FRR to 0-1510/URR. Button is used to recycle tuning servo.	M
	POWER lamp	Line indicates KY-661/URR is receiving line voltage.	M
	POWER switch	Connects line voltage to KY-661/URR.	M
Signal Data Converter-Storer CV-2520-(V)/URC	SIGNAL INPUT lamp	Blinking light indicates reception of coded bits into receiver tuning code input. Steady light indicates no code input. Used for local check of receiver in remote operation.	M
	POWER lamp	Light indicates CV-2520(V)/URC is receiving line voltage.	M
	POWER switch	Connects line voltage to CV-2520(V)/URC.	M

*CAUTION

These switches turn clockwise only, due to stepping switch drives. Do not attempt to force in a counter-clockwise direction; to do so may damage the stepping switch drive mechanism.

(2) Presetting Controls for Remote Tuning, Single Receiver - Presetting controls for the first time includes an initial warm-up period for stabilizing the 1-MHz reference standard in the 0-1510/URR and the 1-MHz standard in the TN-525/FRR. To do this, set the 0-1510/URR POWER switch at ON and allow one hour to elapse. Then set the TN-525/FRR POWER switch at STANDBY and allow another hour to elapse. At the end of the 2-hour period, the receiver frequency stability reaches its rated figure: within 1 part in 10^8. To keep this stability, in preparation for a consequent tuning, maintain the 0-1510/URR and TN-525/FRR POWER switches in these positions. In preparation for remote tuning, proceed to set controls as listed in table 3-3. Settings of controls not listed are optional.

(3) Sequence of Operation - Remote operator procedure, in general, is to program the tuning of the receiver on a push-button keyboard. As each button is pushed, a code is transmitted out of the remote station and into the memory section of Converter-Storer CV-2520(V)/URC. Codes are transmitted in pairs, one to select the control and one to position it. No action takes place, however, until the operator sends the "receiver tune" code at the end of the message. This code triggers Command Signal Decoder KY-661/URR to pull the codes, one-by-one, out of the Storer memory and move the receiver controls accordingly. While the controls are moving, a "tuning" status code is included in the readback to the operator; when controls have stopped moving and the receiver is synchronized to the programmed frequency, the "tuning" readback, changes to "ready". Should the servo fail to synchronize the receiver, the "tuning" readback will turn to "fault". In this case, the remote operator may recycle the tuning servo sequence by sending another message consisting only of another "receiver tune" code. At any time during the programming (before the "receiver tune" code is sent) the operator may correct a mistake by pressing a "clear" button; this effectively "erases" all previous codes in the Storer memory.

The first two codes in any message must be the "equipment selector" codes for the particular receiver to be tuned. These codes trigger a readback and open the memory section of the CV-2520(V)/URC for the tuning codes in the rest of the message. An incorrect "A-E" code will allow the memory input for the block to remain closed, and the rest of the message will have no effect on that block of receivers. The "1-10" code selects a receiver within the block by opening the memory output only to that receiver. Indication that the receiver has been selected is the "equipment selected" readback code to the remote operator.

TABLE 3-3. CONTROL PRESETTINGS FOR REMOTE TUNING, SINGLE RECEIVER

UNIT	CONTROL	SETTING
TN-525/FRR	INPUT ATTENUATOR switch	down
TN-525/FRR	RF GAIN knob	AGC
TN-525/FRR	SILENCER switch	off (down)
TN-525/FRR	LOCK knob	fully ccw
TN-525/FRR	POWER switch	ON
TN-525/FRR	COUNTER MODE switch	REC
TN-525/FRR	BAND SWITCH	AUTO
TD-969/FRR	AGC SOURCE switches (all four)	SYM/B2 for B2 B1 for B1 A1 for A1 A2 for A2
TD-969/FRR	LINE LEVEL ADJUST knobs (all four)*	0 dbm (as indicated) on LINE DBM meter
TD-969/FRR	MONITOR SELECTOR switch	OFF
TD-969/FRR	SYM BFO knob	for kHz-tone preferred in CW reception.
TD-969/FRR	POWER switch	ON
0-1510/URR	PHASE COMPARATOR/FREQ DIFFERENCE switch	PHASE COMPARATOR
0-1510/URR	POWER switch	ON
KY-661/URR	POWER switch	ON
CV-2520(V)/URC	POWER switch	ON

*Use MONITOR SELECTOR switch and LINE-DBM meter to make this adjustment.

For purposes of local checkout in a remote tuning (see paragraph 2-6e, Checkout Procedure) the CV-2520(V)/URC and KY-661/URR modules contain certain indicators. These are a SIGNAL INPUT lamp in the former and a FAULT lamp in the latter. A blinking SIGNAL INPUT lamp indicates code entry into the Storer (but not necessarily into its memory); a steady light indicates no code entry. The FAULT lamp lights when the tuning servo has failed to synchronize the receiver within 15 seconds of reception of the "receiver tune" code. The lamp is combined with a "reset" pushbutton; pushing the button recycles the servo tuning sequence and, in this way, is a parallel control with the remote operator's "receiver tune" button.

During a remote tuning, the local operator will observe front panel switches spinning to their programmed positions. The TN-525/FRR BAND SWITCH, however, will not move, since the band is being selected electrically while the switch is in AUTO position. The TN-525/FRR TUNE knob will spin and can be observed to slow down as the fine tuning adjustment is made. The TN-525/FRR MEGAHERTZ readout will agree with the 0-1510/URR MEGAHERTZ switch settings.

When synchronization has been reached, the TN-525/FRR SYNC INDICATOR lamp will light and the PHASE DIFFERENCE meter will read near-zero-center-scale. (This also applies in a remote AFC tuning, when the receiver has locked with the incoming carrier component.) This synchronization indication and the cessation of knob movement will be an indication to the local observer that the receiver tuning cycle is finished and ready for a possible manual tuning or another remote tuning.

(4) Readback Monitoring - In addition to the "tuning", "ready" and "fault" codes, the readback cycle of codes includes certain receiver control positions. These are:

0-1510/URR 10 MHz, 1 MHz, 100 kHz, 10 kHz, 1 kHz, and .1 kHz switches.

TD-969/FRR AGC TIME CONSTANT switches and MODE switch.

TN-525/FRR FUNCTION switch.

An AFC drift alarm code is also included in the readback, signifying excessive carrier drift from the transmitter, to the point at which the TN-525/FRR AFC hold-in range has been exceeded.

Other readback codes ("decoder power off" and "non-automatic") serve to indicate to the remote operator that the controls have not been properly present for remote control of the receiver. "Decoder power off" signifies that the CV-2520(V)/URC POWER switch is off. "Non-automatic" indicates that the TN-525/URR BAND switch has been set to a position other than AUTO. Included in the readback cycle is a 1-10 code, identifying the receiver in a block of ten receivers.

b. MANUAL CONTROL - Manual tuning of the receiver may be accomplished at any time, either after a remote tuning is finished or during a remote tuning. Manual override of the remote signal is accomplished by setting the CV-2520(V)/URC POWER switch at OFF. If this is done during a remote tuning, any codes remaining in the Storer memory will be erased. However, if a servo frequency tuning is taking place (as indicated by changes in the TN-525/URR MEGACYCLES display), the tuning should be allowed to finish its cycle before manually moving the TUNE knob; otherwise a FAULT readback will be transmitted back to the remote operator.

To maintain a readback of control positions to the remote operator, leave the KY-661/URR POWER switch set at ON. If it is preferred to interrupt the readback, however, set this switch at OFF.

(1) Description of Controls - Refer to table 3-2 and figure 3-1 for description of front panel controls and their functions.

(2) Presetting Controls for Manual Tuning - Ensure that the receiver has had an initial 2-hour warm-up phase for frequency stability, as described in paragraph 3-2a(2). Then set controls as listed in table 3-3.

(3) Sequence of Operation - After presetting controls per table 3-4, determine channel reception mode (ISB or symmetrical) and frequency control mode (synthesized, AFC or local) required. Then proceed to tune the receiver, following procedure in applicable paragraphs of A., B., C., D., E. and F.

A. Synthesized Frequency Control - Set TN-525/FRR FUNCTION switch at SYN, BAND SWITCH at AUTO and set 0-1510/URR MEGAHERTZ switches for 10 MHz, 1 MHz, 100 kHz, 10 kHz, 1 kHz and 0.1 kHz components in carrier frequency. As each MEGAHERTZ switch is moved, receiver will synchronize (in 2-7 seconds) to the new frequency setting; this is indicated by the TN-525/FRR SYNC INDICATOR lamp. It is not necessary to wait for synchronization between switches, however.

B. AFC Control - Tune receiver for carrier component as described in above paragraph (A). Then (when signal input commences) set TN-525/FRR FUNCTION switch at AFC. Observing TN-525/FRR PHASE DIFFERENCE meter and SYNC INDICATOR lamp, hold down TN-525/FRR AFC TUNE switch to obtain center-scale reading on the meter and a steady light from the lamp. Such an indication signifies capture of the carrier component (in the incoming signal) by the TN-525/FRR AFC circuit. When this occurs, immediately release AFC TUNE switch. If, however, the capture does not occur, hold down AFC TUNE switch again and vary TN-525/FRR FINE TUNE knob to obtain capture indication. Release AFC TUNE switch.

C. Local Frequency Control - Set TN-525/FRR FUNCTION switch at LOCAL and BAND SWITCH for appropriate band. Turn TN-525/FRR TUNE knob to bring carrier frequency (down to the .1-kHz component) on TN-525/FRR MC digital display. Monitoring signal at TD-969/FRR by means of TD-969/FRR MONITOR SELECTOR switch, LOCAL

GAIN knob and Speaker LS-588/U, turn TN-525/FRR FINE TUNE knob to bring intelligence on proper channel/s.

D. 4-Channel Sideband Reception - Set TD-969/FRR MODE switch at ISB. Then set SYM-B2, B1, A1 and A2 AGC SOURCE and AGC TIME CONSTANT switches for agc sources and decay speeds giving best results.

NOTE

A SLOW decay speed is preferable for reception of a single keyed tone in a channel. A FAST speed is generally used for multiple keyed tones or voice in a channel. In some cases, a MEDIUM speed may be preferable. Normally, AGC SOURCE switches will be set to feed the AGC signal back into its own originating channel.

E. Triple, Double or Single Channel Sideband Reception - Set TD-969/FRR MODE switch at ISB. Then set AGC SOURCE and TIME CONSTANT switches of channel/s to be received for appropriate source and decay speed. Positions of AGC switches for channels not to be received are optional. If it is required to turn off audio output of channels not to be received, this may be done by setting their LINE LEVEL ADJUST knobs completely counterclockwise.

F. Symmetrical Channel Reception - Set TD-969/FRR MODE switch for AM or CW, depending upon the type of signal to be received, and for 2.5 kHz or 6 kHz, depending upon the width of the transmitted signal. 6 kHz is appropriate for AM; 2.5 kHz is used for CW. In the case of an MCW transmission, set switch at AM 2.5 kHz.

When receiving CW, set SYM BFO switch for audio output tone desired. This may be done by setting the MONITOR SELECTOR switch to SYM and

TABLE 3-4. CONTROL PRESETTINGS FOR MANUAL TUNING, SINGLE RECEIVER

UNIT	CONTROL	SETTING
CV-2520(V)/URC	POWER switch	OFF
TN-525/FRR	INPUT ATTENUATOR switch	down
TN-525/FRR	RF GAIN knob	AGC
TN-525/FRR	SILENCER switch	off (down)
TN-525/FRR	METER FUNCTION switch	RF HIGH
TN-525/FRR	POWER switch	ON
TN-525/FRR	COUNTER MODE switch	REC
TN-525/FRR	LOCK knob	fully ccw
TD-969/FRR	METER SENSITIVITY switch	0
TD-969/FRR	AGC SOURCE switches	SYM-B2 at B2 B1 at B1 A1 at A1 A2 at A2
TD-969/FRR	LOCAL GAIN knob	ccw
TD-969/FRR	LINE LEVEL ADJUST knobs (SYM-B2, B1, A1, and A2)*	0 dbm as indicated on LINE-DBM meter
TD-969/FRR	MONITOR SELECTOR switch	OFF
TD-969/FRR	SYM BFO knob	0
TD-969/FRR	POWER switch	ON
0-1510/URR	PHASE COMPARATOR/FREQ DIFFERENCE switch	PHASE COMPARATOR
0-1510/URR	POWER switch	ON
KY-661/URR	POWER switch	ON

*Use MONITOR SELECTOR switch and LINE-DBM meter to make this adjustment.

turning up the LOCAL GAIN knob for a test tone volume at Speaker LS-588/U. When receiving AM or MCW, position of the SYM BFO knob is optional. Set SYM-B2 AGC TIME CONSTANT switch for appropriate agc decay speed (there is no agc source selection in this channel, since there is only one channel being transmitted).

(4) Indicator Monitoring - After the receiver has been tuned for a particular mode of reception, periodic monitoring of the input and output signals may be performed. For all modes, the RF/AFC LEVEL meter (on the TN-525/FRR) may be used to measure the overall signal strength at the antenna input. To do this, set the TN-525/FRR METER FUNCTION switch to RF HIGH. If the signal is very weak, it may be necessary to set the switch to RF LOW to get a good reading. The meter dial has a separate calibration for each signal. For AFC mode, the METER FUNCTION switch is left at AFC CARRIER position and the meter is used to monitor the carrier component level (in the incoming signal) "captured" by the AFC circuit. If there is an extreme signal fade, the AFC circuit may become ineffective and the tracking action is lost. If the fade is momentary, the AFC will pick up the carrier as it re-appears but, if the fade is extended, a drift may occur and it may be necessary to re-tune the AFC to pick up the strayed signal.

Monitoring the carrier level is therefore advisable, from time to time, when operating on AFC. When the needle falls into the red band on the AFC dial calibration, there is an insufficient level in the incoming carrier to maintain AFC. Loss of AFC will be indicated by a wavering and clipping in audio output tones, when monitored, and the extinguishing of the SYNC INDICATOR lamp. At the point of loss (if it is due to signal drift) the PHASE DIFFERENCE meter needle will move from the center green band to the yellow band and follow the carrier drift up to a ±1 kHz drift (red band) beyond which point (its reading limit) it will return to center abruptly and the SYNC INDICATOR lamp will go out. The center reading, in this case, will not indicate recapture, however, since the SYNC INDICATOR lamp must be on, in addition, to indicate this.

In monitoring for synthesized operation, the PHASE DIFFERENCE meter and SYNC INDICATOR lamp are used again. The PHASE DIFFERENCE meter reads at or near the center and the SYNC INDICATOR lamp is on while the receiver is synchronized and locked to the 0-1510/URR 1-MHz standard. When synchronization is lost for any reason, the SYNC INDICATOR lamp will go out. In synthesized operation of a single receiver, when using an external 1-MHz standard in lieu of the 0-1510/URR standard, the 0-1510/URR includes an automatic switching system to switch in the 0-1510/URR internal 1-MHz standard in the event of the external standard failure. When this happens, the 0-1510/URR EXTERNAL STANDARD FAILURE lamp goes on. This switching and warning system also works in reverse (i.e.: in the event of failure of the 0-1510/URR standard, the external standard is switched in and the INTERNAL STANDARD FAILURE lamp goes on). The 0-1510/URR also includes a FREQUENCY DIFFERENCE/PHASE COMPARATOR meter and switch for monitoring the frequency or phase error between the two standards.

NOTE

When not in use, leave PHASE COMPARATOR/FREQ DIFFERENCE switch in PHASE COMPARATOR position.

In all modes the audio output level of each channel may be monitored by either the TD-969/FRR LINE-DBM meter or a headset at the PHONE jack. Positioning the MONITOR SELECTOR switch connects a particular channel to meter, headset, and speaker output. The LOCAL GAIN knob is used to control the volume of output to the headset and speaker.

(5) Tuning Adjustments - A wide range of manual gain adjustments and individual channel agc adjustments are available by front panel control. Using agc throughout the receiver (with the TN-525/FRR RF GAIN knob at AGC, the TN-525/FRR INPUT ATTENUATOR switch down and the TD-969/FRR channel switches at AGC) the audio output is maintained at a constant* 0 dbm (1 milliwatt across 600 ohms) output level for a wide range of input at the antenna (1 uv to 1 volt). If a different output level is desired, the level for each channel may be increased up to +12 dbm or down to -40 dbm, by means of the TD-969/FRR LINE LEVEL ADJUST control. If manually-controlled gain of the receiver is preferred in lieu of agc, set the TD-969/FRR AGC SOURCE knobs to their "MAN" positions and rotate the TN-525/FRR RF GAIN knob clockwise, past the AGC detent, setting it to the preferred position. The TD-969/FRR channel LINE LEVEL ADJUST knob adjustments may be made also along with this; however, care should be taken in the combination of gain adjustments to obtain the desired output level without distortion or high background noise destroying the intelligence. The agc systems are designed to produce constant output, consistent with the highest signal-to-noise ratio. AGC source in 4-channel modes may be selected by experiment and by monitoring the channel to produce the best agc effect upon each channel; this will depend largely on the particular characteristics of the signal or signals on that channel. For instance, a transmission including a single steady tone on one channel (for the express purpose of agc reference) will make an excellent source for the other channels.

*±1.5 dBm

3-3. SUMMARY OF OPERATING PROCEDURES

a. MANUAL TUNING - Table 3-5 lists a step-by-step manual tuning procedure for a typical 4-channel transmission, with the receiver to operate by synthesized frequency control. The example is for a carrier component of 8.5263 MHz with a number of voice frequency tone telegraph channels transmitted within each of three (B2, B1 and A2) signal channels. A1 channel contains only a steady agc reference tone. Audio level output per channel is to be 0 dbm.

b. REMOTE TUNING - To prepare the receiver locally for a remote tuning, check to ensure that controls are positioned as described in table 3-3.

3-4. OPERATOR'S MAINTENANCE

Operator's maintenance as outlined here consists of practices to be followed during manual operation at the receiver site. Remote operator's maintenance is outlined in the instruction manual for the remote control console.

a. OPERATING CHECKS AND ADJUSTMENTS - Before operating the receiver on synthesized frequency control, check to ascertain that the receiver has undergone a frequency stabilizing warm-up period (as described in paragraph 3-2a(2)). If stabilization has not been reached, it will be noticed in the erratic behavior of the TN-525/FRR SYNC INDICATOR lamp. A steady light, during operation of the receiver, indicates stabilization.

b. EMERGENCY MAINTENANCE - Front panel AC LINE indicator-fuse pairs provide instant notification of a short in the a-c line input to each modular unit. A light in the fuse cartridge holder cap indicates a blown fuse. SPARE fuse holders on each front panel contain spare fuse cartridges for replacement. Figure 3-2 is a fuse location diagram for Receiving Set AN/FRR/-85(V)1. Included with each diagram is a chart listing the functional sections of the receiver protected by each fuse pair and fuse ratings. Power supply circuitry beyond the a-c input, in each modular unit, includes a short-proof feature; therefore, the indicated short can only occur in the a-c input section. Before replacing fuse cartridge, pull out unit on drawer slides and inspect POWER switch wiring and transformer for possible cause.

In the particular event of a given receiver's 1-MHz standard failing the disabled receiver may be referenced to the 1-MHz standard in another receiver by connecting an appropriate cable from 1 MHz EXT STD jack J8, on the faulty receiver, to 1 MHz MONITOR jack J7, on the operative receiver.

3-5. AUXILIARY COUNTER USAGE

As a convenience, the TD-525/FRR front panel includes a COUNTER INPUT jack and COUNTER MODE switch. At times in which the receiver is not in use, the frequency counter in the TN-525/FRR (with its digital MEGAHERTZ display) may be utilized to measure an external 0.1-35 MHz frequency, if its amplitude is between 0.25- and 1.0 VRMS. To do this, set the COUNTER MODE switch at HIGH and connect the frequency to be measured at the COUNTER INPUT jack. Frequency will be displayed to four places beyond the decimal point. To reveal the fifth digit from the decimal point, set the COUNTER MODE switch at LOW. Entire reading will shift to the left, revealing the fifth digit.

TABLE 3-5. TYPICAL MANUAL TUNING PROCEDURE, SINGLE RECEIVER

STEP	UNIT	CONTROL	OPERATION
*1	0-1510/URR	POWER switch	Set at ON. Allow one hour to elapse before proceeding to Step 2.
*2	TN-525/FRR	POWER switch	Set at STANDBY. Allow one hour to elapse before proceeding to Step 3.
3	TN-525/FRR	POWER switch	Set at ON.
4	0-1510/URR	PHASE COMPARATOR/ FREQ DIFFERENCE switch	Set at PHASE COMPARATOR.
5	TD-969/FRR	POWER switch	Set at ON.
6	KY-661/URR	POWER switch	Set at ON.
7	TN-525/FRR	INPUT ATTENUATOR switch	Set in down position.

*If an initial warm-up period has been performed, both switches will be ON and Steps 1 and 2 are unnecessary.

TABLE 3-5. TYPICAL MANUAL TUNING PROCEDURE, SINGLE RECEIVER (cont)

STEP	UNIT	CONTROL	OPERATION
8	CV-2520(V)/URC	POWER switch	Set at OFF.
9	TN-525/FRR	FUNCTION switch**	Set at SYN.
10	TN-525/FRR	RF GAIN knob	Set at AGC.
11	TN-525/FRR	BAND switch	Set at AUTO.
12	TD-969/FRR	MODE switch**	Set at ISB.
13	TD-969/FRR	SYM-B2 AGC SOURCE switch	Set at A1.
14	TD-969/FRR	B1, A1 and A2 AGC SOURCE switches	Set at A1.
15	TD-969/FRR	A1 AGC TIME CONSTANT switch**	Set at FAST. ***
16	0-1510/URR	10 MEGAHERTZ switch**	Set at 0.
17	0-1510/URR	1 MEGAHERTZ switch**	Set at 8.
18	0-1510/URR	0.1 MEGAHERTZ switch**	Set at 5.
19	0-1510/URR	0.1 MEGAHERTZ switch**	Set at 2.
20	0-1510/URR	0.001 MEGAHERTZ switch**	Set at 6.
21	0-1510/URR	0.0001 MEGAHERTZ switch**	Set at 3.
22	TN-525/FRR	MEGAHERTZ display and SYNC INDICATOR lamp	Check figures in display with 0-1510/URR switch settings. Figures should match, display should read 8.5263 MHz and SYNC INDICATOR lamp should be on.
23	TD-969/FRR	Four LINE LEVEL ADJUST switches (SYM-B2, B1, A1 and A2)	Set each for 0 dbm reading on TD-969/FRR LINE DBM meter, using MONITOR SELECTOR switch.
24	TD-969/FRR	MONITOR SELECTOR	Set at OFF.

** Turn clockwise only.
*** Positions of other TIME CONSTANT switches optional.

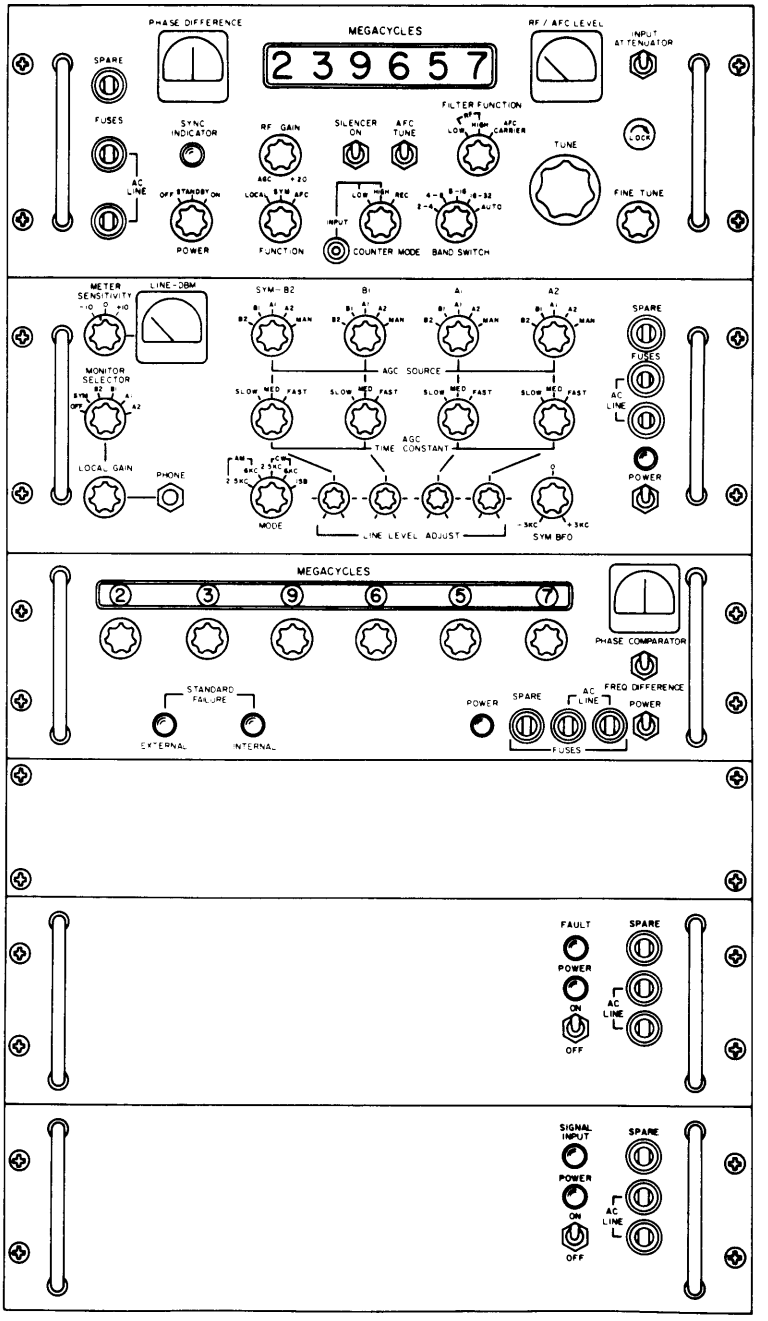


Figure 3-1. Front Panel Controls/Fuse Location Diagram, AN/FRR-85(V)1, Typical Receiver

SECTION IV

TROUBLESHOOTING

4-1. LOGICAL TROUBLESHOOTING PROCEDURE.

a. INTRODUCTION - The procedure described in this section is aimed at directing the troubleshooter to the faulty component, connection or wire by logical choice and in as few steps as possible. The basis for the steps is the structure of the receiver. Each receiver is divided electrically into functional sections and mechanically into modular units in a rack; each modular unit is divided into removable subassemblies (plug-in P/C boards, plug-in stepping switches, etc.). In the troubleshooting procedure, a faulty subassembly can be removed and replaced quickly, placing the Receiving Set back in operation; troubleshooting (and repair) of the removed subassembly can then be continued at a different time or locality if necessary. In troubleshooting a Receiving Set, then, there are seven basic steps to be taken. These are:

1. Symptom recognition.
2. Symptom elaboration.
3. Listing probable faulty functional sections.
4. Localizing the faulty functional section.
5. Localizing the faulty modular unit within the functional section.
6. Localizing the faulty subassembly within the modular unit.
7. Localizing the faulty component within the subassembly.

b. SYMPTOM RECOGNITION - At the first sign of trouble in the receiver, it is important to determine whether or not it is the Receiving Set that is giving the trouble or some associated equipment (i.e.: the remote control site, teletype linkages, audio leads, r-f transmission lines, etc.).

c. SYMPTOM ELABORATION - After it has been determined that the Receiving Set is at fault, the symptom should be examined more closely. Use front panel controls and/or the remote control site keyboard to emphasize the trouble. Table 3-2, Control Functions, will be useful in this step. Note also that there are several modes of operation possible (see paragraph 3-1) involving remote and manual tuning, frequency control, channel reception, and diversity/single receiver operation. It is particularly important in this step to note in which operating mode or modes the trouble is encountered.

d. LISTING PROBABLE FAULTY FUNCTIONAL SECTIONS - Paragraph 4-2, Overall Functional Description, lists and describes the ten functional sections of a receiver (see figure 4-1) and includes table 4-1, Troubleshooting Chart, Local Tuning and table 4-2, Troubleshooting Chart, Remote Tuning. These tables list symptoms-vs.-funtional sections. On the basis of observations made in the previous step, and referring to paragraph 4-2, it should be possible to pick out two or three of the sections that may be the cause of the trouble.

e. LOCALIZING THE FAULTY FUNCTIONAL SECTION - To determine more exactly the faulty functional section from the list made in the previous step, refer to paragraph 4-3, Functional Section Descriptions, under the sub-paragraph heading/s of the section/s. Each of these subparagraphs are further divided into "overall functional section description" (relating to a servicing block diagram of the section) and "overall functional section test data" (relating to test procedure and to waveform/voltage test data found on the servicing block diagram). By using the primary input-vs-output test points on each functional section, it can be determined which one is at fault. Test setups and control positions (for the specific test data given on the servicing block diagram) are included to the left of the diagram.

f. LOCALIZING THE FAULTY MODULAR UNIT WITHIN THE FUNCTIONAL SECTION - In some cases it may be required, by a particular maintenance organization, to remove the faulty rack modular unit and replace it with an overhauled unit, continuing the faulty unit troubleshooting at a different time or locality as a "bench test" operation. For this reason, input-vs.-output test points and values for each modular unit within a functional section are included in the servicing block diagram for the section.

g. LOCALIZING THE FAULTY SUBASSEMBLY OR AREA WITHIN THE MODULAR UNIT - When the modular unit has been discovered, it may be left in the rack for the purposes of "system troubleshooting" or it may be removed for "bench test" troubleshooting. In either case, reference to paragraph 4-3 sub-paragraphs "overall functional section description" and "overall functional section test data" should reveal the faulty subassembly, P/C board, or wiring connection area. Subassemblies may be located by referring to major component location diagrams for each modular unit in Section 5.

It should be pointed out here, that a quick short-cut can be performed in this step, by using spare plug-in subassemblies for a "substitution check" to reveal the faulty one.

TABLE 4-1. TROUBLESHOOTING CHART, LOCAL TUNING

SYMPTOM	FUNCTIONAL SECTION INDICATED
With signal input indicated on TN-525/FRR RF/AFC LEVEL meter, no audio output can be detected.	Signal detection.
With TN-525/FRR RF GAIN knob at AGC, variations in signal input strength as indicated by RF/AFC LEVEL meter produce volume variations at audio output.	Gain control
Varying TN-525/FRR RF GAIN knob does not produce audio level variations.	Gain Control
In diversity operation, audio from the identical channels of receivers A and B cut out at the same time.	Diversity quieter.
In a manual synthesized tuning (with the TN-525/FRR BAND switch manually positioned for the band) the correct figure comes up on the MEGACYCLES display but it is not possible to obtain a "sync" indication.	Synthesizer/phase lock or sync indicator.
Although a successful manual synthesized tuning has been achieved, in an automatic synthesized tuning (with the TN-525/FRR BAND switch set at AUTO) and the correct figure comes up on the MEGACYCLES display, it is not possible to obtain a "sync" indication.	Automatic tuning
In a manual synthesized tuning a "sync" indication is reached but the correct figure is not displayed on the TN-525/FRR MEGACYCLES display.	Digital counter
The receiver has been successfully tuned and synchronized in a synthesized tuning. However, repeated consequent AFC tuning procedures fail to give a "sync" indication (capture of transmitted carrier).	AFC
Some while after a successful synthesized tuning, monitoring the receiver reveals a loss of "sync".	Synthesizer/phase lock or sync indicator
Some while after a successful AFC tuning, monitoring the receiver reveals a loss of "sync".	AFC or sync indicator

TABLE 4-2. TROUBLESHOOTING CHART, REMOTE TUNING

SYMPTOM	FUNCTIONAL SECTION INDICATED
Readback information at the remote control site does not match control positions and status (either totally or partially).	Remote readback
Although remote readback section is working satisfactorily, remote tuning message fails to produce some or all changes at the receiver.	Remote tuning
The equipment selected" readback is not received when the equipment selection code pair is sent.	Remote tuning or Remote readback
Although a blinking SIGNAL INPUT lamp on the Converter-Storer indicates application of teletype codes, there are no changes or incomplete changes in the receiver when the TUNE code is sent.	Remote tuning

h. LOCALIZING THE FAULTY COMPONENT WITHIN THE SUBASSEMBLY OR AREA - When the faulty subassembly has been discovered, it is generally expeditious at this time to replace it from the spares supply. Further troubleshooting of the subassembly may then be performed in a modular unit at a different site or time. For this latter purpose, the technician may refer to paragraph 4-4 "Subassembly Description". The text in sub-paragraphs of 4-4 is divided into subassemblies and these are presented in the reference symbol order of a single receiver. The text refers to sub-assembly schematics in Section 5 and these also include test points. Test data given is based on the same test setup and control position arrangement given on the functional section diagram.

Before starting subassembly troubleshooting, the technician should check the "Notes" column opposite its listing in Section 6, Parts List. Some subassemblies have been categorized by the provisioning agency as "non-reparable" from a practical or cost-wise point of view. In addition, some are recommended to be returned to the factory for repair. In both cases, there should be spare subassemblies available for replacement, eliminating the necessity for any further troubleshooting procedure.

4-2. OVERALL RECEIVER FUNCTIONAL DESCRIPTION.

a. INTRODUCTION - Radio Receiving Set AN/FRR-85 is made up of ten functional sections (see figure 4-1, Overall Functional Block Diagram).

b. SIGNAL DETECTION SECTION - The signal detection section functions as the basic receiver. A 2-32 mc r-f signal, containing a 4-channel sideband, AM or CW transmission, is received at the antenna input. Audio appears at the output in the form of a symmetrical channel (for AM or CW) or four demultiplexed channels (B2, B1, A1 and A2) in a four-channel sideband transmission.

c. GAIN CONTROL SECTION - The gain control section adjusts amplifier gain at the r-f and i-f stages. It may be set manually, at the front panel, or it may be set for AGC (automatic gain control). In AGC mode, a level sensing signal from the 250-kc i-f stage measures the level of the incoming signal and a corresponding d-c voltage is issued to keep the receiver output constant through a wide range of signal input levels.

d. DIVERSITY QUIETER SECTION - The diversity quieter section is utilized only in the AN/FRR-85 Receiving Set. In space or frequency diversity mode, the two receivers are tuned and operated to receive the same signal. The diversity quieter in each receiver samples an individual channel AGC output and like samples from the channel of the associated receiver. The sample representing the weak signal in that receiver initiates a quieting signal back to that receiver's channel audio amplifier stage from its own quieter.

e. SYNTHESIZER/PHASE LOCK SECTION - This section sets the receiver for synthesized operation by locking all receiver frequencies to a 1-mc standard. It has two inputs: (1) a 21-37 mc frequency from the receiver's h-f TUNE oscillator and (2) a signal from the receiver's BAND selector setting. The output is a d-c correction voltage to the h-f oscillator from a phase locking section that automatically locks the receiver to the standard in the final phase of fine tuning. When phase locking has occured, it sends a "sync" signal to the sync indicator section. The synthesizer/phase lock section contains its own 1-mc standard, stable to within one part in $1X10^8$ for a 24-hour period. If a higher external 1-mc standard is available, however, this standard may be used to control the internal one. Electronic automatic switching circuit switches

in the external standard in case of the failure of the internal.

f. AUTOMATIC TUNING SECTION - The automatic tuning section, works with the synthesizer/phase lock section to affect a completely automatic frequency tuning. When the receiver BAND switch is set at AUTO and the digital frequency selection knobs on the synthesizer/phase lock section are set for the desired receiver frequency, BCD (binary coded digit) signals are sent to comparators in the automatic tuning section. These comparators also receive BCDs from the digital counter, representing the present receiver h-f oscillator reading. The comparators then issue a correctional signal to the TN-525/FRR tuning control via a tuning motor drive gear train in a servo loop and a logic circuit issues a band selection signal to electrically select the receiver's band setting. When the servo loop adjusts the tune control within the phase locking range, this circuit synchronizes the receiver to the 1-mc standard in the same manner as for a manual synthesized tuning. -30V input, "virtual ground" and "buffered d-c loop" signals are programmed from the synthesizer phase lock section in such a sequence as to start and stop the automatic tuning at the proper times. A time delay in the automatic tuning section lights a "fault" lamp if synchronization is not reached within twenty seconds.

g. DIGITAL COUNTER SECTION - The digital counter section is a lighted numeral display unit, representing the 2-32 mc frequency for which the receiver is tuned. It displays the frequency to four places beyond the decimal point and works by an actual cycle count of the receiver's h-f (21-37 mc) oscillator.

h. AFC SECTION - The AFC (automatic frequency control) section serves to compensate for signal drift from a relatively unstable (or non-synthesized) transmitter. The AFC section, when properly tuned, locks onto the transmitted carrier at its 250-kc stage. Any deviation in the carrier frequency alters a 250-kc injection frequency in a control loop and (by d-c correction voltage control) alters the r-f oscillator in the signal processing section in a second control loop so as to produce fidelity of audio output. When the AFC section has locked to a carrier, it sends a "sync" signal to the sync indicator section. In order to allow the second loop to act first, the first loop is momentarily opened by the AFC TUNE switch.

i. SYNC INDICATOR SECTION - The sync indicator section doubles for AFC or synthesized frequency control mode, since only one mode is employed at a time. The sync indicator section receives DC voltages from the synth/phase lock and the AFC sections to indicate, by the use of a meter (1M1) and light (1DS1), the phase lock of the HF oscillator in the synthesize mode and the DC voltage locking of the HF oscillator in the AFC mode. The system is "locked up" when the meter indicates and the light is on.

j. REMOTE TUNING SECTION - The remote tuning section receives teletype codes from the remote control site and translates them into the proper form and sequence to tune the receiver. In the frequency tuning phase, the automatic tuning section is energized and employed.

The first codes to arrive are a pair of equipment selection codes (A-E and 1-10, see table 1-3) that open a memory section in a particular receiver. Codes then arrive at the input in pairs, one selecting a receiver control and one positioning it. The memory section stores these codes as they arrive and they remain stored until the "receiver tune" code arrives at the end of the command message. The code control pairs then act to move stepping-switch drives on the receiver controls one-by-one. As each switch homes, it sends back a "switch stopped" signal, initiating the processing of the next code pair for the next control. In the process, the synthesizer digital frequency controls are moved to the desired frequency figure and automatic tuning ensues as previously described. Other code pairs select frequency control mode (AFC/synth), channel reception mode (AM, CW, ISB) and individual channel AGC feedback time constants (fast, medium, slow). A time delay reset pulse is created at the beginning of the tuning cycle to reset the automatic tuning section in the event of a previous "fault" trip.

k. REMOTE READBACK SECTION - The remote readback section supplies a continuous readback of receiver control positions and tuning status to the remote operator. A series of gating pulses issue from this section, one for each receiver control, initiating readback codes representing the stepped positions of the controls. The codes are translated into series teletype format and appear at a keyer output of the remote readback section for teletype transmission. Included in the readback is a receiver status ("tuning/ready/fault") readback derived from continuous information fed into a logic section: a "sync/no sync" signal, a "tune lockup" signal, a "servo stopped" signal and a "fault" signal. "Memory/decoder power off" information is supplied in the readback when the memory/decoder power section is switched off locally and a "non-automatic" signal issues when the receiver BAND switch is not set to AUTOmatic. Either of these two conditions indicates to the remote operator that the receiver is not properly set for a remote tuning. An "AFC alarm" readback is generated when the AFC section loses the transmitted carrier due to excessive transmitter drift. An "equipment selected" readback is generated from the remote tuning section when the memory input has been opened by the correct equipment selection code pair.

l. TYPICAL SYMPTOMS VS. FUNCTIONAL SECTIONS - Tables 4-1 and 4-2 present indicated faulty functional sections from typical symptoms encountered in a local and remote tuning respectively. Local operation performances (table 4-1) should be checked first in order to rule out areas in a remote operation performance check (table 4-2).

4-3. FUNCTIONAL SECTION DESCRIPTIONS

a. SERVICING BLOCK DIAGRAMS - Figures 4-2 through 4-11 are servicing block diagrams for the ten functional sections of a single receiver system, typical for Receiving Set AN/FRR-85. The one exception to the latter is in the remote tuning section; there is one CV-2521(V)/URC Converter-Storer serving both receivers in a Dual Receiving Set. The areas affected by this difference are shown in figure 4-10. Included in all diagrams are pertinent front panel controls to relate their effects on each functional section in a troubleshooting study.

Test points are symbolized throughout figures 4-2 through 4-11 in accordance with the phase of troubleshooting to be performed. These phases are (1) input/output checks of functional sections, (2) input/output checks of modular units and (3) input/output checks of subassemblies. The test point symbol legend is shown in notes on each diagram.

Test data for the Receiving Set falls into two categories: for binary logic circuitry and for communications circuitry. Test data for the former is in timing-chart format and data for the latter is in the form of pertinent waveforms, voltages and frequencies. Waveforms, voltages and frequencies are shown directly on servicing block diagrams; timing charts are shown in seperate illustrations, referenced to the test points shown on the servicing block diagrams. Text in the following paragraphs (pertaining to "test data") refers specifically to timing charts when these are required. In general, these areas are the digital counter, automatic tuning, remote tuning and remote readback sections.

In all cases, text in the following paragraphs under the sub-headings of "test data" should be referred to before taking measurements. The text contains specific control positions and test setup requirements to obtain the specific readings.

b. TEST EQUIPMENT REQUIRED - See paragraphs 5-1a, and 5-2b, for test equipment requirements.

c. USAGE OF TIMING CHARTS - Timing charts (figure 4-12 and 4-13) are categorized by receiver functional sections involving binary logic and subdivided further into phases and modes of these sections. Each line represents a test point time variance between two voltage values and all lines are plotted against a common time base for comparison. Test points are arranged from top to bottom in normal order of checking (from input to output) of a functional section, or subdivision thereof.

Using time bases A and B of the oscilloscope, check test points in pairs (the test point and the one directly below it on the chart) at coinciding pulse edges (voltage changes). This comparison check will reveal, by reference to the P/C board logic/schematic in section 5, the logic network/component to be replaced. To make a measurement, set the oscilloscope for an external triggering mode, with a negative triggering slope and level for a negative-going change and a positive triggering slope and level for a positive-going change. The exact shape of the pulse edge is not an important factor in troubleshooting the binary logic sections. Very often, different attenuator lines into the oscilloscope will produce pulse shape distortions that are not present in the equipment being tested. The critical fact is whether or not the expected voltage changes occur in the polarities are coincidences as indicated on a common time base.

d. SIGNAL DETECTION SECTION (figure 4-2)

(1) Overall Functional Section Description - Heavied lines indicate path of intelligence. RF Tuner TN-525/FRR processes the signal from its 2-32 mc stage to a 250-kc i-f output. The 2-32 mc carrier and sidebands from the antenna are directed to four r-f amplifier band circuits (1A10A3A1 through 1A10A3A4) in tuner assembly 1A10 via input/attenuator 1A11. Tunable band-pass ranges are in octave steps: 2-4mc, 4-8mc, 8-16mc, and 16-32mc. In local tuning, bands are gang tuned with a 2-37mc local oscillator (1A10A1) for the incoming frequency by means of the front panel TUNE control*. Band separation is further accomplished in 1st i-f P/C board 1A9 by using four separate i-f mixers and stages at this point (rather than one mixer and one i-f). The outputs of the difference mixers (.625, 1.25, 2.5, and 5.0 mc) are fed to four separate i-f states. Each stage contains amplifiers and a crystal symmetrical bandpass filter; a high degree of selectivity occurs in this area. The front panel BAND SWITCH (in positions 1 through 4) serves to (a) select one of four band paths from input/attenuator assembly 1A11 through tuner assembly 1A10, (b) select the proper division ratio on HF local oscillator divider P/C board 1A8 to produce the appropriate mixer injection frequency and (c) energize subsynthesizer P/C board 1A6 to produce an appropriate mixer injection frequency. Second i-f P/C board 1A7 functions to convert the selected band frequencies to the second i-f of 250 kc. A further degree of selectivity is gained in a crystal filter (not shown) in the mixer output. Output of the 250-kc carrier and sidebands is then routed to Demultiplexer TD-969/FRR.

Demultiplexer TD-969/FRR may be operated for 4-channel ISB (independent sideband) mode (figure 4-2) or for symmetrical channel mode (figure 4-2A) by positioning the MODE selector switch. In the AM or CW positions the TD-969/FRR will pass the symmetrical channel only; in the ISB position it will pass the four sideband channels only. In the symmetrical mode (figure 4-2A) a further selection of audio detection and channel bandwidth may be made by the MODE switch. When the switch is in one of the AM width positions (2.5 kc or 6.0 kc), the carrier and sidebands are processed in an envelope detector to produce audio at the width selected. When the switch is in one of the CW width

*The 2-37 mc range is repeated for each band.

positions (2.5 kc or 6.0 kc), the tone frequency in a sideband (or the carrier itself) is processed in a product detector, with adjustable BFO injection, to produce audio at the filtered width selected.

In the symmetrical mode, the signal path through the TD-969/FRR then, proceeds through symmetrical IF/AGC P/C board 2A5, where width is selected (at the i-f stage) and over to symmetrical demodulator P/C board 2A4, where a detector is selected. The a-f derived from the detector is adjusted in level by the SYM/B2 LINE LEVEL ADJUST knob and routed out of the receiver via the B2 audio/demod P/C board (2A6). The section of the 2A6 board thus used is made to double for the symmetrical channel and the B2 channel, since only one channel will be coming through at any given time, in accordance with the mode selected by the MODE switch.

In the ISB mode (figure 4-2) the carrier (suppresssed or partial) and both sidebands are applied simultaneously to B2, B1, A1, and A2 channel IF/AGC boards (2A7, 9, 11, 13, respectively). A crystal filter at the input of each board picks out and passes the appropriate band of frequencies on to the appropriate channel audio/demod card opposite it. These boards (2A6, 8, 10, and 12) process the 250-kc sideband channels through product detectors to produce four audio channel outputs from the receiver. Product detectors for the two direct channels (A1 and B1) use a 250-kc injection frequency; detectors for the translated channels (A2 and B2) use 243.71-kc and 256.29-kc injection frequencies to produce the required audio. These four injection frequencies are obtained from subcarrier generator P/C board 2A3.

2A3 board derives the injection frequencies by using the receiver's basic 1-mc frequency source (from RF Tuner TN-969/FRR, see next paragraph). The 1-mc is divided by 100 to produce 10 kc into a keyed oscillator. A 6.29-mc harmonic from the oscillator, selected by a crystal filter, is divided by 1000 to produce 6.29 kc. This 6.29 kc is used as a common injection frequency for a difference mixer and a sum mixer. The other common injection frequency is 250 kc, derived by dividing the 1-mc standard by four. The difference mixer then produces 243.71 kc; the sum mixer produces 256.29 kc.

The position of the RF Tuner TN-525/FRR FUNCTION switch 1A12 acts on a gate in phase detector driver P/C board 1A1A2 to select the receiver's 1-mc basic frequency from two possible sources: (1) a highly stable 1-mc standard from Reference Signal Generator 0-1510/URR (see paragraph 4-3g, Synthesizer/Phase Lock section) or (2) a 1-mc standard of lesser stability located in input/standard P/C board 1A1A1. The latter source is used in tuning for AFC (see paragraph 4-3j) and tuning for LOCAL frequency control.

Tuning circuits for LOCAL frequency control are all contained in the basic signal detection section of the receiver. In this mode, the h-f oscillator (1A10A1) in RF tuner TN-525/FRR is disconnected from any control by the AFC section or the synthesizer/phase lock section.

In IF/AGC P/C boards 2A7, 2A9, 2A11, and 2A13 (in Demultiplexer TD-969/FRR) there are delay equalizers (not shown) associated with the crystal filters in each board. These equalizers function to cancel out the time delay effect through the input filters for frequencies at the extreme edges of each passband, a point particularly critical in high-speed data transmission.

LINE DBM meter 2M1, in Demultiplexer TD-969/FRR, together with MONITOR SELECTOR switch 2S2 and METER SENSITIVITY switch 2S8 are used to adjust and monitor the receiver audio output level for each channel. Adjustment is made by LINE LEVEL ADJ potentiometers 2R2, 2R3, 2R4 and 2R5. A 0dbm reading on the meter indicates a 1-mw output into a 600-ohm line. The METER SINSITIVITY switch extends the reading range on the meter for low or high outputs.

The front panel PHONE jack (2J20) on Demultiplexer TD-969/FRR and LOCAL GAIN potentiometer 2R1 are used for headset or speaker sound monitoring. In this mode, MONITOR SELECTOR switch 2S2 selects the audio channel, to the speaker or headset and the LOCAL GAIN knob regulates the volume.

(2) Overall Function Section Test Data

a) Test Equipment Required:

HP-606B, HF Signal Generator
AN/USM-281A, Oscilloscope
AN/USM-207, Frequency Counter
AN/PSM-4C, VOM
ME-303/U, VTVM

b) Procedure - To test the signal detection section for ISB mode, attach an RF signal generator to the antenna input jack, J8, on the rear interface panel, and terminate audio channels A1, A2, B1 and B2 with 600 ohm dummy loads. Set the receiver controls and signal generator frequencies and amplitudes as shown in the table on Figure 4-2. Perform tests A, B, C and D at 3, 6, 12 and 24 megacycles respectively, referring to the signal frequencies table for points which vary for each test. Use an RF VTVM, sensitive wide band oscilloscope, frequency counter and DC volt meter as required. Since the TN-525/FRR counter mode selector switch is in the "REC" position, the frequency to which the receiver is tuned will be indicated on the receiver counter. Whenever possible, test points on the servicing block diagrams have been used; when test points are not available, extender card pin numbers have been identified. Readings which depend on AFC action should not be hurried; a finite time is required for voltages to stabilize. In general, internally generated injection frequencies should be exact, while signal frequencies dependent on the

external signal generator will depend on the care with which the signal generator is tuned.

To test the signal detection section in the SYMMETRICAL mode, first perform the test of the signal detection section ISB mode. Then refer to figure 4-2A. For the test of the SYMMETRICAL mode, the signal generator at the antenna input is modulated externally by either a 1KC audio signal or a 2KC audio signal, depending on the bandpass being tested, or, for the test of the CW function, the signal generator is unmodulated. The carrier frequency is specified as 18 mcs, but any other frequency in the range of the receiver may be used. Test A refers to 1KC modulation Bandwidth 2.5KC, Test B refers to 2KC modulation, Bandwidth 6KC. Test C refers to the CW mode; the signal generator is unmodulated and the internal beat frequency oscillator determines the output audio frequency.

e. GAIN CONTROL SECTION (figure 4-3)

(1) Overall Functional Section Description - The gain control section encompasses a manually adjusted gain control, an AGC (automatic gain control) and a level meter working from AGC samplings.

The AGC system falls into two main sections: a high-level section in RF Tuner TN-525/FRR and a low-level section in Demultiplexer TD-969/FRR. When used together the two sections keep the output of the receiver constant for a total range of antenna input from 1.0 uv to 1 volt. Attack points are arranged so that for an antenna signal level in the range of 1.0 uv to 500 uv, the TD-969/FRR AGC System is active and the TN-525/FRR AGC system is inactive. When the antenna signal strength increases above 500 uv, the TN-525/FRR AGC system becomes active and joints that of the TD-969/FRR in keeping the audio output constant. At 30 mv antenna input, an AGC overload sensing circuit, in TN-525/FRR 2nd IF P/C board 1A7, switches in a 20-db attenuator in input attenuator assembly 1A11, thereby placing additional control on the signal. An INPUT ATTENUATOR switch (1S2) controls the attenuator when the signal at the antenna is less than 30 mv. In the ON position the attenuator is switched in; in the OFF position, automatic switching at 30 mv takes place.

The AGC system in RF Tuner TN-525/FRR is switched in by setting RF GAIN potentiometer 1R2 to AGC position, actuating a built-in switch. The AGC system in Demultiplexer TD-969/FRR is switched in by setting the AGC SOURCE knobs to a position other than MANUAL.

TD-969/FRR AGC circuits are isolated for each channel and AGC SOURCE control switches are arranged to select channel feedback source and AGC attack-and-decay speeds (TIME CONSTANT) individually for each sideband channel. Each sideband channel may receive its feedback from its own output or from one of the other three sideband channels. AGC controls for the symmetrical channel (see figure 4-3A) select attack-and-decay speed only, since this channel always receives AGC feedback from its own output.

The manually controlled gain for both TN-525/FRR and TD-969/FRR modular units is adjusted by the TN-525/FRR RF GAIN knob, first setting the TD-969/FRR AGC SOURCE switches at MANUAL so as to substitute the adjustment from MANUAL GAIN potentiometer 1R2 for the AGC inputs into the individual channels.

RF/AFC LEVEL meter 1M2 in RF Tuner TN-525/FRR (with METER FUNCTION switch 1S2 in an "RF" position) functions to assist the RF GAIN knob adjustment setting by indicating incoming signal strength. In the RF LOW position of the switch, the meter derives the signal level for a relatively weak signal from a summing of AGC levels from the four separate channel AGC feedbacks in the TD-969/FRR. In the RF HIGH switch position, a relatively strong signal is measured from the AGC output in the TN-525/FRR r-f stage. The AFC CARRIER switch position monitors the level of the "captured" carrier component in AFC operation (see paragraph 4-3j, AFC SECTION).

(2) Overall Functional Section Test Data

a) Test Equipment Required

HP-606B, HF Signal Generator
ME-303/U, VTVM
AN/PSM-4C, VOM
AN/USM-281A, Oscilloscope

b) Procedure - To test the gain control section for ISB mode, attach signal generator and loads to rear interconnect panel as shown in "test setup" diagram included in figure 4-3. Set receiver controls as listed under the diagram. Test AGC system by performing "A", "B", and "C" tests for the three variations in antenna input signal strength indicated (minimum, maximum, and overload). Test manual gain control system by performing "D" and "E" tests (for minimum and maximum gain settings of the TN525/FRR RF GAIN knob); the minimum setting is the extreme counterclockwise position (just short of AGC switch-in) and the maximum is the extreme clockwise position. Refer to "signal variations" table for points that vary with each test. Use an RF VTVM for RF measurements and a DC meter with at least 20,000 ohms/volt sensitivity for the DC measurements.

Test of AGC Time Constant Circuits: See Table 5-1.

f. DIVERSITY QUIETER SECTION (figure 4-4)

(1) Overall Functional Section Description - The diversity quieter section is used in a dual diversity operation of two receivers (AN/FRR-85). All circuitry is located in the Demultiplexer, TD-969/FRR.

Inputs to the diversity quieter system are the five individual channel AGC signals described in paragraph 4-3e. Four AGC comparators in monitor/diversity P/C board 2A2 and diversity quieter in audio/demod P/C boards 2A6, 2A8, 2A10 and 2A12 function as individual channel quieters in a diversity operation. Two AGC levels are compared in each channel comparator, one from each receiver half. The output of the comparator works on the diversity quieter to enable or disable the final amplifier stage in the audio/demod P/C board. If, for example, channel B1 in receiver "A" is receiving a weaker signal than is channel B1 in receiver "B", the diversity quieter in the receiver "A" B1 audio/demod P/C board disables the final amplifier stage and that of receiver "B" remains enabled.

The diversity quieting feature is not required when the AN/FRR-85 is operated in diversity with an external combiner at the audio output. The exchange of AGC signals between receivers is through an interconnecting cable (10W17) running between the two DIVERSITY connectors on the upper and lower interconnect panels at the rear of the rack (see figure 5-1); this cable is removed when the AN/FRR-85 is operated with a combiner. When the receiver is operated in diversity using AGC comparisons, however, the TD-969/FRR AGC SOURCE switches (see paragraph 4-3e, Gain Control Section) must be positioned so that each channel receives its own AGC feedback.

(2) Overall Functional Section Test Data

a) Test Equipment Required

AN/PSM-4C, VOM
AN/USM-106A, VTVM
Two (2) HP-606B, HF Signal Generators

b) Procedure - To test the diversity quieter section, attach a signal generator and loads to receiver "A" and "B" rear interconnect panels as shown in the "test setup" diagram included in figure 4-4. Set receiver controls as listed under the diagram. Test system by performing "A" and "B" tests (for the two combinations of receiver "A" and "B" relative input strength) as indicated. Refer to "signal variations" table for points that vary with each test. Use a VTVM to measure "VAC" and "VDC" points.

g. SYNTHESIZER/PHASE LOCK SECTION (Figure 4-5)

(1) Overall Functional Section Description

A. Receiving Set AN/FRR-85 - The synthesizer/phase lock section involves RF Tuner TN-525/FRR and Reference Signal Generator 0-1510/URR. This section is defined only as that portion involved in a manual tuning (adjustment of the TN-525/FRR TUNE and FINE TUNE knobs and BAND switch) as opposed to the automatic tuning section described in paragraph 4-3h. Although automatic tuning for synthesized frequency control is always used (for its greater convenience) the manual tuning method is described here in order to subdivide this area from automatic tuning section for troubleshooting purposes.

In manual tuning, the operator sets the TN-525/FRR FUNCTION switch at SYN position and the BAND switch at the appropriate band. He then sets the six 0-1510/URR digital frequency switches (10MC, 1MC, 100KC, 10KC, 1KC and 0.1KC) for the desired 2-32mc frequency. (The example shown in figure 4-2 is for 13.4567 mc; frequencies obtained throughout are shown in parentheses.) The tuning is then completed by adjusting the TN-525/FRR TUNE and FINE TUNE knobs until the 21-37mc frequency of h-f local oscillator 1A10A1 is correct for the desired 2-32mc frequency as displayed on the digital counter (see paragraph 4-3i). Illumination of the SYNC INDICATOR lamp on TN525/URR indicates synchronization.

In the final stages of tuning a phase locking circuit takes over to automatically capture and lock oscillator 1A10A1 frequency to the stability of the 1-mc standard in Reference Signal Generator 0-1510/URR.

A monitor/logic circuit (included in 1-mc distributor P/C board 3A3) functions to supply the 1-mc reference frequency, derived either from the internal 1-mc standard (fi) in the 0-1510/URR or an external standard (fe). The 1 mc is applied at three points: (1) phase detector driver P/C board 1A1A2, (2) 100-kc selector P/C board 3A5 and (3) 1-mc selector P/C board 3A3. In 3A5 the 1 mc is divided by ten to produce 100 kc and its harmonics. A harmonic selector in 3A5 selects nine of these harmonics - - 16.1 mc through 16.9 mc - - separated by 0.1-mc steps. 16.0 and 17.0 mc are selected in 3A4 from the harmonics present in the 1-mc input. These 16.0-17.0 (eleven) frequencies are routed to five matrix distributors (contained in 3A6, 3A7, and 3A8) each controlled by one of the front panel frequency switches of the group 1 MC, 100 KC, 10 KC, 1 KC, and 100 CPS (3A14S1 through 3A18S1). Positioning each switch in a 0 thru 9 position has selected (by binary code input) one frequency as indicated by a "test" notation on the diagram. Meanwhile, 1-mc and its harmonics are applied to a 3-6 mc selector in P/C board 3A4. The selector output is controlled by the 10 MC switch (3A19S1) by means of a binary code input. Positioning this switch in a 0, 1, 2, or 3 position selects a 3-, 4-, 5-, or 6-mc output, respectively, from the distributor. 1.4 mc and 11 mc are also selected from the 1-mc frequency in 3A4 to serve as additional injection frequencies for four mixer-divider stages (3A9, 3A10, 3A11, and 3A12). The output from the four stages (14.04567mc in this example) is brought into a plus-mixer with the output from the 3A4 3-6 mc selector (4 mc). The sum (18.04567 mc) is combined in a minus-mixer with the output (16.7 mc) from the 1 MC distributor and the difference frequency (1.34567 mc) is routed to phase detector driver P/C board 1A1A2 in the

TN-525/FRR. (In this manner, the 0-1510/URR may be tuned to put out a 0 - 3.99999-mc range; however, due to the TN-525/FRR 2-32 mc tuning range, it is used here to put out .20000 to 3.20000 mc.) In addition to this, phase detector driver P/C board 1A1A2 also receives the basic 1-mc standard reference from the 0-1510/URR, as previously mentioned. With the TN-525/FRR FUNCTION switch in SYN position, this 1-mc passes through a gate in phase detector driver P/C board 1A1A2 and over to a frequency divider in phase detector P/C board 1A5, converting this reference frequency into 1 mc/16, or 62.5kc. Meanwhile, the 21-37 mc frequency from HF L.O divider 1A8 and input/std 1A1A1, besides going to the digital counter also gets divided into a 262.5-462.5kc frequency in phase detector drive P/C board 1A1A2 and this frequency represents the oscillator setting in phase detector P/C board 1A5. At the same time, the previously mentioned 0.2-3.2mc frequency, representing switch settings in the 0-1510/URR is divided into a 200-400 kc representive frequency in 1A1A2 and this is routed to a difference mixer receiving the oscillator-representive 262.5-462.5 kc. This difference mixer, in effect, compares the 0-1510/URR frequency switch settings (representing the desired frequency) with the instantaneous oscillator setting at that time (representing the present frequency). The difference error represented in the local oscillator, therefore, will appear in the 62.5 kc output of the minus-mixer; in the fine-tuning phase, this error will be represented as a difference in phase when compared to the previously described reference 62.5 kc derived from the 0-1510/URR. The two 62.5 kc frequencies are compared in two phase detectors, #1 and #2. Detector #1 produces a small d-c output as long as there is an error. When the phase difference is exactly 90° (produced by a 90° shifter), the detector output goes to zero volts. This dc-to-0 volts (a) corrects local oscillator 1A10A1 in an electrical correction loop, and (b) brings PHASE DIFFERENCE meter 1M1* to a zero-center-scale reading. The 90° phase shifter acts on phase detector #2 to cause its output to go to a maximum voltage when a null (0V) is issuing from phase detector #1. The maximum voltage (a) de-energizes sync relay 1A5K1, lighting SYNC INDICATOR lamp 1DS1*. (1A5K1 is initially energized by the depleted voltage from phase detector #2 in a "no sync" condition.)

A frequency comparator and a gate in phase detector driver card 1A1A2 prevents a "false lock". Due to the wide tuning range on each band there are instances in which the local oscillator, moving towards the correct frequency, can issue a frequency 62.5 kc below the 200-400 kc derived from the synthesizer; this would also produce a 62.5 kc output to the phase detectors in phase detector P/C board 1A5. The frequency comparator, therefore, compares the 200-400 kc (synthesizer) frequency (f2) and the 262.5 - 462.5 kc (oscillator) frequency (f1) and closes the gate when f2 is greater than f1.

* Part of the sync indicator section, see paragraph 4-3k.

In Reference Signal Generator 0-1510/URR, 1Mc distributor P/C board 3A3 contains circuitry for automatic alternating of 1-mc standard sources (external and internal) in the event of the failure of one of them. When the external standard is used, it is connected at rear interconnect panel jack (6W1) J-10 and the initial effect is that the output of the internal standard (3A1) is phase-locked to the output of the internal standard. Phase locking occurs as the 1 mc (fe) from the external standard is brought to a phase detector for comparison with the 1 mc (fi) from the internal standard. The d-c error from the detector is brought to the internal 1-mc oscillator circuit to correct it (via a temporary memory section, functioning in an external standard failure). The corrected output of the internal standard is then routed to a 1-mc switching logic section. This section is a level sensing and logic system that ensures a 1-mc output through two basic conditions: (1) failure of internal standard and (2) failure of external standard or no external standard used. Working with the 1-mc switching circuitry is a front panel alarm: The STANDARD FAILURE lights (3DS1 and 3DS2). A signal from the fi or fe level detector lights the INTERNAL or EXTERNAL lamp, respectively, when failure occurs.

FREQ. DIFFERENCE/PHASE COMPARATOR meter 3M1 and switch 3S1 are for checking the internal standard against the external standard. With the switch in the PHASE COMPARATOR position, the d-c (representing difference in phase) registers on the meter. With the switch in the FREQ DIFFERENCE position, the d-c correction voltage is disconnected from the internal standard and replaced by a fixed reference voltage, thereby "freezing" the standard. The difference between the two standards is then read as the a-f frequency difference on the meter.

B. Receiving Set AN/FRR-85 - In the space or frequency diversity operation of two synthesized frequency control receivers it is necessary to have a common 1-mc standard for stability reference, although, in frequency diversity, two separate (and different) 0.2 - 3.2 mc frequencies are utilized from separate Reference Signal Generators. By attaching the 1-mc monitor output of receiver "A" to the external input of receiver "B" a common standard is obtained from receiver "A" with a spare (in receiver "B") that will be switched in automatically in the event of the "A" standard failure. If an external standard is then attached at jack 9W1J10 of receiver "A", the external standard becomes the common standard with two spares.

(2) Overall Functional Section Test Data (figure 4-5)

a) Test Equipment Required:

HP-606B, HF Signal Generator
AN/USM-281A, Oscilloscope
AN/USM-207, Frequency Counter
AN/PSM-4C, VOM

b. Procedure - To test the synthesizer/phase lock section, ensure that loads are attached at J7 and J6 on the rear into panel as shown in the "test setup" diagram included in figure 4-5. Set the controls as listed under the diagram. Perform test "A" using the internal 1-mc standard and with no input connection at J10 on the rear interconnect panel.

Test "B" checks the functioning of the 1-mc switching logic and meter 3M1. Attach the signal generator to J10 on the rear interconnect panel and set it for 1.000005 mc. Set the PHASE COMPARATOR/FREQ DIFFERENCE switch at FREQ DIFFERENCE and measure test points 3, 3A, and 3B. Set the switch at PHASE COMPARATOR and slowly bring the signal generator frequency to 1.0000 mc. The meter needle should return to the center of the dial. Attach the oscilloscope at J9 on the rear interconnect panel and, observing the EXTERNAL and INTERNAL STANDARD FAILURE lamps, remove the signal generator; the EXTERNAL lamp should light and there should be no interruption of the 1-mc output as indicated on the oscilloscope. Test "C" checks the "pull-in" functioning of the phase detector.

An external digital frequency counter should be used to measure all frequencies presented with figures beyond the decimal point. Measure amplitudes and waveforms of these frequencies with the oscilloscope.

Other frequencies may be checked with the oscilloscope only; use the VTVM to measure "VDC" points. Waveform and frequency test  is shown in two places in figure 4-5.

h. AUTOMATIC TUNING SECTION (figure 4-6)

(1) Overall Functional Section Description - Modular units involved in the automatic tuning section are RF Tuner TN-525/FRR, Reference Signal Generator 0-1510/URR, and Command Signal Decoder KY-661/URR.

It may be said that phase detector 1A5 is the triggering input to the automatic tuning system. Automatic tuning is energized by setting the TN-525/FRR BAND switch (1S4) at AUTO, the FUNCTION switch (1A12S1) at SYN and the 0-1510/URR MEGACYCLES switches to the new desired frequency. The last adjustment sets up a mismatch between the 0-1510/URR frequency and the current tuned frequency of the TN-525/FRR (as represented on its counter MEGACYCLES display). If the resulting mismatch is over one kc, detector #2, in phase detector 1A5, (a) Disconnects a "virtual ground" signal to motor direction control 4A10 and (b) energizes sync relay 1A5K1 (see paragraph 4-3g, Synthesizer/phase Lock Section)*. The

* If the resulting mismatch is within ±1.5 kc, the phase locking section will correct the local oscillator to this figure without action from the automatic tuning section.

energized 1A5K1 then completes a path for a -30V supply to the coil of servo control relay 4K4. The energized 4K4 (a) connects a +28V supply to servo loop control 4A11, (b) connects the +28V as a reference to the center tap of a direction control coil of a motor in TUNE motor/generator 1A10A4B1, (c) connects a 115 VAC fixed phase supply to a power coil of the motor and (d) connects a 26 VAC reference across a servo feedback generator in 1A10A4B1. The motor control signals (the remaining requirement for the motor action) originates from a digital tuning section.

The digital tuning section (consisting of P/C boards 4A6 through 4A11 in the KY-661/URR) functions to (a) electrically select a band in the TN-525/FRR and (b) supply the motor direction (cw or ccw) and speed controls to bring the TN-525/FRR frequency within the "capture range" of phase detector 1A5. Fine tuning is then accomplished electrically by the phase locking section.

Band selection is derived by the settings of the 0-1510/URR 10 MC and 1 MC switches represented in BCD (binary coded digit) code. From readout wafers on these switches, bits 2 and 1 of the 10 mc code and bits 8, 4 and 2 of the 1 mc code are routed to a band select logic circuit in 4A9. This circuit produces a 4-bit code for each band and the code produces (via band select relays 4K2 and 4K3) a ground signal (derived from the TN-525/FRR BAND switch in AUTO) at the appropriate band select input pin (A, B, C or D) at receptacle 1J4 in the TN-525/FRR. This ground, it will be noticed, parallels the ground derived by manually positioning the BAND switch at one of the four band positions in a manual tuning (see figure 4-2).

Motor direction and control is derived from comparing the mismatch of five of six digits (10 MC, 1 MC, 100 KC, 10 KC and 1 KC) between the 0-1510/URR and the TN-525/FRR in BCD form. For the 10 MC digit, a 2-bit (2 and 1) readout (representing 0-3) from a waver on switch 3A19S1 and a similar readout from the 10-mc digit counter in the digital counter section (see paragraph 4-3i) are introduced to a digital comparator in 4A6. The error output of the comparator is either an "L" (tune lower) or an "H" (tune higher) signal. Likewise for the 1 MC, 100 KC, 10 KC and 1 KC digits, 4-bit codes (representing 0-9) are separately compared with resulting "L" or "H" signals. All the "L" and "H" signals are brought to an error polarity logic circuit in 4A9. The output of this circuit (the "tune direction" output) is either an "H" (tune higher) +2.5VDC signal or an "L" (tune lower) +2.5VDC signal to a search generator in motor direction/control P/C board 4A10. The result from the generator is an a-c constant frequency "search" signal with a phase and amplitude proportional to direction and amount of error, respectively, into an operational amplifier in servo loop control P/C board 4A11. The "search" signal is triggered by the previously mentioned "virtual ground" signal from 1A5 via a one-shot circuit in 4A10. The operational amplifier (triggered by gating signal which, in turn, has been generated

by the "virtual ground") then puts out a motor control signal with a phase and amplitude proportional to direction and amount of error. This a-c signal is connected to a motor control unit in 4A11, via coupling transformer 4T1, and the resulting signal from the motor control unit to the motor in motor/generator 1A10A4B1 causes the motor to move in the prescribed direction at a set speed. The speed is controlled by a "tach feedback" signal from a motor-driven generator in 1A10A4B1. A continuous comparison is made with the amplitude of the "search" signal and a correction is made in the operational amplifier output. When the digital comparator L and H outputs in 4A6, 4A7 and 4A8 all go to "zero error", both L and H outputs from 4A9 into 4A10 go to +2.5V; the TN-525/FRR is, at this point, digitally tuned to match the 0-1510/URR settings down through the 1-kc component. Before this point is reached, however, the phase locking section (with its capture range of ±1.5 kc) joins in to complete the fine tuning phase (down through the 0.1-kc component).

When the phase lock capture range is entered, sync relay 1A5K1 in phase detector 1A5 de-energizes and the "virtual ground" signal appears. The de-energized relay cuts off the -30V supply to the coil of servo control relay 4K4. Capacitor 4C7 (across the coil), however, hold this relay energized for two seconds before it drops out, maintaining the voltage supplies to drive motor assembly 1A10A4 during this interval. Meanwhile, the arrival of the "virtual ground" to the search generator in 4A10 results in a stepped decrease in amplitude in the search signal. This amplitude decrease slows the motor RPM speed for the fine-tuning stage. As in the higher speed, the "tach feedback" holds the motor to the lower speed. In addition, the virtual ground signal is also fed to the output gates of the 4A9 tune direction section, thereby closing the gates and shutting off the tune direction signals.

As phase locking continues, a "buffered d-c loop" signal, connected to 4A10 from phase detector 1A5, decreases towards zero volts. At about the ±2-volt point (phase lock) a "chopper" signal is generated from 4A10, sending the signal to the operational amplifier and the motor movement. Shortly afterwards, the servo control relay drops out, cutting off the motor and generator power supplies. Phase locking of the local oscillator then continues electrically (as described in paragraph 4-3g). When this has been accomplished, the receiver is tuned and locked to the 0-1510/URR frequency settings down through the 0.1-kc component.

During the 2-second delay interval in which servo control relay 4K4 is held energized figure 4-5, an a-c filter in the d-c loop correction line to the local oscillator is used. This is done in order that the correcting action may take place without nullification by any AC, in the final tuning stage. When sync relay 1A5K1 goes into "sync" position, +24V triggers the 2-second time delay circuit in AC filter subassembly 1A13. The time delay energizes a relay (1A13K1) which routes the d-c correction signal through the filter. When the 2 seconds have elapsed, the relay de-energizes and the a-c filter is by-passed.

A "reverse direction" signal is generated when, in rare instances, phase locking does not occur on the first sweep of the tuning mechanism. When the tuning assembly, driven by the motor, encounters the end of its linear travel (at either end), a limit switch (either 1A10A4S1 or 1A104S2) alternates its position, sending a signal to the high/low tune direction section in 4A9 and reversing its current direction output.

In order to prevent a continuous searching in the event of a real fault, a time delay circuit in the KY-661/URR shuts down the automatic tuning after twenty seconds. ("Sync" normally occurs within ten seconds.) A time delay relay (4K1) is normally in its "no fault" position, furnishing the ground return for the previously mentioned -30V through servo control relay (4K4) coil. At the beginning of the tuning cycle (when sync relay 1A5K1 and servo control relay 4K4 become energized) the latter relay extends a ground signal, setting a 20-second time delay circuit located in stepping switch gating P/C board 4A5. Normally, when no fault occurs, a "sync" condition is reached within ten seconds and the ground is removed by the de-energized 4K4, disabling the time delay. In the event of a fault, however, the twenty seconds run out and the time delay circuit trips relay 4K1 into its "fault" position. The tripped 4K1 then (a) cuts off the ground return for the -30V going to the 4K4 coil, (b) connects a ground to the -30V power supply P/C board 4A12, disabling its output and (c) connects a ground return for +12V into front panel FAULT lamp 4DS1, lighting the lamp. The de-energized 4K4 disconnects the fixed phase a-c voltages to the tuning motor, stopping its movement. However, sync relay 1A5K1 remains in its energized "no sync" position. Recycling of the automatic tuning may then be accomplished by pushing a reset button (built into the FAULT light). This results in resetting relay 4K1 into its "no fault" position and 4K1 then reconnects the -30V to the 4K4 coil, re-energizing this relay and reconnecting the motor fixed phase supplies. The motor then resumes movement, guided by the direction signal from the errors sensed in the digital tuning section.

(2) Overall Functional Section Test Data

a) Test Equipment Required

AN/PSM-4C, VOM
AN/USM-281A, Oscilloscope
ME-303/U, VTVM

b) Procedure - To test the automatic tuning section refer to figure 4-6, Servicing Block Diagram, and figures 4-12 and 4-13, Timing Charts. Set receiver controls as listed under "control positions for test" in figure 4-6. This arrangement sets

up a mis-match, with the TN-525/FRR set for 32.0000 mc and the 0-1510/URR set for 02.0000 mc. Automatic tuning of the TN-525/FRR to 02.0000 mc starts when the KY-661/URR POWER switch is set to ON. Refer to paragraph 4-3c for usage of timing chart. It is necessary to reset the KY-661/URR POWER switch to OFF and reset the mis-match for each new pair of measurements. Use VTVM to measure VAC values.

Test "A" tests all points while the TN-525/FRR is being retuned from 32.0000 mc to 02.0000 mc (high-to-low). Test "B" tests only points 20, 22, 24, 26 and 28 while the receiver is retuned from 02.0000 mc to 32.0000 mc (low-to-high).

The "fault" section may be tested by removing the phase detector P/C board (1A5) while tuning is in progress.

i. DIGITAL COUNTER SECTION (figure 4-7)

(1) Overall Functional Description. - The digital counter section is entirely contained as a part of frequency readout assembly 1A1 of RF Tuner TN-525/FRR. The counter section involves part of input/standard P/C board 1A1A1, offset P/C board 1A1A3, gate generator/counter P/C board 1A1A4, BCD decoders 1A1A5Z1 through 1A1A5Z6 and front panel digital display tubes 1A1DS1 through 1A1DS6. There are two basic modes for operating the counter: (1) the "receiver count" mode, in which the counter is used to read out the receiver's tuned frequency as an aid in tuning and (2) the "external count" mode, an auxiliary usage in which the counter is used as a test instrument to read out a direct count of some external frequency. In the first mode, the counter output also acts as an input for the automatic tuning system.

A. Receiver Count Mode. - Figure 4-7 represents subassembly functioning in the receiver count mode; this results from setting the COUNTER MODE switch (not shown) at REC position. The input to this section is the 21-37 mc (Fo) from the local oscillator L.O. divider 1A8. The 21-37 mc range is repeated for each of the four bands. This frequency (representing the frequency for which the receiver is tuned) becomes divided by two and by ten in input/standard 1A1A1 to produce a 1.05 - 1.85 mc frequency (or Fo/20) at the input of a gate in offset 1A1A3. The control for this gate originates from "inverted gate" pulses from a gate generator in P/C board 1A1A4; timing from the generator opens the gate for a period of 200 ms (or 1/5 second) and closes it for a period of 20 ms. This results in a gate output consisting of 200-ms bursts of pulses (or the 1.05 - 1.85 mc divided by five) alternating with 20-ms intervals of a negative d-c voltage. The gated output (now Fo/100 then goes (a) to a second gate and (b) to an offset network. Control the second gate is from the offset network. The output from the second gate goes to a series of band dividers and gates (controlled by the BAND selector switch) and through a norgate to a decade counter in 1A1A4.

The arrangement of the offset network and band dividers in 1A1A3 results in a 200,000-to-320,000-pulse count representing the 2-32 mc frequency for which the receiver is tuned. The offset network tallies off the first 50,000 pulses of Fo/100 and then reverses its output polarity. The reversed polarity opens the second gate and this results in a pulse output from the second gate that is equal to Fo/100 minus 50,000 pulses. Time durations for opening and closing the second gate vary with the incoming 1.05-1.85 mc frequency; the higher frequencies result in shorter time durations. The resulting pulse count output is passed on to the band dividers and their output gates. Outputs from the dividers are controlled by the setting of the BAND switch (a ground opens the divider output gate). A "2-4" setting results in pulses divided by eight; a "4-8" setting divides them by four; an "8-16" setting divides by two; a "16-32" setting bypasses the dividers.

The decade counter in gate generator/counter 1A1A4 transforms the 200,000-3,200,000 pulses into individual BCD outputs representing the six component digits in the receiver's 02.0000 to 32.0000 mc frequency. The counter is made up of six DCUs (decade counter units) and six BCD storage units. Each DCU counts pulses through 1-9 issuing a BCD (binary coded digit) code (for 1-9) at each pulse to a BCD storage unit. At the tenth count it issues a "0" BCD to its storage unit and a "carry" pulse to the next DCU; that DCU then issues the BCD for "1" to its BCD storage unit. When the second DCU counts ten "carry" pulse results in a "0" BCD to its storage unit and a "carry" pulse to the third BCD. This is repeated until all of the 200,000-3,200,000 pulses are counted and stored.

The gate generator in 1A1A4 transfers readouts, at intervals, to the six digital readout tubes. The generator, referenced to the 1-mc standard from phase detector driver 1A1A2 (see paragraph 4-3d, Signal Detection Section) paces off one "count/read" cycle with each inverted gate signal. This 220 ms signal (consisting of the 200-ms "count" pulse and the 20-ms "off" pulse) is the duration of one "count/read" cycle. During the 20 ms pulse, two more pulses issue from the gate generator: a "read" pulse and a "reset" pulse. The read pulse instantly transfers all the BCD codes in the six storage units over to the six BCD decoders. Each decoder then issues a ground signal to an appropriate pin on its associated digital readout tube and a "0-9" digit lights up, heated by the current drawn through it from a +200V supply. The reset pulse resets the offset in 1A1A3 and the six DCUs in 1A1A4 for a new "count/read" cycle. The BCD code is held on each of the BCD decoders (and the "0-9" digit remains lighted in the tube) until the next "read" pulse in the next "count/read" cycle. Because the number of pulses entering 1A1A4 are equal to the cps count in the receiver tuned frequency (Fr) divided by one hundred, the resulting display represents Fr down through the 0.1-kc (100-cps) component.

In automatic tuning (see paragraph 4-3h) five of the same BCD codes transferred to the

decoders (on the "read" pulse) are also transferred to the digital comparators in Command Signal Decoder KY-661/URR. In automatic tuning, the ground applied to 1A1A3 from the BAND switch is replaced by the ground signal contained in the KY-661/URR band select logic signal.

B. External Count Mode. - Figure 4-7A represents subassembly functioning in the external count mode; this results from setting the COUNTER MODE switch at one of the external count positions (HIGH or LOW). The HIGH position presents the count on the digital display to four places beyond the decimal point; the LOW position shifts the entire display to the left, revealing the fifth digit beyond the decimal point.

In the normal external count mode (HIGH), the frequency takes the same path as does the frequency in the receiver count mode with two exceptions: the offset and band dividers in 1A1A3 are disabled. The external frequency (Fx) to be measured is connected at TN-525/FRR front panel COUNTER MODE INPUT jack 1J13, becomes divided by twenty in 1A1A1 and divided by five by the 200 ms pulse coming into 1A1A3. The frequency (now divided by one hundred) is counted in 1A1A4 in the same manner as is the receiver count mode frequency. It represents the count down through the 0.1-kc component. In either external count mode (HIGH or LOW), a ground is extended from COUNTER MODE switch 1S3 to 1A1A1 and 1A1A3, blocking the receiver count signal, disabling the offset and disabling the band dividers.

When the COUNTER MODE switch is set at LOW the frequency into 1A1A4 becomes Fx divided by ten rather than Fx divided by one hundred. This is accomplished by extending a ground connection at pin 22 of 1A1A1, thereby bypassing the divide-by-ten circuit. The switch in LOW also transfers a ground connection from the decimal point light in the 10 mc digital readout tube to a decimal point light in the 1 mc tube. This causes the decimal point indication to shift one place to the left in the display. Because the number of pulses entering 1A1A4 are equal to the cps count in the input frequency (Fx) divided by ten, the resulting display represents Fx down through the 0.01-kc (or 10-cps) component. Since there are only six counting and display units, however, the extreme left-hand digit (representing the seventh digit) does not become counted or displayed.

(2) Overall Functional Section Test Data

a) Test Equipment Required

AN/PSM-4C, VOM
AN/USM-281A, Oscilloscope
AN/USM-207, Frequency Counter
HP-606B, HF Signal Generator

b) Procedure - To test the digital counter section for receiver count mode, refer to figure 4-7, servicing Block Diagram. Set receiver controls as listed under "control positions for test" in figure 4-7. Tests "A", "B", "C" and "D" test the counter for each of the four bands. Use the oscilloscope to measure frequency amplitudes, the digital counter to read frequency and pulse counts and an ohmmeter to read "ground" and "open" points. Refer to timing chart for points as indicated in the block diagram notes.

To test for external count mode, refer to figure 4-7A, Servicing Block Diagram. Set receiver controls as listed under "control positions for test" in figure 4-7A. Tests "A" and "B" test the counter for HIGH and LOW modes.

j. AFC SECTION (figure 4-8)

(1) Overall Functional Section Description - The AFC section functions in two stages: tuning and operating. In the tuning stage, the operator, having previously tuned and locked the receiver to a specified frequency in synthesized mode, switches to AFC and allows the AFC circuit to lock onto the carrier component in the signal. If the transmitted signal is outside the AFC capture range, it may be necessary to de-tune the receiver for capture. In the operating stage, the AFC circuit, having been tuned, commences to track any subsequent drifts in the transmitted signal.

In the tuning stage, the input to the AFC section is the incoming intelligence signal, consisting of a partial or complete carrier component accompanied by upper and lower sidebands. Each sideband contains intelligence, shown here as two tones each. (See Signal Detection Section, paragraph 4-3d.) This signal is sampled at AFC P/C board 1A3 by analyzing the carrier component; the sidebands are stripped off by a narrow bandpass filter (the filter passes 249.925 - 250.075 kc) and the 250-kc carrier component is applied to two phase detectors. The output of a 250-kc variable oscillator is also applied to the detectors via -45° phase shift circuits; the phase shift creates a phase difference of 90° between the oscillator frequency applied to phase detector #1 and that applied to phase detector #2. When there is a frequency error in the 250 kc from the narrow band-pass filter, as compared to the 250 kc from the oscillator, phase detector #1 issues a d-c voltage (d-c correction loop). This voltage contains amplitude and polarity representing the amount and direction of the error, respectively, and this is read on PHASE DIFFERENCE meter 1M1. As the receiver is de-tuned, (by de-tuning the local oscillator) the error becomes progressively smaller until it reaches zero volts, and this is indicated by a zero-center scale reading on the meter (or "sync"). The 90° phase difference in phase detector #2, meanwhile, causes its d-c output to increase as the output of phase detector #1 decreases. When a null is reached in detector #1, detector #2 is putting out its maximum voltage, and this voltage is sufficient to energize lockup relay 1A3K1. The energized 1A3K1 (a) energizes and locks up sync relay 1A3K3 which, in turn, lights SYNC INDICATOR lamp 1DS1 and (b) completes a correction loop (fast d-c loop) back to the 250-kc oscillator and a correction loop via a delay circuit (slow d-c loop) back to the local

oscillator via a-c filter 1A13 (see paragraph 4-3d, Signal Detection Section). Thereafter any frequency deviations in the incoming carrier will be copied by the oscillator, and the AFC circuit is said to be "tuned" or "in sync". During the tuning, front panel AFC TUNE switch is held down, momentarily grounding out the slow d-c loop back to the local oscillator in order to prevent counteraction by that loop while detuning the local oscillator. When "sync" has occurred, the switch is released, so that both loops may act.

In the operating stage, the 250-kc from the oscillator (containing the same frequency deviations as that of the incoming carrier) is applied to subcarrier generator 2A3, to be used as the reference frequency for generating the 250 kc 243.71 kc and 256.29 kc injection frequencies to the product detectors (see paragraph 4-3d, Signal Detection Section). The AFC position of the FUNCTION switch, by means of gate control, blocks the 250 kc derived from the 1-mc source and a divide-by-four circuit. As the injection frequency deviations track with the sidebands entering the product detectors, the resulting audio remains undistorted through transmitter drifts. The fast and slow d-c loops work together to keep the incoming carrier within the limits of the AFC hold-in range (±1kc). The slow d-c loop functions to minimize the excursions of the local oscillator in order that the carrier component entering 1A3 may pass through the narrow bandpass filter (or ± 75 cps pull-in range). Attack times for the fast and slow d-c loops are designed to keep AFC tracking up to a maximum transmitter drift rate of 10 cps per second.

(2) Overall Functional Section Test Data: figure 4-8

a) Test Equipment Required

HP-606B, HF Signal Generator
AN/USM-281A, Oscilloscope
AN/PSM-4C, VOM

b) Procedure - To test the AFC section, refer to figure 4-8, Servicing Block Diagram. A signal generator, unmodulated, is connected at the antenna input to represent an incoming carrier.

Test A checks the overall operation of the system. With the system "lock up" as indicated in TEST A, figure 4-8, various measurements are taken. Test B checks the range over which the AFC will remain locked in.

k. SYNC INDICATOR SECTION (figure 4-9)

(1) Overall Functional Section Description - The sync indicator section is made up of TN-525/FRR PHASE DIFFERENCE meter 1M1 and SYNC INDICATOR lamp 1DS1. The meter and lamp are shared by the synthesizer/phase lock section (paragraph 4-3g) and the AFC section (paragraph 4-3j). Only one of these sections are operative at a given time; the FUNCTION switch SYN or AFC position supplies the -24V power to phase detector 1A5 or AFC 1A3, respectively.

The signals to the meter and to the light are similar for SYN or AFC modes. The signal to the meter is an isolated sample of the polarized d-c correction loop going to the local oscillator and reads zero volts when synchronization has been obtained. The triggering signal to the lamp is +24V and appears when the "capture range" has been entered (just before synchronization).

Meter dial calibrations are in colors to indicate status of synchronization. A reading in the green (central) zone indicates synchronization within the hold-in range. A yellow range reading is a warning that the phase-locking hold-in range is about to be exceeded. A red range indicates loss of phase-lock and, in operating conditions, the phase detector d-c output disappears, the meter needle returns to zero-center-scale and the SYNC INDICATOR lamp loses the +24V supply and extinguishes.

(2) Overall Functional Section Test Data: (figure 4-9)

a) Test Equipment Required

HP-606B, HF Signal Generator
ME-303/U, VTVM

b) Procedure - This section prescribes two separate tests: one for SYN (synthesized) mode and are for AFC mode. Complete directions for the tests are given on figure 4-9.

1. REMOTE TUNING SECTION (figure 4-10)

(1) Overall Functional Section Description

A. Introduction - The remote tuning section for a single receiver involves Signal Data Converter-Storer CV-2520(V)/URC, Command Signal Decoder KY-661/URR and stepping switches located on front panel controls in modular units 0-1510/URR, TD-969/FRR, and TN-525/FRR. A teletype message containing tuning information codes is stored and processed through the CV-2520 (V)/URC and decoded in the KY-661/URR. Drive signals are then issued, one-by-one, to each of the stepping switches and the controls are moved to their positions.

B. Receiving Set AN/FRR-85(V) figure 4-10

1. Code Storage. The Signal-Data Converter-Storer functions to (1) convert the teletype serial pulses in each code into parallel pulses (along a time base) and (2) store them, as they arrive, in preparation for command signals from the Command Signal Decoder. Tuning codes enter the receiver via MEMORY INPUT receptacle (6W3) J4 on the rear rack interconnect panel. Heavy lines in figure 4-10 represent the path of the code. The

5-bit codes are made up of pulses of current from a standard keyed teletype loop and include a "start" pulse at the beginning and a "stop" pulse at the end. Isolation keyer P/C board 5A1 keys a logic voltage in the input of clock timing P/C board 5A2 and also serves to isolate the code inputs of an array of AN/FRR-85(V) Receiving Sets working from a common teletype loop. (Up to fifty Receiving Sets may be operated from a common loop.) Clock timing P/C board 5A2 contains a decade counter circuit that functions as a shift-register with ten shifts per character. The "start" pulse triggers a clock (not shown) in the register. The next five shifts move the first five bits of the character over to parallel shift-register 5A3. The next three shifts give the Converter-Storer the ability to accept transmissions of the 6, 7, or 8 level characters. The final shift is generated from pin E of 5A3 from a flip-flop (part of the decade-counter register in 5A2) and this serves to stop the clock in 5A2. The first five bits of the code become stored momentarily in the 5A3 register and then move, in parallel pulses, to the five bit-memory sections in integrated shift register 5A7. The codes cannot become stored in 5A7, however, until 5A7 receives a "gate control signal" from Shift Tuning Circuit 5A6 (pin T).

The gate control signal is generated by the "equipment selector" codes, (see table 1-3) contained in the first two characters of the tuning message. These first two characters are used for selecting one of a possible fifty receivers working from a common teletype loop input (A-1, B-3, E-9, D-2, etc). In each Signal-Data-Converter-Storer an "X-Y" matrix in 5A3 is individually wired for an A-E letter. Bits 1 and 2-5 of the first correct (or incorrect) character then opens (or does not open) the "A-E" gate. The opening of the "A-E" gate with the first character and the accompanying "common reset" pulse (pin V of 5A3) cause a gate in Z10 of 5A3 to open and a "letters clear" signal to be sent to pin 7 of 5A6. The opening of the "A-E" gate also sets flip-flop Z1 on 5A3. With Z1 set and with the "common reset" pulse (pin V of 5A3) accompanying the second character (signifying the "1-10" selection) a second gate in Z10 will reset the flip-flop Z1 and will send a "2nd character enable" signal to pin W of 5A4 and 5A5, Gating Circuits. Additionally, the code of the second character will cause one or the other of two gates in Z11 of 5A3 to operate, generating either a "RCVR #1-5 SEL" signal (to pin X of 5A4) or a "RCVR #6-10 SEL" signal (to pin X of 5A5). This same code also causes Readback Selector 5A11 to initiate a readback of receiver status from the particular receiver selected.

The 2-5 bits of each character are also sent to both Gating Circuits, 5A4 and 5A5. The operation of both Gating Circuits is similar, but only one operates for a particular program in accordance with "RCVR #1-5 SEL" and "RCVR #6-10 SEL" signals. The receiver selection signal and the "2nd character enable" signal will cause Z-7 on 5A4 or 5A5 to open. The opening of gate Z-7 and the 2-5 bits in the second character will cause a "start tune" signal to be sent to one of the "start tune gates". However, the "start tune gates" will be inhibited until an "E" signal (signifying start tune) arrives at pin K of 5A4 or 5A5. The opening of gate Z-7 and the 2-5 bits of the second character also generate a "letters gate inhibit" signal which is sent to the "A-E" gate via pin Y of 5A3, inhibiting the gate for the completion of the tuning message. The "letters gate inhibit" signal is also sent to 5A6, Shift Timing Circuit (pin D). The "Timer" the releases the "memory input gate control" signal to pin V of 5A7, opening the gates to the "Bit Memory" for the completion of the message (those characters following the first two equipment select characters). The "memory input gate control" signal is also sent to pin N of 5A3 and operates a gate which allows the "1" bits of characters in the rest of the message to be sent to the "Bit Memory" on 5A7. At the same time, 5A6 releases an "equipment selected" signal to stunt relay 5K1, energizing it into its "correct" position. This extends a ground (or "stunt" signal) to each of the other four receivers on the common teletype line at pin 3 of 5A2, closing their respective code input gates. 5K1 also generates an "equipment selected" readback signal for that receiver (4A4 pin H).

With the bit-memory gates set open, the next code to arrive (the first tuning instructions code) becomes stored. The Shift Timing Circuit (5A6) receives "clock pulses" on pin W and "single shift pulses" on pin X for each incoming character. These signals are sent to a gate in Z-11 which generates a "single shift" signal for each character. This signal causes the "Timer" to send a "shift pulse" to pin 6 of 5A7. The "shift pulse" moves the bits of the character in parallel by one position towards the "Bit Memory" output on 5A7. Each successive code is moved into the memory in this manner, moving towards the output to make room for the next code in the input. Maximum capacity of the bit memories is for 32 codes. This continues in this manner until the arrival of the "E" (or "receiver tune") code, at the end of the message.

The "E" code causes a "tune" signal to appear at pin 17 of 5A3. This signal is carried to pin 19 of 5A6 and 5A6 produces an "E" signal at pins S and 5.

A "start tune" signal is then issued to the Decoder. At the same time, the "E" precipitates a series of "fast shift" pulses from pin V of 5A6 to the bit-memory sections in 5A7. This moves all the codes towards the output of the sections. When the first bit #1 arrives at its output, a "monitor" pulse is generated and travels through the monitor gate to pin J of 5A6, stopping the "fast shift" pulses.

It is at this point that the code storage phase is over; the arrival of the "start tune" signal at the Decoder and the five code bits at its input precipitate the next phase: the code transfer phase.

2. Code transfer. The "start tune" signal, into the Decoder, serves to ensure that time delay relay 4K1 is in its "no fault" position, in the event that it has been tripped previously into its "fault" position. This, in turn, ensures that there is continuity for the ground return of the energizing -30V to servo control relay 4K4 in the automatic tuning section. 4K1 also supplies continuity for a "tune lockup" circuit, necessary for the code transfer phase.

Referring to table 1-2, Remote tuning Input Codes, "addressal function" codes (intended to select a receiver control) start with a "1" as bit "1 and "action function" codes (intended to position the control) start with a "0". The remote operator, therefore, programs his message in a series of code pairs, each pair consisting of an addressal function code followed by an action function code. Bit #1 in the code is therefore used for furnishing continuity for bits 2-5 to the correct portion of the remote tuning section. Bits 2-5, in effect a 4-bit code, position the stepping switches.

The stepping switches fall into two main categories: the master stepping switch (4A15S1) and the receiver control stepping switches. An addressal function code moves the master stepping switch to an appropriate position to supply continuity to a selected receiver control for the consequent action function code. The action function code then moves the receiver control stepping switch to its appointed position.

A reciprocating action between the Decoder and the Converter-Storer commences with the first code, drawing each code out of memory, positioning a stepping switch, and drawing the next code out, etc. In the first addressal code, the "1" polarity of bit #1 supplies a ground to the drive wafer (A) pin #3 of 4A15S1, via control gate #1 in 4A5 and SCR (silicon rectifier) diode 4CR3. Bits 2-5 of the code are brought to drive input gating P/C board 4A4 where there are sixteen 4-bit code gates representing sixteen function positions for all of the remote tuning stepping switches. The appointed code gate then opens, and through wafer "A", a notch-homing wafer, supplies a negative pulse to (Z2) gate #1. When the notch lines up with the code gate, Gate #1 closes, the continuity is interrupted and the rotation stops. The polarity at pin 8 of 4A15 then reverses and (via control gate #1 in 4A5) cuts off 4CR3. The reversed polarity from control gate #1 also causes a "memory advance" signal to be sent back to pin U of Shift timing circuit 5A6. 5A6 responds by sending out a "single shift" pulse from pin V to the 5A7 bit-memories and this shifts the next code to the Decoder. The next code, the action function code, contains "0" for bit #1. This causes another control gate (#2 in 4A5) to present receiver stepping switch ground at the annode of SCR 4CR2. This ground is immediately routed (via wafer "C" of 4A15) to the selected receiver stepping switch actuator coil (shown in figure 4-10 as Reference Signal Generator 0-1510/URR 10 MEGACYCLES switch 3A19). At the same time, the 4-bit code at the 4A4 code gates has opened a gate and is supplying a negative pulse through the notch homing wafer in the receiver stepping switch to 4A15S1 wafer "B". When that switch has homed, this wafer sends back a "receiver switch home" signal to gate #2 in 4A5, cutting off 4CR2 and sending the next "memory advance" pulse back to 5A6. The reciprocating action continues until all character pairs are drawn out of memory and the "E" code, stored last in the memory, arrives at the Decoder.

The "E" code brings the remote tuning cycle to a halt by breaking continuities and shutting off the reciprocating signals. Bit #1 of the "E" code (10000) is a "1" and ground is again supplied to 4CR3 and the master stepping switch drive. Bits 2-5 (0000_ open the 4A4 code gate for function position #16 (the 18th consecutive position for 4A15S1) to its position #18. In position #18, continuity for a "tune lockup" circuit furnishing operating voltages to 4A5 gate Z5 is cut off; the continuity has been held by 4A15S1 wafer "G" through function positions 1-15. As a consequence the next "memory advance" pulse is not sent and no more action occurs.

During the code transfer cycle, at each code transfer, a "decoder inhibit" signal is sent from the Converter-Storer to the Decoder, in order to prevent a "memory advance" signal from issuing from the Decoder during a code shift in the memory. The "decoder inhibit" pulse is generated by the "single shift" pulse in 5A6.

At the beginning of the code transfer cycle, a "memory inhibit" signal is sent from the Decoder back to the Converter-Storer teletype code input to prevent more code storage from a successive message while the code transfer is taking place. The "memory inhibit" signal is generated at the setting of the time delay circuit in 4A5. In remote tuning, this time delay circuit is set at the beginning of the code transfer when wafer C of master stepping switch 4A15S1 goes into its "tune lockup" positions (1-15) from its normal position (#18). When the tune lockup interval is finished, the memory inhibit signal is removed.

Automatic (frequency) tuning is precipitated by a remote-controlled changing of any of the 0-1510/URR MEGACYCLES switches. This produces the same change at phase detector 1A5 output as locally moving a MEGACYCLE switch. If the 20-second interval in the 4A5 time delay circuit runs out, either due to a tuning fault or due to the master stepping switch sticking, the time delay circuit (a) trips relay 4K1 into a "fault" condition and (b) removes the "memory inhibit" signal from the code input gate in 5A2, so that a new message may be sent. In this case, a recycling may be had by sending the two equipment selector codes and another "E" code. The "E" code precipitates another "start tune" signal, resetting tripped relay 4K1 back into its "no fault" condition and re-connecting the -30V path to the tuning servo section.

All of the receiver stepping switch drive wafers are the notch-homing type. Some, however, contain more than one notch. These switches use a low number of function positions and time is therefore saved by repeating the notches through one complete revolution, eliminating the need for the switch to perform one complete revolution when going from one setting to another.

3. Clear Code. In the event of a realized error by the remote operator during his message transmission, he may send a "clear" code (before the "E" in sent); this code "erases" all previously stored codes in the 5A7 bit-memory sections. The clear code (11111) produces a "clear" signal from pin 8 of 5A3 to pin 6 of 5A6. 5A6 then emits a series of fast shift pulses to the memory, moving the codes out of 5A7. Since no "E" has been sent, pin E of 5A7 does not produce the monitor signal back to 5A6 to shut off the shift pulses. However, when the next code is sent, the removal of the clear signal at pin 6 of 5A6 stops the pulses. Although the "dumped" codes move into the Decoder, there is no code transfer action since there is no "start tune" signal and, consequently, no tune lockup continuity established.

4. Blank Code. In some types of teletype transmitting equipment it is possible for the operator to inadvertently send a "blank" code. This is a "start" pulse, followed by five "0" bits (or absence of code). A blank (00000) code gate in 5A3, in this case, prevents this code from becoming stoared in the memory. A "blank" signal output from pin 18 of 5A3 works through an inverter in 5A6 to inhibit the usual shift triggering pulse from pin V of 5A2 to pin X of 5A6. Since the preceding code into the memory has not been shifted, the blank code does not become stored.

(2) Overall Functional Section Test Data

a) Test Equipment Required

TT-176, Teleprinter/Keyboard
AN/USM-281A, Oscilloscope
AN/PSM-4C, VOM
DC Loop Supply

b) Procedure - To test the remote tuning section in Receiving Set AN/FRR-85(V), refer to figure 4-10, Servicing Block Diagram, and figures 4-12 and 4-13, Timing Charts. Test input for this section is a teletype code generator attached at pins of the MEMORY INPUT receptacle on the rack rear interconnect panel. The code generator may be either the normal input from the remote operating station or a test teletype code generator. Code inputs for the results shown on the timing chart are stated on the timing chart. The chart is divided into the normal phases encountered in remote tuning with input codes selected to produce the cirtical voltage changes at each point. Set receiver controls for this test as shown in table 3-3. Refer to paragraph 4-3c for usage of timing chart.

To test the remote tuning section in Receiving Set AN/FRR-85, refer to figure 4-10 Servicing Block Diagram for the code storage check and the Decoder section of figure 4-10 for the code transfer check for a typical receiver half. Use figure 4-13, Timing Chart, for the code storage check.

m. REMOTE READBACK SECTION (figure 4-11)

(1) Overall Functional Section Description - The remote readback section for Receiving Set AN/FRR-85 consists of a readback transmitter section in Command Signal Decoder KY-661/URR fed by coded information from readback wafers on the various stepping switches involved in the automatic tuning section (see paragraph 4-3m). Besides readback wafer data, the transmitter receives other information regarding receiver status from relays and switches involved in a remote tuning. In a Dual Receiver the remote readback section for each receiver is identical to the one in the AN/FRR-85 and each section operates independently, transmitting on a separate channel. The following description is for the AN/FRR-85 with reference to servicing block diagram figure 4-11.

Readback transmission is in the form of a continuous cycling of teletype codes representing receiver control positions and receiver tuning status. One cycle of the characters is shown in table 1-4; "character transmission order" is the order in which the codes leave the receiver readback transmitter. Energization for the transmission is in the readback bit shift register 4A3. When power is applied to the KY-661/URR, 4A3 commences and continues to send out a series of

"code shift" pulses to readback code shift register 4A2 after each character is sent. Upon receipt of each pulse, 4A2 sends out a "gating" pulse to a source of readback information, generating a code from that source. The character bits travel through common lines to bit shift register 4A3 where the bits are shifted out in serial pulse teletype form, (preceded by a "start" pulse and followed by a "stop" pulse) to output keyer 4A1.

Referring to table 1-4, it may be seen that character bits representing receiver control positions are contained in bits #2-5 of each character transmission. Characters #2 through #7 also contain additional information, from other sources, in bit #1. In some cases, the information is contained in the bit #1 polarity appearing in the two successive characters. In the case of the 10 mc and 1 mc characters (for example) the gating pulse for 10 mc is routed in two directions: to the 10 mc readback wafer (3A19S1-C) for the 4-bit readout and an inverted pulse to a tuning/ready/fault logic section in drive input gating P/C board 4A4. Four sources of tuning status information are connected to the logic section (tuning/ready, fault/no fault, sync/no sync and tune lockup). The resulting bit #1 polarity (1 or 0) appears at pin 16 of 4A4 and becomes transmitted with bits #2-5 issuing from 3A19S1-C. The 1 mc gating pulse, that follows also splits two ways: to the 1 mc readback wafter and to the tuning/ready/fault logic section. The four sources of information again present bit #1 information. The polarity relationship of bit #1 in the first character compared with that of the second character contains the significant information of the three receiver tuning conditions: tuning, ready or fault.

Characters #8 and #9 contain information only in bit #1. In these two codes, bit #2 is always a "1" in order to prevent the creation of an "E" code (10000). Characters #10 is not used, therefore a blank is sent (00000). This is done to maintain the correct readback order to the remote control station (AN/URA-63).

Character #11 contains information only in bits #2 and #3 for mode switch (2A14S1) position information.

Characters #13 and #13 each readout the combined positions of two controls each, in the group of four AGC TIME CONSTANT switches. The 2-bit code from each switch is directed to the 4-bit common transmission line to be transmitted in one character.

Characters #14, 15 and #16 are not used therefore blanks (00000) are sent as for character #10.

The 17th character in the cycle is a 4-bit code from a wired matrix located in 4A2. This code represents the receiver's identification in a line of ten possible receivers. The matrix is wired individually for each receiver.

The first code to be transmitted, in a cycle, is the "E" code (10000). This serves to reset and synchronize the readback indicator circuit, at the remote operator's control station, for each cycle. The "E" code is generated from pin M of 4A2 (in its first shift) as a single bit #1.

(2) Overall Functional Section Test Data

a) Test Equipment Required

TT-176, Teleprinter/Keyboard
DC Loop Supply
AN/PSM-4C, VOM
AN/USM-281A, Oscilloscope

b) Procedure - To test the remote readback section, refer to figure 4-11, Servicing Block Diagram, and figure 4-12, Timing Chart. Test input for this section is the specific setting of receiver controls designed to test the readback section, in its various modes, and these settings are included on the timing chart. Reading at the output of the section (the READBACK SIGNAL receptacle on the rack rear interconnect panel) may be via the normal readback indicator at the remote control site or by using a standard teletype receiver. For this purpose, specific teletype characters that should appear at the output are entered on the timing chart. Refer to paragraph 4-3c for usage of timing charts.

4-4. SUBASSEMBLY DESCRIPTIONS

a. INTRODUCTION - The following information is to be used in troubleshooting to locate the faulty component or area within a subassembly. Those subassemblies categorized as "non-reparable" or "factory reparable" in the parts list (Section VI) are not described.

Generally, a subassembly functions in one specific receiver functional section and the description is in terms of that functional section. Sometimes, however, a subassembly becomes involved in more than one receiver functional section. In this case, the description is divided into sections.

UNIT #1

b. 1A1A1 INPUT STANDARD

(1) Circuit Description (figure 5-10/5-11) -

A. Signal Detection Section - 1Mc standard Z6 is used as the receiver's basic 1-mc source when the receiver is operated in a local frequency control mode (see figure 4-2 and paragraph 4-3d). In this mode, a ground is presented to pin 15 allowing Q6 to conduct and thus apply B+ to Z6. Amplifier Q7 presents the 1 mc (stable to within 1 x 10^6) at pins 14 and 13.

B. Synthesizer/Phase Lock Section - Driver Q5 and L. O. output buffer Z1A function to clip the local oscillator 21-37 mc frequency (fed in at pins 16 and 17) in preparation for introduction to an external frequency comparator circuit. The output appears at pins 20 and 21.

C. Digital Counter - The greater portion of the circuitry appearing on this P/C board is utilized by the receiver's digital counter section (see figure 4-7 and paragraph 4-3i). The digital counter is operable in three modes: receiver, external high and external low. In the receiver mode, the same 21-37 mc appearing at the output of part A of Z1 (in the synthesizer/phase lock section) is routed through open nandgate Z1B, amplified through parts A and B of Z2 and open nandgate Z3D to become divided by two and then by ten through Z4. The output (21-37 mc divided by twenty) is routed through gates Z5d and Z5c to appear at pins C and D. In the external high mode, an external .1-35mc frequency (to be counted) is introduced at pins 24 and 25, amplified through Q1, Q2, Q3 and Q4 and appears at the input of control gate Z2c. In the external mode, a ground is presented at pin 18 and a high at pin 22; this causes the output of Z1c to go high, opening the control gate Z2c and closing control gate Z1B thereby blocking the local oscillator 21-37mc. The .1-35 mc then progresses via a nandgate Z2D to the same divide-by-20 route used by the 21-37 mc, in the receiver mode. In the external low mode, the .1-35 mc is routed in the same manner as in external high except that divide-by-10 circuit Z4 is bypassed. In this mode a ground appears at pin 22 blocking control gate Z5D and opening the control gate Z5B bypassing the divider.

(2) Test Data - Test data is given for inputs and outputs of each of the described receiver functional sections in servicing block diagrams 4-2, 4-5 and 4-7. Pertinent tests and measurements are presented in Sective V Maintenance.

c. 1A1A2 PHASE DETECTOR DRIVER

(1) Circuit Description (figure 5-12/5-13)

A. Signal Detection Section - The receiver's basic 1-mc source is introduced at pins J and H, amplified through Q6, Q7, and Q8, the output appearing at pins M, F and P.

B. Synthesizer/Phase Lock - The greater portion of the circuitry appearing on this P/C board is utilized by the receiver's synthesizer/phase lock section (see figure 4-5 and paragraph 4-3g). This falls into four categories: a 1-mc selection, a local oscillator divider, a .2-3.2 mc divider and a frequency comparator.

In the 1-mc selection, two 1-mc sources (external and internal) are introduced at pins 5 and J, respectively; ground extensions from an external switch make the selection. When the receiver is in a synthesized frequency control mode, a ground is presented at pin S, enabling Q3; Q3 applies B+ to Q4 and Q5, allowing the 1 mc from pin 5, Q4 and Q5 to proceed into Q6 through Q8. (When the receiver is in a local frequency control mode, the ground is removed from pin S blocking this passage and allowing the 1-mc appearing at pin J to proceed through Q6, Q7, and Q8.) The selected external 1-mc then issues from pins P, F and 10.

The local oscillator divider consists essentially of Z1, Z2 and Z3; these integrated circuits divide the receiver's 21-37 mc local oscillator frequency by 80 and pass it on to an external phase detector via pins W and V.

The .2-3.2 mc divider consists essentially of transistor Q9 and integrated circuits Z7, Z8, Z9, Z10 and Z11; this section divides a reference .2-3.2 mc (appearing at pins 2 and 4) into an appropriate frequency within the 200-400 kc range for use in the external phase detector. Each sequential divider (one in Z9 and two in Z10) divides by two. The final division is selected by the position of the receiver band selector switch; this 4-position switch presents a ground at one of the band selection pins (A, B, C or D). The ground works through system of inverters and nandgates to disable the output of one divider, for bands 2, 3 or 4. For band 1, all the dividers are disabled and the frequency remains undivided. The resulting frequency travels through three nandgates and a filter network to pins 3 and 1.

The frequency comparator consists mainly of Q1, Z4, Z5, Z6 and Q2. There are two inputs to the comparator: f1 and f2. Frequency f1 is the 21-37 mc/80 (or 262.5-462.5 kc) frequency from the local oscillator divider section and appears at pin 9 of Z3 and the base of Q1; f2 is the 200-400 kc frequency from the .2-3.2 mc divider section and

appears at pin 14 of Z11 and the base of Q2. A logic system of inverters in Z4 and nandgates in Z6 control the polarity of pin 8 output of Z5 to pin 1 of the nandgate (200-400 kc control gate) in Z11. If f1 > f2, this output goes positive opening the control gate and allowing the 200-400 kc to proceed to the phase detector; if f1 < f2, the output goes negative and the 200-400 kc is blocked.

(2) Test Data - Test data is given for inputs and outputs of each of the described receiver functional sections in servicing block diagrams, figures 4-2, 4-5 and 4-7. Pertinent tests and measurements are presented in Section V Maintenance.

d. 1A1A3 OFFSET

(1) Circuit Description (figure 5-14/5-15) - The entire offset circuit functions only in the receiver's digital counter section (see figure 4-7 and paragraph 4-3i). The purpose of this circuit (in the receiver mode of operation) is to convert the Fo/20 input into an output of Fr/100, where Fo is the 21-37 mc of the local oscillator and Fr is the 2-32 mc of the receiver. The relationship of Fo to Fr is dependent upon the receiver's 4-position band switch and the formulae are shown in figure 4-7. The Fo/20 (a 1.05- to 1.85-mc frequency) is introduced at pin D and pin 5 of Z15B, a control gate. Controlling the gate is an "inverted gate" positive logic-level pulse lasting for 200 ms (or 1/5 second). During this pulse, pulses that number 1/5 of the normal cps are allowed through the gate and this, in effect, divides the fo/20 by five. The result, Fo/100, is tallied by an "offset" circuit, consisting of dividiers Z16, Z17, Z8, Z7 and Z6, which are arranged in series as to present one pulse at the end of a count of 50,000 pulses. The pulse, issuing from Z6, works through Z14 and Z5 to control a gate (Z15C) at the output of the first control gate (Z15B). This results in an output from Z15C which is equal to Fo/100 minus 50,000 pulses. This is introduced to a section composed of nandgates, inverters and divide-by-two circuits in Z10, 11 and 12 and Z1, 2 and 3 integrated circuits. Depending on the position of a 4-position band-switch in the receiver, a ground is presented at 13, 12 or 11. This closes the paths of all but one of the four to a norgate in Z4. For band 4, the Fo/100 -50,000 pulses are divided by eight; for band 3 they are divided by four; for band 2 they are divided by two and for band 1, the dividers are bypassed and there is no division. The resulting output appears at pin N.

At the end of each count cycle, a nagative pulse appearing at pin M, resets the offset via Z13D.

Bands A and B (pins S and R) are also used in receivers containing a 6-position band switch; these, however, are not utilized in this receiver.

For the external high count mode, the input at pin D is Fx/20, where Fx equals the external frequency being measured. The "inverted gate" pulse succeeds in dividing the Fx/20 by five, making it Fx/100 at pins 6 of Z15. In the external count mode (high or low) a ground is presented at pin 9, disabling the offset section and the band divider section. The disabled offset section holds the second control gate (Z15c) continually open and the Fx/100 proceeds through output nandgate Z4.

In the external flow count mode, the path of the signal is the same as that of the external high mode, except that the input frequency at pin D is Fx/2. This results in an Fx/10 at the output of the first control gate and it is this frequency that appears at pin N.

(2) Test Data - Test data is given for inputs and outputs of the offset circuitry in servicing block diagram figure 4-7. Pertinent tests and measurements are presented in Section V Maintenance.

e. 1A1A4 GATE GENERATOR/COUNTER

(1) Circuit Description (figure 5-16/5-17) - The entire gate generator/counter circuit functions only in the receiver's digital counter section (see figure 4-7 and paragraph 4-3i). It is composed of a gate generator and a decade counter (paced by the gate generator).

The gate generator, using a 1-mc standard frequency as a reference, generates an "inverted gate" pulse, a reset pulse, and a "read" pulse at different intervals during one count cycle; it consists of integrated circuits Z1 through Z6, Z19 through Z22 and transistor Q1. The 1-mc reference is brought in at pin 3 and F. The "inverted gate" pulse appears at pin 9, the "reset" pulse at pin 3 of Z20 and pin 11, the "read" pulse at the collector output of Q1.

The decade counter consists of six divide-by-ten circuits (or decade counter units) Z7 through Z12, and six BCD storage units (latching memories) Z13 through Z18. In the receiver count mode, the function of the counter is to translate the 20,000- to 320,000-pulse input at pin N (representing the receiver's 2-32 mc frequency) into BCD codes for the six digital components in the 02.0000- to 32.0000-mc figure. This is accomplished during one count cycle. The pulses from pin N enter the row of series-connected dividers and, at the end of the count cycle, each divider presents the 0-9 count, in BCD code, to the latching memories. The memories immediately present the same BCD codes at their outputs, and these outputs are maintained until the end of the next count cycle.

In the external count modes, the incoming pulses (1,000-350,000, representing the external .1 to 35 mc frequency) take the same course as that of the receiver count mode. The "fast count" input (at pin J) is not utilized in this receiver.

(2) Test Data - Test data is given for inputs and outputs of the gate generator and the decade counter in servicing block diagram figure 4-7. Pertinent tests and measurements are presented in Section V Maintenance.

f. 1A1A5 INTERCONNECT BOARD, FREQUENCY READOUT ASSEMBLY

(1) Circuit Description (figure 5-8) - Figure 5-8 depicts the entire frequency readout assembly (1A1) and shows the schematic wiring of 1A1A5. 1A1A5 is a P/C (printed circuit) board assembly supplying printed connections between P/C boards 1A1A1, 1A1A2, 1A1A3 and 1A1A4 and providing P/C receptacles (1A1A5) XA1, (1A1A5) XA2, (1A1A5) XA3 and (1A1A5) XA4 for the four boards. Also included in the 1A1A5 assembly are (1A1A5) J1 and (1A1A5) J2 receptacles, (1A1A5) Z1 through (1A1A5) Z6 BCD decoders and (1A1A5) XDS1 through (1A1A5) XDS6 sockets for digital indicators (1A1) DS1 through (1A1) DS6. (1A1) A5J1 and (1A1) A5J2 are receptacles for connections external to frequency readout assembly 1A1.

1A1A5 is of a universal design for compatibility with different requirements, including a receiver (GPR-10) containing two extra lower bands: 0.5- to 1-mc and 1- to 2-mc. Notations "used on GPR-10 only" are for card pin numbers and conductors not used on RF Tuner TN-511/URR.

Each BCD decoder takes the BCD code output for a digit of the count from 1A1A4 and transforms it into a ground signal for one of the "0-9" pins on a digital indicator, lighting that numeral for the period of one count cycle. In (1A1)DS1 and (1A1)DS2 indicators, there is a decimal point light, to the right of the numeral display. Normally the point in DS2 is lit, from a ground presented at pin 25 of 1A1A5J1: in the external low count mode, however, the ground is transferred over to pin 50, lighting the DS1 point.

(2) Test Data - Test data is given for inputs and outputs of 1A1A5 for each of the receiver functional sections involved in servicing block diagrams figures 4-2, 4-5 and 4-7.

g. 1A2 POWER SUPPLY

(1) Circuit Description (figure 5-18/5-19) - Power supply 1A2 converts 35VAC, 13.5VAC, 26-VAC and 220VAC into +24V, +5V, -24V and +200-VDC, respectively. The d-c output voltages are used to supply several of the receiver's functional sections (in part and in whole) as checked:-

Functional Section	Supply +24V	+5V	-24V	+200V
Signal Detection	X		X	
Gain Control	X		X	
Synthesizer/Phase Lock	X	X	X	
Automatic Tuning	X			
Digital Counter (Rec & Ext)		X		X
Digital Counter (Ext only)	X			
Diversity Quieter			X	

In the +24V supply, the 35VAC is rectified through full wave bridge rectifier CR1. This is followed by a series voltage regulator section and a current limiter section. The voltage regulator consists of transistor Q2 followed by an externally mounted (2N3442) current limiting transistor, transistor Q4, diode CR3 and resistors R7, R8 and R9. The output voltage is sampled in the network formed of R7, R8 and R9 and fed to the base of amplifier Q4. This is amplified in Q4 with a reference voltage developed across diode CR3. The output from Q4 is a correction voltage and this is fed back to the base of series regulator 1Q4. The current limiter consists of transistor 1Q4, resistors R4 and R5, and transistor Q3. The current limiter (or short-proof feature) is, in effect, in the common current line that is the base of Q2 and the collector of Q4, in such a way that 1Q4 can only draw a certain amount of current. When the +24V output is shorted, the voltage drop across R4 and R5 turns on switching transistor Q3. Q3 then draws current off of the common line, and this is the current limiting action. By setting potentiometer R4, the maximum current may be set; here it is shown for a 750 ma output.

The +5V and -24V supplies are essentially of the same circuit design, with a voltage regulator and a current limiter in each. The -24V supply has a half-wave rectifier (CR7) in the input, in place of the full-wave type.

The +200V supply only consists of a half-wave rectifier (CR10) in the input, followed by a ripple filter (C19, R28 and R29).

(2) Test Data - Test data for the 1A2 assembly is included in its schematic (figure 5-19).

h. 1A3 AFC

(1) Circuit Description (figure 5-20/5-21) - The greater part of the receiver's AFC section is housed in P/C board 1A3 (see figure 4-8 and paragraph 4-3j). The 250-kc carrier and sidebands enter at pins 3 and 4 and narrow bandpass filter FL1. Transistors Q1 through Q6 form a limiter amplifier chain for the 250 kc carrier from the filter to the two phase detectors. Phase detector #1 is composed of transformer T1, diodes CR9 and CR10, capacitors C36 and C40, and potentiometer R44; phase detector #2 consists of transformer T2, diodes CR11 and CR12, capacitors C44, C62 and C46, and potentiometer R57. The 250 kc oscillator is completely contained in assembly Z4; voltage regulators VR1 and VR2, temperature-stabilizing diodes CR16 and CR17, potentiometer R34 and capacitor C26 form its fine tuner. The 250 kc output goes to the external demultiplexer via driver Q7 and is coupled to the two phase detectors via a +45° - and -45° phase shifter, to produce the 90° phase difference required. The +45° phase shifter is made up of capacitors C37 and C38 and resistors R43 and R45; capacitors C41 and C42 and resistors R50 and R52 make up the -45° shifter. The limiter amplifier input to each phase detector is at the potentiometer wiper. The output of phase detector #1 appears at TP9 and is brought over to a normally open contact of AFC tune relay K2, via operational amplifier

Z2. The output of phase detector #2 appears at TP11; during "sync", this maximum voltage output triggers operational amplifiers Z1 and Z1's output appears at the base of transistor Q10. Q10 provides a ground for the coil of lockup relay K1, causing it to energize. The energized K1 then supplies a ground to the coil of sync relay K3; K3 then connects +24V to the external "SYNC INDICATOR" lamp. Closed contacts on the energized K1 also supply continuity for the d-c correction loop back to 250-kc oscillator Z4 (E MOD input) via source follower Q12 and eventually to the receiver's local oscillator via an R-C time constant network. When the external AFC TUNE switch is used, the ground appearing at pin 7 of 1A3 causes relay driver transistor Q11 to conduct, energizing tune relay K2. During this interval, the closed contacts of K2 ground out the d-c correction loop towards the local oscillator. The time delay circuit of this "slow" loop is composed of capacitors C52, C53 and C54 and resistors R54 and R69.

When AFC is lost, relays K1 and K3 deenergize; K3 then extinguishes the sync lamp and its "alarm" contacts go into alarm position.

(2) Test Data - Test data is given for inputs and outputs of the 1A3 circuitry in servicing block diagram figure 4-8. Pertinent tests and measurements are presented in Section V Maintenance.

i. 1A5 PHASE DETECTOR

(1) Circuit Description (figure 5-22/5-23) -

A. Synthesizer/Phase Lock Section - The greater part of circuitry appearing in 1A5 is utilized by the receiver's synthesizer/phase lock section (see figure 4-5 and paragraph 4-3g). The receiver's 1-mc reference enters at pins B and C, is amplified through transistors Q8 and Q9 and divided by 16 through integrated circuit Z2. The resulting 62.5 kc is brought over to the two phase detectors via a 90° phase shifter section via driver Q7. This 90° section is composed of a + (plus) and a - (minus) 45° phase shifter section. The +45° shifter is composed of capacitors C31 and C32 and resistors R38 and R40; the -45° shifter is made up of capacitors C29 and C30 and resistors R35 and R36. The two 62.5 kc signals, now 90° apart in phase, drive phase detectors #1 and #2 via drivers Q6 and Q5, respectively.

Phase detector #2 is composed of transformer T4, diodes CR5 and CR6, capacitors C34 and C60, resistor R43 and potentiometer R61. Phase detector #1 is composed of transformer T3, diodes CR1 and CR2, capacitors C27 and C59, resistor R32 and potentiometer R20. The 62.5 kc input from the minus mixer into each of the phase detectors is at the potentiometer wiper. The minus mixer is made up of transistors Q2 and Q18, transformer T2, resistors R4, R5, R6 and R8, potentiometer R7 and capacitors C61 and C8. The .2-.4-mc input to the mixer enters at pins 10 and 11 and is brought over to the bases of Q2 and Q18. The .2625- to .4625-mc input enters the mixer via pins 12 and 13, driver Q1 and coupling transformer T1. The output is amplified through transistor Q3 and brought to the potentiometer-wiper inputs of the two phase detectors via drivers Q4 and Q10. The d-c correction output from phase detector #1 is brought out to pins J, M and N via a low-pass filter consisting of capacitors C17, C18, C19 and C20 and resistors R21 and R22. The outpus from phase detector #2 (appearing across potentiometer R61) is brought through a high-gain d-c amplifier consisting of Q11, Q12, Q13 and Q14 to drive sync relay K1 via relay driver Q17. At the "sync" point, the maximum voltage across R61 causes Q17 to provide a return for +24V through K1, thereby energizing K1. K1 then connects +24V to the external SYNC INDICATOR lamp via pin 3.

B. Automatic Tuning Section - The output of phase detector #1 (at pins M and N) is utilized in the receiver's automatic tuning section. This diminishing d-c voltage is connected to operational amplifier Z1. Z1, in this case, functions as a buffer connection of the d-c loop to the automatic tuning section via pins 4 and 5. A "vertical ground" signal from phase detector #2 is also used. This is taken from the collector of Q13 and routed through Q15 and Q16. At the point of sync, the maximum voltage (appearing across potentiometer R61) causes the output of Q16 (pin 8) to go to ground.

During the automatic tuning interval (before "sync" has been reached) sync relay K1 remains deenergized, supplying a switch closure at pins 1 and 2 of 1A5; this furnishes continuity for the -30V required for automatic tuning. Upon sync, K1 energizes and the -30V supply is cut off, halting the tuning process.

(2) Test Data - Test data is given for inputs and outputs of the 1A5 circuitry in servicing block diagram figures 4-5 and 4-6. Pertinent tests and measurements are presented in Section V Maintenance.

j. 1A6 SUBSYNTHESIZER

(1) Circuit Description (figure 5-24/5-25) - The subsynthesizer functions only in the receiver's signal detection section (see figure 4-2 and paragraph 4-3d). The receiver's 1 mc enters at pins R and P of 1A6 and becomes amplified through Q13 and Q14. Integrated circuit Z1 divides the 1 mc in half and the resulting 500 kc (and harmonics) are routed to four band-divider sections. Each section has a fine-tuned circuit to select a harmonic, a divider and a band logic signal input. The receiver's band switch produces a ground (for the band selected) at one of the band logic inputs (a switching transistor) enabling that band-divider section and disabling the other three. In the band 1 section, the harmonic selected is 7 mc. Z6 divides the signal by four (into 1.75 mc) and Z5 divides the 1.75 mc by two (or into .875 mc). In band 2, the harmonic is 3 mc, the division (through Z4) is by two and the result is 1.5 mc. In band 3, the harmonic is 5.5 mc, the division (through Z3) is by two and the result is 2.75 mc. In band 4, the harmonic is

10.5 mc, the division (through Z2) is by two and the result is 5.25 mc. The common output from 1A6 appears at pin 10, via output driver Q27.

(2) Test Data - Test data is given for inputs and outputs of the 1A6 circuitry in servicing block diagram figure 4-2. Pertinent tests and measurements are presented in Section V Maintenance.

k. 1A7 SECOND IF

(1) Circuit Description (figure 5-26/5-27)

A. Signal Detection Section - The top portion of the 1A7 schematic is used in the receiver's signal detection section (see figure 4-2 and paragraph 4-3d). The balanced minus mixer is made up of field-effect transistors Q1 and Q2, resistors R3, R5 and potentiometer R4. The input from the subsynthesizer (pins 11 and 12) is coupled to the mixer via transformer T1, resistors R1 and R2 and capacitors C2 and C3. The input from the first i-f amplifier (pins 13 and 14) is via coupling capacitor C1. The mixer output is the difference frequency of 250 kc and sidebands. This is routed through band-pass filter FL1 to an amplifier chain composed of transistors Q3, Q4, Q7, Q9, Q10 and Q11 and out of 1A7 at pins J and K.

The middle row of transistors work for noise suppression. When an external switch is set for noise suppression, the +24V is connected to pin 15 of 1A7; this activates a noise detector circuit. The circuit, composed of transistors Q12, Q13, Q14, Q15, Q16 and Q17, samples the mixer output via resistor R8 and capacitor C30. The output is coupled through transformer T4 to the noise gate section. This section is composed of transistors Q18, Q19, Q21, Q23 and Q24. The gating output (TP14) is fed to the center tap of T2, in such a way as to cut out the signal during the brief interval of a noise "spike".

The noise detector gage triggering level is adjustable to various conditions that may exist in an environment. A sample of the detector output is taken from the emitter of Q17 and brought, through potentiometer R74 to d-c amplifiers Q20 and Q22. The output of Q22 is fed back to the input of the noise detector transistor bases. This furnishes an adjustment (at R74) for the operating level of the detector.

B. Gain Control Section - The bottom row of transistors (on the schematic) function as a major part of the receiver's high level automatic gain control section (see figure 4-3 and paragraph 4-3e). The agc detector is composed of transistors Q32, Q33, Q34, Q35 and Q36. The signal sampling is brought into the base of Q32 from the signal detection section output via drivers Q29 and Q30. The detector feedback output is switched into the system via the receiver's agc switch which closes pins C and N of 1A7. With this closure, the feedback is connected (a) to the I. F. amplifier chain via Q8 and (b) to the external r-f amplifier section through pin H of 1A7.

The agc attenuator sensing section is composed of transistors Q41, Q38, Q39 and Q40. Its input is from the agc detector output and its output is to the receiver's attentuator insertion relay in the r-f section, via pin E of 1A7. When triggered at its input (at the base of Q41) the output goes to ground energizing the external relay located in 1A11.

The agc detector also furnishes the input for the receiver's signal strength meter (for a high level signal). This is taken off of the detector output and routed to the external meter via transistor Q37 and pin B of 1A7.

Manual gain control of the receiver is accomplished by a front panel adjustment of a potentiometer external to 1A7. This is a 3-part potentiometer connected to 1A7 in such a way as to adjust the gain setting of two points in the signal detection section amplifier chain and to adjust the gain setting of the external demultiplexer. The positive d-c voltage at pin 10 of 1A7 is adjusted through the first part of the pot and brought back through pin M to regulate the amplifier chain via emitter bypass attenuator Q5. The positive and negative voltages at pins 3 and 2, respectively, are brought out to the third part of the pot and the wiper is connected to pin N. This manually adjusted gain voltage input then takes the same path as the aforementioned agc detector output (to the amplifier chain via Q8). The positive voltage at pin 4 is brought out to the second part of the pot and brought back in at pin F and then to d-c amplifier Q31 to furnish the manually adjusted gain for the demultiplexer, via pin 6 of 1A7.

C. AFC Section - A sample of the output of the signal detection section 250kc amplifier chain is brought out for the AFC section of the receiver. This output is buffered through transistors Q27 and Q28.

(2) Test Data - Test data is given for inputs and outputs of 1A7 in servicing block diagrams figures 4-2, 4-3 and 4-8. Pertinent tests and measurements are presented in Section V Maintenance.

l. 1A8 LOCAL OSCILLATOR DIVIDER

(1) Circuit Description (figure 5-28/5-29)

A. Signal Detection Section - The circuitry in 1A8 functions primarily in the receiver's signal detection section (see figure 4-2 and paragraph 4-3d). The 21-37 mc signal input from the receiver's local oscillator enters at pins 3 and 4 of 1A8. Amplification takes place through transistors Q1, Q2 and Q3. The signal then proceeds through a nandgate combination (Z1) that functions as a distribution amplifier. From there it is routed to four band-divider sections, each with its own output. Each section has a band logic signal input. The receiver's band switch produces a ground (for the band selected) at one of the band logic inputs enabling that band-divider section and disabling the other three. Z2, Z3 and Z4 are divide-by-two integrated circuits.

Z1 is in the input of band 4, Z2 is in the input of band 3 and Z3 is for band 2; band 4 does not use a divider in its input. When, for example, band 1 is selected by the band switch, the 21-37 mc becomes divided through all three dividers (or divided by 8) to become a frequency in the 2.4625- to 4.625-mc range. The inputs to the output band sections for bands 2, 3 and 4 are blocked and all three dividers are enabled. If band 2 is selected, the ground signal at pin M of 1A8 disables divider Z4 so that only Z2 and Z3 dividers are operating; and the same signal enables the band 2 output circuitry only. The 21-37 mc then becomes divided by four and issues as a frequency in the 5.25- to 9.25-mc range. For band 3, in the same manner, the 21-37 mc becomes divided by two and becomes a frequency in the 10.5- to 18.5-mc range. When band 4 is selected, all 3 dividers are disabled and there is no division of the 21-37 mc at the band 4 output.

B. Digital Counter Section - The amplified 21-37 mc (issuing from transistor Q3) is also utilized by the receiver's digital counter section. This output appears at pins 2 and 1 again, via nandgate distribution amplifier Z1.

(2) Test Data - Test data is given for inputs and outputs of 1A8 in servicing block diagrams figures 4-2 and 4-5. Pertinent tests and measurements are presented in Section V Maintenance.

m. 1A9 FIRST IF AMPLIFIER

(1) Circuit Description (figure 5-30/5-31) - The entire circuitry of 1A9 is used only in the receiver's signal detection section (see figure 4-2 and paragraph 4-3d). There is separate circuitry for each of the receiver's four bands; however, only one band circuitry is enabled at one time. This is dependent upon the position of the receiver's band switch. A selected band places a ground on one of the band logic input pins (P, N, E or J); this enables that band circuitry. All bands share a common output path: pins 5 and 6 of 1A9.

Taking band 1 as a typical example, the frequency in the 2-4 mc range (from the r-f tuner) comes into the balanced minus mixer at pins 15 and 5 of 1A9; the injection frequency (from the local oscillator divider) comes in at pins 14 and 5. The minus mixer consists of transformer T1, field-effect transistors Q3 and Q4, resistors R4, R5, R6, R7, R8 and R10, potentiometer R9, and capacitors C6 and C7. The difference output, always .625 mc, is passed through a highly selective crystal-centered bandpass filter (FL1), with a width of about 12 kc. The .625 mc signal is then amplified through field-effect transistor Q5 and issued through buffer amplifier Q6.

(2) Test Data - Test data is given for inputs and outputs of 1A9 in servicing block diagram figure 4-2. Pertinent tests and measurements are presented in Section V Maintenance.

n. 1A11 INPUT/ATTENUATOR

(1) Circuit Description (figure 5-33/5-34) - P/C card 1A11 contains the RF attenuator and pre-filter circuitry for the TN-511/URR. Incoming RF enters 1A11 and is routed to a normally-closed contact (pin 3) of relay 1A11K13, which, in its normally-deenergized state, bypasses the RF attenuator circuitry and directs the signal into the RF pre-filter circuits via a bank of pre-filter selector relays. Attenuator relay 1A11K13 is energized by a virtual ground supplied by external relay driver circuitry and/or a manual attenuator switch. When energized, 1A11K13 routes incoming RF through a resistive T-pad attenuator consisting of resistors 1A11R1, -R2, and -R3, before passing the signal on to the pre-filter selector relays.

After leaving the attenuator relay circuitry, the incoming signal appears at a bank of four pre-filter selector relays. One of these four relays (1A11K1, -K2, -K3, and -K4) will apply the signal to the input of one of four low-pass pre-filters, depending upon the band selected. Since all four pre-filters are identical in principle of operation, a detailed description of one such pre-filter will serve as a model for all four.

Consider Band 3 (8-16 MHz) selection: RF from the attenuator relay appears at a normally-open contact (terminal 1) of DPDT relay 1A11K3. Upon selection of Band 3, a low logic level (near-ground potential) is applied to terminal 7 of 1A11K3, causing it to energize, thereby connecting terminal 1 to terminal 2, and connecting terminal 4 to terminal 5. The results of connecting terminals 1 and 2, and terminals 4 and 5 are the following: (1) Incoming RF is routed from terminal 1 out through terminal 2 to terminals 1 and 6 of DPDT relay 1A11K9; (2) Simultaneously, a ground is supplied to terminals 7 (coils) of DPDT relays 1A11K9 and -K10, thereby enabling them to energize, if a suitable energizing voltage is also present. The conditions under which this voltage is applied will be explained shortly. Continuing with signal flow: RF appears at terminals 1 and 6 of relay 1A11K9. In its de-energized state, terminal 1 of 1A11K9 is open, and terminal 6 is connected to terminal 5. This routes RF from terminal 6 out through terminal 5, through Band 3 pre-filter section "B" (1A11A3), to terminal 5 of relay 1A11K10. When de-energized, terminal 5 of 1A11K10 connects to terminal 6, thereby routing pre-filter output out of the card as Band 3 RF output.

Note that each pre-filter is composed of two sections, labelled "A" and "B"; all "A" sections are mounted directly on card 1A11, while all "B" sections are subassemblies mounted "piggyback" on 1A11. In order to maintain optimum low-pass filter characteristics while minimizing attenuation of desired signals, two pre-filter sections are used per band: The "A" section covers the lower portion, and the "B" section covers the upper portion of each band. Switching between sections (in the Band 3

example) is accomplished by relays 1A11K9 and -K10, and occurs at the approximate geometric mean point of the band(in the case of Band 3, this point is near 11.3 MHz). Recall that it was previously mentioned that these switching relays would energize when suitable voltage was present at their coils: This energizing voltage is applied by means of a microswitch mounted on the tuner assembly, and actuated as the TN-511/URR is tuned past the geometric mean point (11.3 MHz, for Band 3). Note that both relays are of DPDT configuration, so that both input and output of the pre-filter are simultaneously switched over, thus minimizing loading by the unused pre-filter section. Also note that both input and output of an unused pre-filter section are grounded, to avoid undesirable stray capacitive effects.

Approximate crossover points for each band are as follows:

Band 1	2.83 MHz
Band 2	5.65 MHz
Band 3	11.3 MHz
Band 4	22.6 MHz

(2) Test Data - Test data for 1A11 are found within Servicing Block Diagram, figure 4-3; additional pertinent information is contained within figure 4-2.

o. 1A13, AC FILTER (figure 5-36/5-37)

(1) Circuit Description (figure 5-35) - AC filter card 1A13 improves reliability of the DC loop produced in the synthesizer/phase lock section, by eliminating the possibility of oscillator instability due to stray AC pickup.

1A13 has four inputs: (1) +24 VDC (terminal E1) sync trigger signal (applied upon successful phase lock); (2) +24 VDC B+ (terminal E4); (3) DC loop (terminal E5); (4) DC loop common (terminal E2). Inputs (3) and (4) are also the only outputs of 1A13, appearing at terminals E6 and E3, respectively.

Consider the conditions before and after achievement of phase-lock:

Before phase-lock is achieved, the following inputs are presented to 1A13: E1, no input; E2, common side of DC loop; E4, +24 VDC B+; E5, a positive or negative correction voltage of variable amplitude, depending upon direction and magnitude of frequency error.

With no input at terminal E1, transistor 1A13Q1 is biased off; consequently, there is no path to ground for +24 VDC on the coil of DPDT relay 1A13K1, and the relay is de-energized. In the de-energized state, 1A13K1 does the following: (1) places a short circuit around the resistor-capacitor filter network consisting of 1A13C2, -C3, and -R3; (2) places a short circuit around loop series resistor 1A13R4. The filter network is not enabled at this time, because to do so would significantly impair loop response speed.

Upon achieving phase-lock, however, +24 VDC sync trigger appears at terminal E1; simultaneously; loop voltage (terminal E5) goes to zero. All other inputs remain as they were before phase-lock.

The application of +24 VDC to terminal E1 begins charging 40 uf capacitor 1A13C1 through 100 K resistor 1A13R1: the time constant of this RC pair is approximately two seconds. After two seconds, the voltage across 1A13C1 is sufficient to saturate transistor 1A13Q1, thereby providing a path to ground for the coil of relay 1A13K1, allowing it to energize.

When 1A13K1 energizes, it: (1) removes the short circuit from 12 K resistor 1A13R4, placing it in series with the DC loop, between terminals E5 and E6; (2) removes the short circuit from the resistor-capacitor combination of 1A13C2, -C3, and R3, placing this filter network across the DC loop, immediately after 12 K series resistor 1A13R4. 1A13R4 raises the loop impedance to a value suitable for use by the filter network.

Note that once the filter is connected to the loop, response speed of the loop drops somewhat. Although speed of response was critical during the automatic tuning process, once the tuner has achieved and maintained phase-lock such speed is no longer necessary.

Should phase-lock be lost, the +24 VDC sync trigger will disappear from terminal E1, and diode 1A13CR1 will effectively short-circuit timing resistor 1A13R1, allowing timing capacitor 1A13C1 to discharge almost immediately. Transistor 1A13Q1 will therefore quickly cease conduction, de-energizing relay 1A13K1, thereby removing the filter network from the loop, and returning the loop to full response speed. The purpose of the two-second time delay in relay activation is to prevent relay chattering under marginal phase-lock conditions tions.

(2) Test Data - Test Data for Low Pass Filter card 1A13 are contained within figure 4-5 (Servicing Block Diagram, Synthesizer/Phase-Lock Section).

UNIT 2

p. 2A1 POWER SUPPLY

(1) Circuit Description (figure 5-43/5-44) - Power supply 2A1 converts 35 VAC, 21 VAC, 13.5 VAC and 26 VAC into +24V, +15V, +5V and -24V, respectively. In the +24V supply, the 35 VAC is rectified through full wave bridge rectifier CR1.

This is followed by a series voltage regulator section and a current limiter section. The voltage regulator consists of transistor Q2 followed by externally mounted power amplifier transistor Q101, transistor Q4, diode CR3 and resistors R7, R8 and R9. The output of transistor Q101 is sampled in the network formed of R7, R8 and R9 and fed to the base of comparator Q4. This is compared in Q4 with a reference voltage developed across diode CR3. The output from Q4 is a correction voltage and is fed back to the base of series regulator Q2. By setting potentiometer R8, DC output voltage may be set. The current limiter consists of transistor Q1, resistors R4 and R5 and transistor Q3. The current limiter (or "short-proof feature") is, in effect, in the common current line that is the base of Q2 and the collector of Q4 in such a way that the base of Q2 can only draw a certain amount of current. When the +24 V output is shorted, the voltage drop across R4 and R5 turns on switching transistor Q3. Q3 then draws current off of the common line, and this is the current limiting action. By setting potentiometer R4, the maximum current may be set; here it is shown for a 600 ma output.

The +15V, +5V and -24V supplies are essentially of the same circuit design, with a voltage regulator and a current limiter in each.

(2) Test Data - Test data for the 2A1 assembly is included in its schematic (figure 5-44).

q. 2A2 MONITOR/DIVERSITY

(1) Circuit Description (figure 5-45/5-46)

A. Signal Detection Section - The amplifier section for receiver audio monitoring is included in the 2A2 circuitry (see figure 4-2 and paragraph 4-2b). This section is isolated from the receiver audio line output so that the monitoring will have no effect on the signal output. The audio is brought in at pin 13 to amplifier circuitry consisting of Q1 through Q6. The output at pins 12 and 13 drives the speaker.

B. Gain Control Section - Signals from the receiver's low-level agc system are used to obtain the receiver's low level signal strength reading (see figure 4-3 and paragraph 4-3e). Samples of agc feedback from i-f channels SYM, B2, B1, A1 and A2 are brought into a level summing network at pins 3, 4, 5, 6 and 7, respectively. The summing network consists of transistors Q12, Q13, Q14, Q15 and Q16. The output, through diodes CR19 and CR20 is amplified through operational amplifier integrated circuit IC5 and appears at pin S of 2A2.

C. Diversity Quieter Section - The agc comparator circuits for the receiver's diversity quieter section are included in P/C board 2A2 (see figure 4-4 and paragraph 4-3f). Agc feedback samples from each of the receiver's five i-f channels (SYM, B2, B1, A1 and A2) are brought into 2A2 at pins B, C, D, E and F, via transistors Q7, Q8, Q9, Q10 and Q11, respectively. These signals are then brought to four comparator networks (IC1, IC2, IC3, and IC4 and their associated components) and, at the same time brought out at pins 8, 9, 10 and 11. (The SYM and B2 signals share the same path, since only one of the two will appear at any given time.) These four agc signals (at pins 8, 9, 10 and 11) are for the associated receiver's comparators. The other inputs to the comparator are from the associated receiver's i-f channel agc feedbacks (SYM/B2, B1, A1 and A2) and are brought in at pins H, J, K and L, respectively. If, in any one of the comparators, the receiver's channel i-f level (as indicated by the agc level) is more than 6 db weaker than that of the associated receiver, the comparator (which is an operational amplifier) is triggered to send out a "quieting" signal to that a-f channel in that receiver; and that a-f channel in the associated receiver remains operative.

(2) Test Data - Test data is given for inputs and outputs of 2A2 in servicing block diagrams figures 4-2, 4-3 and 4-4.

r. 2A3 SUBCARRIER GENERATOR

(1) Circuit Description (figure 5-47/5-48)

A. Signal Detection Section - The greater part of the circuitry in 2A3 is utilized in the receiver's signal detection section (see figure 4-2 and paragraph 4-3e). The basic 1-mc reference signal enters at pin 4 and is amplified through transistors Q1 and Q2. The divide-by-100 section is made up of two decade counters, Z1 and Z2, each one dividing the frequency by 10. The resulting 10 kc is then brought over to the base of Q3. The output of Q2 is also brought to a divide-by-4 circuit, essentially the master-slave flip-flop Z6, which succeeds in dividing the signal by 2 twice. The resulting 250 kc is amplified separately through Q9 and through Q10 and brought out at pins L and M of 2A3 to be used in the receiver's A1 and B1 product detectors. The 250 kc signal is also applied (via Q11 and Q12 amplifiers) to the emitters of Q13 and Q14.

The 10 kc and the 250 kc are used to create the 243.71 kc and 256.29 kc required for the receiver's B2 and A2 product detectors. The 10 kc applied to the base of Q3 (a keyed oscillator) causes Q3 to produce harmonics and these, amplified through Q4, are brought to a narrow bandpass filter, FL1, centered at 6.29 mc. The 6.29 mc output is applied via Q5 and Q6 to a divide-by-1000 section, consisting of decade counters IC3, IC4, and IC5, each of which divides the signal by ten. The resulting 6.29 kc is passed through a low-pass filter consisting of capacitors C24 and C25 and coil L7 and this is applied to the bases of Q13 and Q14. This causes Q13 and Q14 to act as mixers, producing sum and difference frequencies from the 6.29 kc and the 250 kc. At the output of Q13 a filter, FL2, picks out the sum frequency, (256.29 kc); at the output of Q14 FL3 picks out the difference frequency 243.71 kc. These two frequencies are brought out (the 256.29 kc via Q15 and Q17 and the 243.71 kc via Q16 and Q18) to pins S and P, respectively, to be used in the receiver's A2 and B2 product detectors.

B. AFC Section - Transistors Q7 and Q8 are used in the receiver's AFC section (see figure 4-8 and paragraph 4-3j). When the receiver's controls are set for AFC mode, a ground appears at pin A and the 250 kc drift-tracking signal appears at pins 5 and 6. The ground signal acts through diode CR3 to disable divider Z6, thereby blocking the 1-mc-derived 250 kc; the same ground signal acts through diode CR4 and switching transistor Q7 to enable amplifier Q8. The drift-tracking 250 kc is then substituted for the stable 1-mc-derived 250 kc, as the basis for the product detector injection frequencies.

(2) Test Data - Test data is given for inputs and outputs of 2A3 in servicing block diagrams figures 4-2 and 4-8.

s. 2A4 SYMMETRICAL DEMODULATOR

(1) Circuit Description (figure 5-48/5-50)

A. Signal Detection Section, Symmetrical Channel - The greater part of 2A4 circuitry is involved in the receiver's symmetrical channel signal detection (see figure 4-2A paragraph 4-3d). The 250 kc signal enters at pin 10 and then through a low-pass filter consisting of coils L1, L2, and L3 and capacitors C1, C2 and C3. From there it divides in two directions: to the envelope detector and to a product detector. The envelope detector consists of transistors Q1, Q2 and Q3, diode CR1 and their associated components. The product detector consists of transistor Q4, transformers T1 and T2, diodes CR2, CR3, CR4 and CR5, and their associated components. Both detectors share a common audio output amplifier state, consisting of transistors Q9, Q10, Q11, Q12 and Q13 and their associated components. Only one detector is operative at a time and this depends on the position of the receiver AM/CW selector control. A ground from this selector at pin N enables the envelope detector in the AM mode; a ground at pin L enables the product detector in the CW mode.

The 247-253 kc BFO (beat frequency oscillator) for the product detector is made up of transistor Q5, diodes CR6, CR7, CR8, CR9 and CR10, capacitors C15, C16, C17, C18, C19, and C20, coil L4, resistors R25, R26, R27, R28, and R29, potentiometers R23 and R24 and an external associated potentiometer (SYM BFO on Front panel of Unit 1). The latter is connected across pins F and J with the wiper connected to pin 6. Varying this potentiometer adjusts the BFO through its frequency range. BFO output is at the emitterjof Q8 and is coupled to the product detector via transformer T2.

B. Signal Detection Section, Meter Amplifier - The signal for the receiver's output level meter (for all modes) is included in 2A4 (see figure 4-2 and paragraph 4-3d). The audio signal samples comes in at pin 14, becomes amplified through transistors Q14, Q15 and Q16 and rectified into a d-c value by diodes CR11 and CR12. The d-c value is brought to pins 12 and 13 for the external meter (LINE DBM METER, 2M1).

(2) Test Data - Test data is given for inputs and outputs of 2A4 in servicing block diagrams, figures 4-2 and 4-2A.

t. 2A5 SYMMETRICAL IF/AGC

(1) Circuit Description (figure 5-51/5-52)

A. Signal Detection Section - The larger portion of 2A5 circuitry is involved in the receiver's symmetrical signal detection section (see figure 4-2A and paragraph 4-3d). The 250 kc i-f signal enters 2A5 at pin 14 and splits into two directions to a 6-kc width band-pass filter, FL2, and to a 2.5-kc width filter, FL1. The 6-kc filter is driven by Q1 and drives Q3; the 2.5-kc filter is driven by Q2 and drives Q4. Only one filter circuit is operative at a time, and this depends on the position of the receiver 6 KC/2.5 KC selector control. When the control is in a 6 KC position, a ground at pin 13 enables Q1 and Q3; when the control is in a 2.5 KC position, a ground at pin 12 enables Q2 and Q4. The two filter outputs share a common i-f amplifier chain consisting of transistors Q5, Q6, Q7, Q8, A10, Q11, Q12 and Q13. The signal output to the associated demodulator is via pins 5 and 6. A monitor i-f is taken out at pins 3 and 4.

B. Gain Control Section - Gain control for the symmetrical channel is included in 2A5 (see figure 4-3A and paragraph 4-3e). A samples of signal level is taken at Q12 and routed to an agc detector. The detector consists of amplifiers Q15, A16, A17 and Q18, whose collector voltages are requlated by H2V zenor diode, CR7. Rectification to a d-c voltage occurs at diodes CR2 and CR3. The

receiver's slow/medium/fast agc time constant selector switch picks off an output from pin 10, 9 or 8, respectively. The slow time constant circuit is determined by resistors R97 and R98, capacitors C62 and CR6, the medium by R95, R96, C61 and CR5, the fast by R93, R94, C60 and CR4. After the selection has been made, the agc is fed back to the amplifier chain via pin 11, Q14, Q9 and CR1. Instead of agc, a manually adjusted gain may be brought in at pin 11. Q19, Q20 and Q21 are temperature compensating devices for Q5, Q6 and Q9 respectively.

(2) Test Data - Test data is given for inputs and outputs of 2A5 in servicing block diagrams, figures 4-2A and 4-3A.

u. 2A6, 8, 10, 12 AUDIO/DEMODULATOR, ISB

(1) Circuit Description (figures 5-53/5-54)

A. Signal Detection Section - The greater part of this circuitry is used in the receiver's signal detection section (see figure 4-2 and paragraph 4-3d). The 250-kc i-f signal enters the P/C board at pins 12 and 13 and passes through a low-pass filter; the filter consists of coils L1, L2 and L3 and capacitors C1, C2 and C3. From there the signal goes to the product detector. The product detector consists of transistor Q1, transformers T1 and T2, diodes CR1, CR2, CR3 and CR4, and their associated components. The injection frequency is brought in at pin 15; this frequency varies with 2A6, 8, 10 and 12. For 2A6 it is 243.71 kc, for 2A8 and 10 it is 250 kc, for 2A12 it is 256.29 kc. The injection frequency is amplified through Q2 and Q3 and brought into the product detector at transformer T2. Output from the product detector is across capacitor C13 and this audio is amplified through Q4, Q5, Q6, Q7 and Q8. Here it is (a) brought out to an audio monitoring line via pins M and N and (b) brought out to the receiver's line level control via pins R and P. After level control, the audio signal re-enters the P/C board at pins 9 and 10. Further amplification occurs through Q9, Q10, Q11, Q12 and Q13. The signal is then coupled to the audiojoutput via transformer T3 to pins 6, 7 and 8. A sample of audio is taken before the coupling transformer (T3) and isolated through Q15 for the receiver's output level meter (pins 4 and 5).

B. Diversity Quieter Section - A Squelch input at pin B works through switching transistor Q14 to cut out the signal in the entire audio amplifier chain during dual diversity receiver operation.

(2) Test Data - Test data is given for inputs and outputs of 2A6, 8, 10 and 12 in servicing block diagrams, figures 4-2 and 4-4.

v. 2A7, 9, 11, 13 IF/AGC, ISB

(1) Circuit Description (figure 5-55/5-56)

A. Signal Detection Section - The greater part of the circuitry is used in the receiver's signal detection section (see figure 4-2 and paragraph 4-3d). The 250-kc carrier and sidebands enter at pin 14 and are amplified through Q1. FL1 is the crystal-centered sideband 3-kc channel filter and differs in the center frequency; in 2A7, 9, 11 and 13. The range for 2A7 is centered at 245.405 kc, that for 2A9 9+ 248.315, 2A11 is at 251.645 kc and that for 2A13 is at 254.595 kc. The selected channel frequencies then pass through Q2 and delay equalizer EQ1. The output of EQ1 is then coupled to the i-f amplifier chain, consisting of Q3, Q4, Q5, Q6, Q8, Q9, Q10 and Q11. Output is at pins 6 and 5. A monitor output is taken out at pins 3 and 4.

B. Gain Control Section - Gain control for the ISB channel is included in the circuitry (see figure 4-3 and paragraph 4-3e). A sample of signal level is taken at Q10 and routed to an agc detector. The detector consists of amplifiers Q13, Q14, Q15 and Q16, whose collector voltages are requlated by VR-1. Rectification to a d-c voltage occurs at diodes CR2 and CR3. The receiver's slow/medium/fast agc time constant selector switch picks off an output fraom pin 10, 9 or 8, respectively. The slow time constant circuit is determined by resistors R84 and R85, CR6 and capacitor C52, the medium by R82, R83, CR5 and C51, the fast by R86, R81, CR4, and C50. After the selection has been made, the agc is fed back to the amplifier chain via pin 11, Q12, Q7, and CR1. Instead of agc, a manually adjusted gain may be brought in at pin 11. Q17, Q18 and Q19 act as temperature compensating devices for Q3, Q4 and Q7.

(2) Test Data - Test data is given for inputs and outputs of 2A7, 9, 11 and 13 in servicing block diagrams, figures 4-2 and 4-3.

UNIT 3 REFERENCE GENERATOR

w. 3A2 POWER SUPPLY

(1) Circuit Description (figure 5-64/5-65) - Power supply 3A2 converts 15 VAC, and 35 VAC into +5 VDC, +15 VDC and +25 VDC, respectively. The d-c output voltages are used to supply the receiver's synthesizer/phase lock section.

In the +5V supply, the 15 VAC is rectified through full wave bridge rectifier CR3. This is followed by a series voltage regulator section and a current limiter section. The voltage regulator consists of transistor Q9 followed by an externally mounted (2N3442) power amplifier transistor, transistor Q12, diode VR6 and resistors R24, R25 and R26. The output of the 2N3442 transistor is sampled in the network formed of R24, R25 and R26 and fed to the base of comparator Q12. This is compared in Q12 with a reference voltage developed across diode VR6. The output from Q12 is a correction voltage and this is fed back to the base of series regulator Q10. The current limiter consists of transistor Q9, resistors R21 and R22 and transistor Q11. The current limiter (or "short-proof" feature) is, in effect, in the common current line that is the base of Q10 and the collector of Q12, in such a way that the base of Q10 can only draw a certain amount of current. When the +5V output is shorted, the voltage drop across R21 and R22 turns on switching transistor Q11. Q11 then draws current off of the common line, and this is the current limiting action. By setting potentiometer R22, the maximum current may be set; here it is shown for a 1.2 amp output.

The +15V and +25V supplies are essentially of the same circuit design, with a voltage regulator and a current limiter in each.

(2) Test Data - Refer to Section 5.

x. 3A3 1 MC DISTRIBUTION CARD

(1) Circuit Description (figure 5-66/5-67) - Circuitry in 3A3 is used in the receiver's synthesizer/phase lock section only (see figure 4-5 and paragraph 4-3g.).

When using a 1-mc standard source external to the receiver, the internal 1-mc standard in the Reference Signal Generator (3A1) becomes phaselocked to the external standard. The external standard (fe) comes in at pins 21 and 22; the internal standard (fi) enters at pins 1 and 2. Amplification takes place for fe through Q1, Q2 and Q3 and for fi through Q4, Q5 and Q6. Nandgates Z1D and Z2D, in this case, function as clippers. The 1-mc fe and fi are each divided by two through the two halves of master-slave flip-flop Z6; the two resulting 500 kc signals are then brought over to nandgate Z5. The output of Z5 is 500 kc exactly (with a maximum voltage amplitude) when the two inputs are exactly in phase. When the inputs are out of phase, the output amplitude diminishes. This is changed into a ripple d-c voltage through a filter, consisting of choke L5 and capacitors C12 and C13, and brought over to pin 3 of operational amplifier Z8. The pin 2 input of Z8 receives a positive d-c voltage. Z8 functions as a differential amplifier, providing an offset of the error voltage produced by the C12-C13-L15 combination, to a value suitable for use by 1 MHz std Z9.

The output of Z8, an offset DC voltage, is brought over to Q8 and Q27. Q8 functions as a switch and Q27 as a high-impedance source follower and memory, when input from Q8 is absent. From Q27, the d-c output is brought out to pin 17 of 3A3 and used to correct the 1 mc standard (fi) in 3A1. The corrected 1-mc then enters at pins 1 and 2 of 3A3 to close the correction loop. The d-c error output from the junction of L5 and C13 is also brought over to pin 3 of operational amplifier Z7. Pin 2 of Z7 receives a positive d-c voltage. Z7 compares the error output of the C12-C13-L5 integrator with a reference voltage, and functions as a differential amplifier, whose output is the difference between the error and reference signals. The output of Z7 is brought out to pins M and R of 3A3 to operate an external meter, the dial of which is used to indicate phase differences between fi and fe.

A steady positive voltage of approximately +4 VDC is brought out at pin 15 to allow a frequency difference reading (between fi and fe) on the same meter. A receiver "phase comparator/frequency difference" switch (see figure 4-5) is set to the "frequency difference" position of this reading. This switch (a) disconnects the correction voltage to the 3A1 1-mc standard and (b) replaces it with a steady voltage. The 1-mc (fi), now entering pins 1 and 2 of 3A3; remains constant since the phaselock loop is disabled. The frequency difference appears at the same spot as does the phase difference (at the output of Z5A). The resulting d-c voltages from the filter then takes the same path to the external meter; the meter includes calibration markings for frequency difference along with phase difference.

Level sensing circuits are used for warning signals of external/internal 1-mc standard failures. A sample is taken of fe from the output of Q1 and fi from the output of Q4; these samples are fed into two separate level-sensing circuits. The fe circuit consists of Q9, Q10, Q11, Q12, Q13, Z1A, Q14 and Q15; the fi circuit consists of Q15, Q17, Q18, Q19, Q20, Z2-1, Q21 and Q22. Failure of fe causes the collectors of Q14 and Q15 to switch to ground and this warning signal is brought out at pin 20 of 3A3; when fi fails, Q21 and Q22 collectors and pin 4 switch to ground.

Information from the level sensing circuits is also used in the 1-mc switching logic output. Level sensing signals for fe are brought through Z-1B to Z-1C gate. Level sensing signals for fi are brought through Z-2B to Z-2C gate.

Fe is applied to pin 10 of Z-1C gate and fi is applied to pin 10 of Z-2C gate.

Assume that fe fails or its amplitude at input pin 21 falls below about . 7 volt. Z-1C gate will close and fe will not appear at pin 8, Z-1C. This also causes Z-3C to go high, opening Z-3D and allowing fi to proceed through Z-3D. If, on the other hand, fi fails or decreases in amplitude below about . 7 volts, the fi level sensing signal at Z-2C will block fi from proceeding. This resulting high logic level at pin 13, Z-3D, will allow fe to proceed to the output.

In the event of either fe or fi failure, the phase-lock loop is disabled. When failure occurs, either Z-1B or Z-2B causes output of Z-3A to go high, cutting off the operation of Q8 and Q27 via Z5D and Q7. The following truth table illustrates various gate actions under conditions of internal standard operation, external standard operations, and operation when both standards are functioning:

Output of	INT.	EXT. (int. failure)	Both
Z1C	H	ext. 1 MHz	ext. 1 MHz
Z1B	L	H	H
Z2B	H	L	H
Z3A	H	H	L
Z3B	L	ext. 1 MHz	H
Z3C	H	ext. 1 MHz	H
Z3D	int. 1 MHz	ext. 1 MHz	int. 1 MHz
Z2C-Z4	int. 1 MHz	H	int. 1 MHz

The 1-mc output from the 1-mc logic switching circuits is applied to Q23 via amplitude control R89. The emitter output of Q23 feeds three separate 1-mc stages: Q24, Q25 and Q26. The output of Q24, at pin 7 is applied to card 1A1A2 in the counter section of the RF Tuner. The output of Q25, at pin 9, is applied to the 1-mc monitor jack on the rear interface panel. The output of Q26, at pin 12, is applied to the synthesizer circuits of the Reference Generator.

(2) Test Data - Test data is given for inputs and outputs of 3A3 in servicing block diagram figure 4-5.

y. 3A4 1-mc SELECTOR

(1) CIRCUIT DESCRIPTION: (Figure 5-68/5-69

The circuitry of 3A4 is used only in the receiver's phase lock/synthesizer section. A 1-mc signal is introduced at pin 12 and is applied to three stages: Q1, Q2 and Q3. The signal appearing at the emitter of Q3 has been purposely distorted to provide an output rich in harmonics of the one megacycle input. This output is applied simultaneously to six crystal-amplifier circuits:

Y-1 = 11 mc
Y-3 = 14 mc
Y-5 = 10 mc
Y-7 = 12 mc
Y-9 = 16 mc
Y-11 = 17 mc

The crystals act as high Q bandpass filters, allowing only the desired harmonics of 1-mc to be amplified.

Y1 frequency, 11-mc, utilizes amplifiers Q4, Q5, Q6 and Q7. Crystal Y2 is also included to insure a clean 11-mc output at pin 19.

Y3 frequency, 14-mc, becomes amplified and tuned through Q8, Q9, Q10, Q11 and Q12. An additional 14-mc crystal, Y4, and tuned coil/capacitor tank circuits serve to further eliminate other products. The 14-mc is then divided by ten through decade counter Z2, becoming 1.4 mc, and this frequency is brought out at pins 17 and 18 via driver Q13.

Y9 frequency, 16-mc, becomes amplified through Q24, Q25, Q26, Q27 and Q28. An additional 16-mc crystal, Y10, and tuned coil/capacitor tank circuits serve to further eliminate other products. The 16-mc is brought out of 3A4 at pins 5 and 6.

Y11 frequency, 17-mc, becomes amplified through Q29, Q30, Q31 and Q32. An additional 17-mc crystal, Y12, tuned coil/capacitor tank circuits serve to further eliminate other products. The 17-mc is brought out of 3A4 at pins 21 and 22.

The 16-mc from Q28, together with a similarly generated 10-mc and 12-mc serve to create the 3, 4, 5 or 6 mc as selected by a 2-bit code from a receiver control. The 10-mc from crystals Y5 and Y6 and tuned amplifiers Q14, Q15, Q16, Q17 and Q18 are divided by two (to become 5-mc) in master/slave flip-flop Z5. The 5-mc is brought over the quadruple nandgate assembly, Z3. If the receiver's 10 MEGACYCLE switch is set at "2", the 2-bit code at pins A and B of 3A4 will be "0" and "1" (or ground and open), respectively. These pins lead to binary decoder Z1. Outputs from Z1 lead to the two quadruple nandgate circuits, Z3 and Z4. The code for "2" will then produce the proper signal to the nandgates, from Z1, to cause 5 mc to be issued from 3A4 pins 1 and 2. In like manner, the 16-mc from Q28 is brought over to master/slave flip-flop Z6. Z6 may be made to divide by two or to divide by four, and this is controlled by Z3 and Z4. The 4-mc is therefore derived at pins 1 and 2 by the appropriate code at pins A and B, working through Z1 to control Z3 and Z4 and causing Z6 to divide the 16-mc by four. The 3-mc and 6-mc are likewise derived from a 12-mc tuned amplifier chain; in the first case Z6 is made to divide by four, in the second case by two.

(2) Test Data - Test data is given for inputs and outputs of 3A4 in servicing block diagram figure 4-5.

z. 3A5 100 KC SELECTOR

(1) Circuit Description (figure 5-70/5-71) - Circuitry in 3A5 is used in the receiver's synthesizer/phase lock section only (see figure 4-5 and paragraph 4-3g.). The 1-mc, used to derive the

16. 1 - through 16. 9-mc stepped frequencies, enters 3A5 at pin 13, and amplifiers Q1 and Q2. The 1-mc is then divided by ten through decade counter Z1 and the resulting 100 kc is distributed through emitter-follower Q3 to the nine tuned-amplifier chains. The 100 kc output of Q3 is rich in harmonics; the resonant frequency of the quartz crystal at the input of each chain selects that harmonic. For instance, in the case of the 16. 1-mc chain, 16. 1-mc crystal Y9 in the input of tuned amplifier Q20, selects that frequency. Further products are eliminated by additional tuned stages in Q21, Q22 and Q23 and 16. 1-mc crystal Y10. The output appears at pin 9 of 3A5.

(2) Test Data - Test data is given for inputs and outputs of 3A5 in servicing block diagram figure 4-5.

aa. 3A6, 7 MATRIX DISTRIBUTOR

(1) Circuit Description (figure 5-72/5-73) - Circuitry in 3A6 and 3A7 is used in the receiver's synthesizer/phase lock section only (see figure 4-5 and paragraph 4-3g.). From one input set of ten (16. 0 through 16. 9) 0. 1-mc stepped frequencies, one of these frequencies is selected for two separate outputs (pins Z and 22 and pins A and B). The frequency selected at each of the two is controlled by a separate 4-bit code input from a receiver MEGACYCLE selector switch (pins C, D, E and F or pins U, V, W and X).

A typical selection can be described for the 16. 0-mc frequency with a code input at pins C, D, E and F. The 16. 0-mc frequency, appearing at pins 2 and 3, becomes amplified through Q1 and Q2 and brought to pin 12 of positive nandgate Z5D and pin 5 of positive nandgate Z6B. If the other input to either gate is positive at this time, the gate will open and the 16. 0-mc will pass through. Assuming that the code is correct at pins C, D, E and F, binary decoder Z1 will send a positive charge to pin 13 of Z5 opening the gate. The frequency then passes through another gate in Z5 (with its input wired to function as an amplifier) and similarly through an amplifier in Z15. Q21 is an additional amplifier and Q22 functions as an emitter-follower to drive the next stage.

(2) Test Data - Test data is given for inputs and outputs of 3A6 and 3A7 in servicing block diagram figure 4-5.

ab. 3A8 MATRIX DISTRIBUTOR

(1) Circuit Description (figure 5-74/5-75) - Circuitry in 3A8 is used in the receiver's synthesizer/phase lock section only (see figure 4-5 and paragraph 4-3g.). From the set of ten (16. 1 through 17. 0) 0. 1-mc stepped frequencies one of these frequencies is selected for the common output (pins M and 10). The frequency selected is controlled by a 4-bit code input from the receiver 1. 0 MEGACYCLE selector switch (pins F, H, L and K).

A typical selection can be described for the 16. 5-mc frequency. The 16. 5-mc, appearing at pins 17 and 18, becomes amplified through Q24 and Q23 and brought over to pin 9 of a positive nandgate in quadruple nandgate assembly Z4. If the code at pins F, H, L, and K is correct for 16. 5-mc, binary decoder Z12 will place a positive charge at pin 10 of Z4 and the gate will open, allowing the 16. 5-mc to pass through. The two inputs to another gate (pins 4 and 5) are wired together and this section then performs as an amplifier for the frequency. This is followed by a 16. 5-mc crystal, Y8, and amplifier Q22. Here the 16. 5-mc comes out on a common line to driver Q31 to appear at output pins M and 10.

(2) Test Data - Test data is given for inputs and outputs of 3A8 in servicing block diagram figure 4-5.

ac. 3A9, 10, 11 MIXER/AMPLIFIER

(1) Circuit Description (figure 5-76/5-77) - Circuitry in 3A9, 3A10 and 3A11 is used in the receiver's synthesizer/phase lock section only (see figure 4-5 and paragraph 4-3g.). The 11-mc enters the + (plus) mixer via pins 3 and 4; the injection frequency enters at pins 1 and 2. The injection frequency for 3A9 is 1. 4 mc, 1. 400-1. 409 mc for 3A10 and 1. 4000-1. 4099 for 3A11. The mixer consists of field-effect transistors Q3 and Q4 with tuned transformer T1 in the output to select the sum frequency. Additional tuned circuits follow with amplifiers Q5, Q6 and Q7 and the signal is applied to the second plus mixer. This mixer is made up of Q10, Q11 and transformer T2. The injection frequency for this is one of a set of ten 0. 1-mc stepped frequencies from 16. 0 through 16. 0 mc as selected by a receiver control. This frequency is brought in at pins 7 and 8, amplified through Q18 and Q19, divided through decade counter Z1 and applied to the mixer via driver Q20. The sum frequency appearing at the output of T2 becomes amplified through Q12, Q13, Q14, Q15 and Q16, divided by ten through decade counter Z2 and leaves the circuit at output pins 18 and 19 via driver Q17.

(2) Test Data - Test data is given for inputs and outputs of 3A9, 3A10 and 3A11 in servicing block diagram figure 4-5.

ad. 3A12 MIXER/AMPLIFIER

(1) Circuit Description (figure 5-78/5-79) - Circuitry in 3A12 is used in the receiver's synthesizer/phase lock section only (see figure 4-5 and paragraph 4-3g.). The 11-mc enters the + (plus) mixer via pins 3 and 4; the injection frequency (1. 40000-1. 40999 mc) enters at pins 1 and 2. The mixer consists of field-effect transistors Q3 and Q4 with tuned transformer T1 in the output to select the sum frequency. Additional tuned circuits follow with amplifiers Q5, Q6 and Q7 and the signal is applied to the second plus mixer. This mixer is made up of Q10, Q11 and transformer T2. The

injection frequency for this is one of a set of ten 0.1-mc stepped frequencies from 16.0 through 16.9 mc as selected by a receiver control. This frequency is brought in at pins 7 and 8, amplified through Q18 and Q19, divided through decade counter Z1 and applied to the mixer via driver Q20. The sum frequency appearing at the output of T2 becomes amplified through Q12, Q13, Q14, Q15 and Q16, and applied to quadruple positive nandgate assembly Z2. Z2 standardizes and limits the output. The signal is then brought over to 3A12 output pins 18 and 19, via driver Q17.

(2) Test Data - Test data is given for inputs and outputs of 3A12 in servicing block diagram figure 4-5.

ae. 3A13 FINAL MIXER/OUTPUT

(1) Circuit Description (figure 5-80/5-81) - Circuitry in 3A13 is used in the receiver's synthesizer/phase lock section only (see figure 4-5 and paragraph 4-3g.). The 3, 4, 5 or 6-mc (selected by a receiver control) enters the + (plus) mixer via pins 3 and 4 and amplifiers Q1 and Q2; the injection frequency (14.00000-14.09999 mc) enters at pins 7 and 8 and amplifiers Q5 and Q6. The mixer consists of field-effect transistors Q3 and Q4 with tuned transformer T1 in the output to select the sum frequency. In the output of T1 is a variable capacitance tuned circuit composed of capacitors C14, C15, C16, C17, C18 and C19, coil L3, diodes VC1 and VC2, and resistors R14 and R15.

The variable capacitance tuned circuit is tuned for four possible frequency ranges, by a 2-bit code entering at pins 15 and 16 of 3A13. The four ranges are (1) 17.00000-17.09999, (2)18.00000-18.09999, (3) 19.00000-19.09999 and (4) 20.00000-20.09999 mc; the four 2-bit codes are selected by a receiver control. A code is applied to binary decoder Z1 and the Z1 output is applied to quadruple positive nandgate assemblies Z2 and Z3. The output of Z3 works through switching transistors Q24, Q25 and Q26. A +25V supply is brought in at pins 1 and 2 and amplified through Q21, Q22 and Q23. This voltage, referred to as "VC bias" is switched to four levels by the switching transistors and a voltage divider circuit (composed of resistors R79, R80, R81, R85, R86 and R87). The VC bias is then connected at the variable capacitance tuned circuit at an input at R14. The four stepped voltages change this circuit's capacitance value and frequency range. The resulting frequency is then amplified through Q7, Q8 and Q9 and brought to the minus mixer, Q10. The other input into Q10 is one of a set of ten frequencies (16.1-17.0 mc) in 0.1-mc steps, selected by a receiver control. This frequency is brought in via pins 17 and 18 and amplifiers Q27 and Q28. The 2.00000-3.20000 mc difference frequency is then amplified to output pins 21 and 22. A parallel output is brought through Q11, Q12, Q13, Q14, Q15 and Q16 and is brought out via amplifiers Q20, Q19, Q17 and Q18 and output pins 19 and 20.

(2) Test Data - Test data is given for inputs and outputs of 3A13 in servicing block diagram figure 4-5.

UNITS 4 AND 8

af. 4A1, 8A1 OUTPUT KEYER

(1) Circuit Description (figure 5-88/5-89) - Circuitry in 4A1 is used in the receiver's remote readback section only (see figure 4-11 and paragraph 4-3m.). Codes in serial pulse teletype form are received at pin V, in "marks" (1) and "spaces" (0). During a space interval, pin V is connected to an external ground ; during a mark interval the ground is disconnected. Relay K1 is a voltage-operated polar relay, connected to an external -12V in such a way as to bias it in the mark position. When a space ground pulse arrives at pin V, the relay is drawn into its space position.

High and low level output pins are available for the two types of teletype loop-operated sending equipment: 60 ma (high-level) and 20 ma (low-level) current loops.

(2) Test Data - Test data for the 4A1 assembly is included in timing chart figure 4-12.

ag. 4A2, 8A2 CODE SHIFT REGISTER

(1) Circuit Description (figure 5-90/5-91) - Circuitry in 4A2 is used in the receiver's remote readback section only (see figure 4-11 and paragraph 4-3m.). Remote readback timing chart figure 4-12 best describes the operation of this circuit. Pin 2 is the input through which "code shift" pulses are received. Flip-flops Z1 through Z5 function as a shift-register. Each gate, in negative quadruple andgates Z6 through Z9, is connected to the shift register so as to open (from four negative inputs) in the following order:

Order	Assembly	Output Pin
1	Z6	10
2	Z6	11
3	Z6	12
4	Z6	1
5	Z7	10
6	Z7	11
7	Z7	12
8	Z7	1
9	Z8	10
10	Z8	11
11	Z8	12
12	Z8	1
13	Z9	10
14	Z9	11
15	Z9	12
16	Z9	1

It may be seen, referring to the timing chart, that bit number 1 of the "E" code is produced at the beginning of the readback cycle when Z5 goes from "set" to "reset" (or when pin 11 of Z5 goes from positive to negative). This charge travels through diode CR3 and, becoming inverted through quadruple inverter Z10, leaves 4A2 via pin M as a positive charge.

A diode group, consisting of CR4, CR5, CR6 and CR7, forms the 4-bit "1-10" receiver identification code as the last code in the readback cycle. Each bit-line contains a diode and terminates in an output pin of 4A2. Pins B, C, 3 and D are bits 2, 3, 4 and 5 of the 5-bit code to be transmitted. Diode arrangement is different for each of the ten receivers. * The presence of a diode creates a "1" bit; the absence of a diode creates a "0". This code is transmitted when pin 11 of Z5 goes to ground. Pin E is not used in receiver operation.

(2) Test Data - Test data for the 4A2 assembly is included in timing chart figure 4-12.

ah. 4A3, 8A3 BIT SHIFT REGISTER

(1) Circuit Description (figure 5-92/5-93) - Circuitry in 4A3 is used in the receiver's remote readback section only (see figure 4-11 and paragraph 4-3m.). Remote readback timing chart (figure 4-12 best describes the operation of this circuit. When +12V and -12V are applied (from the receiver's power supply) to pin 20 and 4, respectively, timing generator Z1 commences to issue a series of regularly timed pulses. Flip-flops Z2 through Z5 function as a shift-register. The six gates in negative dual andgates Z6, Z7 and Z8, are connected to the shift-register so as to place three negative charges on each gate one-by-one at alternate pulses from Z1; the order of this occurrence is from top to bottom. The first gate (as Z5 pin 11 goes negative) produces the "start" pulse; the output of each of the next five gates is dependent on the polarity of the 1-5 bit information sitting on the bit input pin (B, H, 8, 12 or 13). If negative, all four negative inputs into the gate cause its output to go negative; if positive, the output remains positive. The pulses travel one by one through norgate Z9 and pin V of 4A3.

(2) Test Data - Test data for the 4A3 assembly is included in timing chart figure 4-12.

ai. 4A4, 8A4 DRIVE INPUT GATING CIRCUIT

(1) Circuit Description (figure 5-94/5-95) -

A. Remote Tuning Section - The larger part of circuitry in 4A4 is used in the receiver's remote tuning section (see figure 4-10 and paragraph 4-3m.). Remote tuning timing chart, figure 4-12, illustrates the operation of logic components. The 4-bit code input is at pins R, 2, J and B for bits 2, 3, 4 and 5, respectively. Each bit passes through an amplifier in Z1 or Z2 and an inverter in Z7. The sixteen negative andgates in Z8 through Z11 are connected to the bit-lines so as to function as code gates (see table 1-4 for codes). The correct code at a gate causes all four inputs to go negative, causing the normally positive output to go negative.

* See chart in figure 2-11 for diode arrangements.

One inverter, in quadruple inverter Z3, is used to invert the polarity of the "tune lockup" signal. This signal enters at pin S of 4A4 and exits at pin U. The "decoder inhibit" signal utilizes another inverter, appearing at pin X and exiting at pin T.

B. Remote Readback Section - Receiver status logic is read out of gates in 4A4 (refer to timing chart, figure 4-12). The first four gating pulses (10 mc, 1 mc, 100 kc and 10 kc) arrive one-by-one at pins P, M, D and C, respectively. Other inputs come from information on the receiver status (see figure 4-10) at pins V, K, H, E, Y and 21. The polarity appearing at pin 16 of 4A4 for each code represents bit number 1 of that code. This is issued via norgate Z6 and diode CR8.

(2) Test Data - Test data for the 4A4 assembly is included in timing charts, figures 4-12.

aj. 4A5, 8A5 STEPPING SWITCH GATING CIRCUIT

(1) Circuit Description (figure 5-96/5-97)

A. Automatic Tuning Section - The time delay circuitry, involved in an automatic tuning "fault", is contained in 4A5 (see figure 4-6 and paragraph 4-3h.). Refer to automatic tuning timing chart, figure 4-12. At the start of the automatic tuning cycle, a ground is placed at pin Y, triggering a time delay circuit consisting of driver Q2, inverter Q3, and switching transistor Q4. This sets the time delay and causes pin X of 4A5 to go negative (approximately -8V) in relation to pin V (positive with respect to pin X). If, after 20 seconds, the ground is not removed from pin Y, the time delay trips and the voltage at pin X becomes approximately +6V, and pin V becomes slightly positive, with respect to pin X. This trips an external time delay relay into its "fault" position. In this case, a local operator may reset the relay by pressing a reset button; this places a ground on pin K. The ground acts on the base of switching transistor Q1 to cause pin 12 of 4A4 to go to ground.

B. Remote Tuning Section - The greater part of 4A5 circuitry is used in the receiver's remote tuning section (see figure 4-10 and paragraph 4-3l.). Timing chart, figure 4-12, illustrates logic component operation. Mainly, bit number 1 routing and the signal interchange between the decoder and the memory unit is accomplished here.

Dual andgate assembly Z2 contains the two control gates; gate number has pin 6 as an output and gate number 2 has pin 11. Pin 21 of 4A5 is the bit number 1 input. From here it passes through a low pass filter and diode CR6, through Z7 and exits at pin U to the external reset button, then back to pin 14. (The other buffer in 27 is not used.) The control output to the master stepping switch is at pin B; the output for the receiver stepping switches is at pin E. A gate in Z5 (pin 6 output) and gates in Z5 (pin 6 output) and gates in Z6 function in part of

the "tune lockup" circuit. The other gate in Z5 (pin 11 output) creates the "memory advance" signal issuing at pin H. The "memory inhibit" signal, issuing at pin 11, is generated at a gate formed of diodes CR11 and CR12. The "start tune" signal, coming in at pin T, parallels that of the locally operated fault reset button ground at pin K (in the automatic tuning section) and accomplishes the same effect (i. e. : to reset the time delay relay in the event of a previous fault).

C. Remote Readback Section - The origin of the tuning/ready information (routed to the tuning/ready/fault logic section in 4A4) is a signal issuing from pin W. This is derived from the incoming signals (at pin Y) at the start and at the end of the automatic tuning cycle.

(2) Test Data - Test data for the 4A4 assembly is included in timing charts, figure 4-12.

ak. 4A6, 7, 8, 8A6, 7, 8 DIGITAL COMPARATOR

(1) Circuit Description (figure 5-98/5-99) - The digital comparators are used in the receiver's automatic tuning section only (see figure 4-6 and paragraph 4-3h.). There are two isolated comparator circuits contained in each P/C board; the circuits are identical in design. Each one has two 4-contact BCD inputs and one 2-contact (L and H) output. The comparisons are made by means of a series cascaded dual-input nandgates. The outputs of gate assemblies Z8 and Z2, pins W and 2 of the P/C boards, go to ground when both BCD inputs become equal. These outputs are not used in the receiver operation, but may be used in testing the comparator.

(2) Test Data - Test data for the comparators is included in servicing block diagram figure 4-6.

al. 4A9, 8A9 BAND SELECT/ERROR POLARITY LOGIC

(1) Circuit Description (figure 5-100/5-101) The 4A9 assembly is used in the receiver's automatic tuning section only (see figure 4-6 and paragraph 4-3h.). This P/C board contains two separately operating circuits: The band select logic and the error polarity logic. Automatic tuning servicing blocks figure 4-6, more specifically shows the operation of the logic components.

The band select logic section (sheet 2 of figure 4-6) operates from two BCD inputs. The first is the 10 mc 0, 1, 2 or 3 number, represented as the "1" and "2" digits in its BCD code, at pins L and K, respectively. The second is the 1-mc 0-9 number, represented as the "2", "4" and "8" digits in its BCD code, at pins B, C and P, respectively. From here, cascaded nandgates in assemblies Z1 through Z5 and andgates composed of diodes CR1 through CR8 determine (from the 10 mc and 1 mc information) into which of the four bands (2-4 mc, 4-8 mc, 8-16 mc or 16-32 mc) these two components fall. The result is a 4-bit code signal appearing at pins S, X, Y and R. This code is made up of "1s" and "0s"; "1" = +12V and "0" = ground.

The error polarity logic section (sheet 1 of figure 4-6) operates from five 2-contact (L and H) inputs, representing the "tuner lower" or "tuner higher" signals. The output is a single 2-contact signal representing a "tune lower" signal (pin W) or a "tune higher" signal (pin 19). Pins 18 and 20 are for the end-of-band "tuner stop" signal input. Normally, pins 18 and 20 are both left open; when a "stop" signal comes through, either pin 18 (Hi-stop) or pin 20 (Lo-stop) goes low, essentially "freezing" tuner drive motion, by removing control phase from the drive motor. The "virtual ground" signal comes in on pin 17 as sync is achieved (or passed through) and blocks the signals through the gates of Z12.

(2) Test Data - Test data for the 4A9 assembly is included in servicing block figure 4-6.

am. 4A10, 8A10 MOTOR DIRECT CONTROL

(1) Circuit Description (figure 5-102/5-103) The 4A10 assembly is used in the receiver's automatic tuning section only (see figure 4-6 and paragraph 4-3h.). The automatic tuning timing chart, figure 4-12, more specifically shows the sequencing of signals through this P/C board. The search generator, with its inputs of H and L at pins 15 and B, respectively, is made up of switching transistors Q4 and Q5, powered by an external 24 VAC across pins U and S, with the "search" signal output at pin W. The "virtual ground" signal, coming in at pin L, triggers a one-shot circuit component of Q3, Q9, CR8 and Q1 and this produces a pulse at TP3, the "search" output at pin W. The same virtual ground acts through CR6 and pin J to block the signal from the error polarity logic (in 4A9) from coming in at pins B and 15. The virtual ground also acts (through CR9) to create the operational amplifier gating output at pin 21 via switching transistors Q8 and Q2. The "buffered d-c loop" signal, coming in at pin M, is the output control for the chopper, composed of Q6 and Q7. Power for the chopper is an external 1. 1 VAC across pins E and K.

Diodes CR2 through CR3 form part of band select logic circuit of 4A9.

(2) Test Data - Test data for the 4A10 assembly is included in the timing chart, figure 4-12 and servicing block diagram figure 4-6.

an. 4A11, 8A11 SERVO LOOP CONTROL

(1) Circuit Description (figure 5-104/5-105) The 4A11 assembly is used in the receiver's automatic tuning section only (see figure 4-6 and paragraph 4-3h.). The operational amplifier made up of Z1, Q3, Q4 and their associated components, receives its "search" signal input, a signal composed of variable-amplitude a-c. This signal is translated into an a-c output, across pins 21 and 1, to an external coupling transformer. The secondary of

this transformer is connected at pins X, 14 and L and this forms the signal input to the motor control section, composed of switching transistors Q1 and Q2. The output, at pins J and V, is the a-c drive power to the external motor. Q1 and Q2 act as switching devices for the 180° phase shift in the a-c. The "chopper" signal, entering at pin C, works through operational amplifier Z2, to control Z1, A more concise picture of the normal signals occurring throughout 4A11 in an automatic tuning may be seen in timing chart, figure 4-12.

(2) Test Data - Test data for the 4A11 assembly is included in timing chart figure 4-12.

ao. 4A12, 8A12 -30V POWER SUPPLY

(1) Circuit Description (figure 5-106/5-107) Power supply card A12 receives 38 VAC at its input, and converts this to -30 VDC regulated, for use as energizing voltage for the rotary solenoid control positioners.

38 VAC enters A12 at pins 7 and 8 (common to each other) and pins 11 and 12 (also common). Rectification takes place through CR4 (a full-wave bridge rectifier); the resultant pulsating DC is passed through a surge limiting network composed of R7 and R8, and continues out of A12 (at pin 21) to an externally-mounted electronic filter/regulator consisting of series-pass transistor 4Q2 and zener regulator CR1, working in conjunction with board-mounted capacitors 4A12C1 and 4A12C3, in the base circuit of 4Q2. Filter/regulator operation is as follows: 4Q2 acts as a series voltage regulator (essentially a variable series resistance). By the zener action of 4CR1, a constant voltage is maintained in 4Q2's base circuit, and, therefore, a constant voltage output results. At the same time, the effective shunt capacitance of 4A12C1 and 4A12C3 across the -30-volt line has a much greater filtering effect than normal. Large filter capacitors 4C3 and 4C4 also provide a high degree of passive filtering.

A12 incorporates a short-proof current-limiting feature, consisting of diodes 4A12CR2 and 4A12CR3, and resistor network 4A12R2, 4A12R3, and 4A12R4. In the event of a short circuit across the -30-volt output, voltage drop across the resistor network would be greater than that across the diodes, thereby reducing 4Q2's forward bias and, consequently, reducing output current. Circuit values are such that the short-circuit equilibrium point falls well within the safe dissipation range of 4Q2 and all affected circuit components.

Resistors 4A12R5 and 4A12R6 form part of 4A2's bias circuit; resistor 4A12R1 is a bleeder resistor, and capacitor 4A12C2 is a bypass for RF and switching transients. Board output appears between pins 5, 6, H, and J (hot), and pins 1, 22, A, and Z (ground). Diode 4A12CR5 isolates the -30-volt output at pins H and J from that at pins 5 and 6.

Board pins B and D extend 4A12CR1, 4A12CR6, and 4A12R9 connections to external FAULT mode circuitry; pin D receives one side of FAULT lamp 4DS1, inserted in series with the -12-volt output of 4A13. This is routed through diode 4A12CR6, and is brought directly back to pin B, which is externally connected to FAULT relay 4K1. During a FAULT condition, relay 4K1 extends a ground to pin B of 4A12, causing the following:

1. Ground return is provided through 4A12CR6 causing externally-mounted FAULT lamp 4DS1 to illuminate.

2. One side of resistor 4A12R9 is grounded through diode 4A12CR1; the other side of R9 remains effectively connected to -30 VDC board output. The heavy current through 4A12R9 cuts off 4Q2, and causes output voltage and current to drop to a very low value, thereby stopping the rotary solenoid control positioners.

(2) Test Data - Pertinent test data for power supply 4A12 and 8A12 may be found by referring to figures 4-10, 4-10A, 4-11, 4-11A, 4-6 and to figures 5-106 and 5-107.

ap. 4A13, 8A13 +12V, -12V POWER SUPPLY

(1) Circuit Description (figure 5-108/5-109) Power supply boards 4A13 and 8A13 each contain two sections: one section produces +12 VDC regulated, and the other section produces -12 VDC regulated. Input to each section is 18 VAC from one of the secondary windings of power transformer 4T2 or 8T2.

Because both sections are quite similar in operation, only the +12 VDC section need be fully explained; the differences between the +12 VDC and -12 VDC will also be noted. Unless preceded by the unit number, all reference designations refer to components physically mounted on A13; thus, C7 in the following explanation refers to 4A13C7; 4C7 would refer to a component mounted external to 4A13.

Incoming AC (pins B and 2) is rectified by full-wave bridge rectifier CR1, and passes through a surge limiter consisting of R7 and R8. The resultant pulsating DC is applied to pin 3 of Z1: Z1 is an integrated voltage regulator, incorporating current limiting and short-circuit overload protection. Essentially, Z1 functions as an operational amplifier with heavy feedback.

An output of Z1 is applied to the base of driver Q2; Q2, along with R1, forms a divider-bias network for series-pass transistor Q1, which performs the actual regulation: Q1's collector-emitter path falls in series with the filtered output of CR1 (filtering is accomplished external to 4A13 by capacitor 4C5, connected between board pin D and ground). Q1 thus acts as a series resistance, varied by Z1, via Q2. Therefore, voltage output is ultimately regulated by Z1. In order to regulate properly, however,

Z1 must have an error input; this input is obtained by sampling the output voltage at the junction of the voltage divider formed by R4 and R5. The error sample is applied as feedback input to terminal 6 of Z1 (for the reader's information: within Z1, the error input is compared with an internal voltage reference standard in what amounts to a differential amplifier; output of this amplifier is applied to the base of Q2). Capacitor C4, connected between terminals 6 and 7 of Z1 is part of an internal frequency compensation network, to prevent oscillation at high frequencies and/or transient "ringing", due to the high gain through Z1. Capacitor C1 bypasses the +12 VDC regulated output to prevent oscillation and stray pickup, and resistor R9 is an output bleeder. Resistor R10 and capacitor C3 are not used in this application.

Current limiting is accomplished by Z1, in conjunction with resistors R6, R2, and R3; limiting is of the "switchback" type, i. e. - when a heavy current overload occurs, instead of simply limiting current flow to the maximum design the switchback type limiter reduces current flow to a relatively small fraction of maximum output value, until such time as the overload is removed. This is done in order to ensure continued maximum component reliability within the power supply itself, as well as to prevent possible damage to external components, since a current overload usually indicates a malfunction, in which case no purpose would be served by continuing maximum-current operation.

Limiter operation is as follows: Output current creates a voltage drop across R6, which would appear between Z1 terminals 1 and 8; however, the divider composed of R2 and R3 causes another voltage drop; this drop bucks out the drop across R6. It is this bucking action which allows the above-mentioned current increase (in this case, maximum load current is on the order of 2. 0 amperes). However, consider the case of a short circuit at the output: R2 and R3 are effectively in parallel across the output; therefore, the voltage across the combination approaches zero, and the bucking voltage is no longer generated. The heavy current through R6 causes a relatively large drop to appear between Z1 terminals 1 and 8; these become the current-limiting input terminals. Z1 immediately reacts by reducing forward bias on Q1 until output current returns to a safe predetermined value (in this case, about 0. 5 amp). The combination of R2 and R3 also provides a pre-load on the output of about 20 ma, so the regulator will always operate into a load of some sort.

Z1 terminal 4 is ground input for the IC; terminal 5 of Z1 is connected to ground through bypass capacitor C7. C7 reduces noise in the internal voltage reference source by the usual bypass action.

The -12-volt section of 4A13 functions in an identical manner to the +12-volt section, with the following exceptions: the -12 VDC series-pass transistor (4Q1) is mounted external to the board at pins 12 (emitter), 14 (collector, and 21 (base); the surge limiter comprises resistors R19, R20, R21, and R22. Due to the polarity inversion, the current limiter bucking divider is connected between the surge limiter network and the junction of R14 and R15. Resistor R11 is not used in this application.

(2) Test Data - Pertinent test data for power supply 4A13 and 8A13 may be found by referring to figures 4-10, 4-10A, 4-11, 4-11A, and to figures 5-108/5-109.

aq. 4A14, 8A14 +5V./+28V. POWER SUPPLY

(1) Circuit Description (figures 5-110/5-111) Power supply boards 4A14 and 8A14 each produce +5 VDC and +28 VDC from 12 VAC and 30 VAC inputs, respectively, from two secondary windings of power transformer 4T2.

Operation and circuitry of both sections of 4A14 and 8A14 is identical to that of the +12 VDC section of power supply 4A13, immediately preceding this text; therefore, the reader is referred to text section 4. ap, for a detailed explanation of power supply operation.

Note that the only component value changes between boards occur in the two voltage dividers (error feedback, and current limiter bucking divider), in the voltage rating of C2, and in the value of the output bleeders. Also, note that no voltage reference bypass is incorporated in the +5 VDC section of the board; pin 5 of Z1 is left open. All other component values remain identical to 4A13/8A13, as does theory of operation.

(2) Test Data - Pertinent test data for power supply 4A14 and 8A14 may be found by referring to figures 4-10, 4-10A, 4-11, 4-11A, and to figures 5-110/5-111.

UNITS 5 AND 9

ar. 5A1, 9A1 ISOLATION KEYER

(1) Circuit Description (figure 5-119/5-119) The 5A1 assembly is used in the receiver's remote tuning section only (see figures 4-10, 4-10A and paragraph 4-31.).

Pulses of current entering through code input pin 12 (and returning through pin 15) cause a voltage keying output from relay K1, across pins 4 and B. The 20 VAC applied from an external source across pins X and W is rectified across diode CR1 to bias relay K1 in its normally closed position. During the interval of a current pulse, however, transistor Q1 conducts and applies the proper voltage across the alternate coil of K1 to close pins 4 and B. The -12V, applied externally, at pin 4 then gets routed to pin B output.

(2) Test Data - Test data for the 5A1 assembly is included in timing chart, figure 4-13.

as. 5A2, 9A2 CLOCK TIMING CIRCUIT

(1) Circuit Description (figure 5-120/5-121)-

A. Remote Tuning Section - The greater part of the circuitry in the clock timing circuit is used in the receiver's remote tuning section (see figures 4-10, 4-10A and paragraph 4-31.). Timing chart, figure 4-13, illustrates the operation of the logic components on the P/C board. The -12V pulses of each code enter at pin E, become amplified through Z8 and routed to an andgate (with output pin 10) in Z4. The other input to the gate is the stunt line control. The output of the gate, upon arrival of the "start" pulse, sets flip-flop Z1 and Z1 starts timing generator Z2. Z2 then commences to issue a series of regular pulses at pin 6 and at pin 11. The pulses from pin 6 pace the decade counter shift-register (composed of pin 6 andgate in Z4, flip-flops Z11, Z9, Z10 and an additional external flip-flop) the pulses from pin 11 work through single-shot Z3 to pace the code pulses from pin 11 of a Z4 andgate. These code pulses are connected to the inputs of "bit" andgates in assemblies Z5, Z6, and Z7, and the other inputs of these gates are connected to the shift registers in such a way as to be set, one-by-one, for each code bit. Bits 1, 2 and 3 andgates are in Z5 assembly with output pins 10, 1 and 12, respectively; bit 4 andgate is in Z6 with output pin 12. Bit 5 andgates involve Z6 (output pin 1) and an andgate in Z7, with output pin 5. The first five five pulses from timing generator Z2 cause the decade counter to shift five times and each code bit polarity appears one-by-one at 5A2 pins K, N, J, S and T, in that order. Pulses from the timing generator Z2 exit via inverter Z12 and 5A2 pin P for use as bit-shifting pulses in the external memory register. After the next five shifts (to complete the cycle of ten) the external flip-flop sends a positive-going voltage to flip-flop Z1, via pin 2, resetting it and stopping the output of timing generator Z2.

Three more andgates in assembly Z7 are used for separate operations, also paced by the shift register. The andgate with output pin 10 (working with Z6 andgate output pin 10) furnishes a "reset" pulse to external associated circuits, on the sixth shift. Also, at this time, the Z7 andgate, with output pin 11, issues a triggering pulse to the associated timer. On the 5th shift, the Z7 andgate with output pin 6 issues a voltage change when a "blank" signal comes in at pin Y.

B. Remote Readback Section - Inverters in assembly Z8 (with input and output pins 8 and 9, 12 and 11) form part of the signal path for the "memory power off" readback.

(2) Test Data - Test data for the 5A2 assembly is included in timing chart, figure 4-13.

at. 5A3, 9A3 PARALLEL SHIFT REGISTER

(1) Circuit Description (figure 5-122/5-123)- This parallel shift register is used in the receiver's remote tuning section only (see figure 4-10, 4-10A and paragraph 4-31.). Timing Chart, figure 4-13, illustrates the operation of the logic components. Coded bits 1-5 enter, one-by-one, at pins M, V, F, K and 21, in that order. Depending upon polarity, they either set or leave reset flip-flops Z2 through Z6. This leaves charges sitting on (a) P/C board pins X, B, J, C, 7, 16, L, H, 10, and 15 and (b) andgates in Z7, Z9, Z10 and Z11. The coded charges on the P/C board pins is the parallel pulses output of the code. The andgate functions in various ways to decode particular codes that may be encountered in a message. Andgate Z7, together with a specially wired X/Y matrix opens to the correct A-E selector code (see table in figure 2-10 for letters-vs-wiring), and the signal on pin Y from external circuitry which inhibits or opens the Z7 gate. After this, andgates in Z10 with output pins 5 and 6 and flip-flop Z1 function to present outputs to associated circuitry at pins S and P. When the receiver's 1-10 code follows, Z11 andgates with output pins 5 and 6 issue signals. Gates in Z10 with output pins 11 and 10 are for passing the bit #1 information to memories "A" and "B" when used in dual system, in the AN/FRR-85 only output 11 is used. Input signals on pins W and N open or inhibit the andgates in Z10 with output pins 11 and 10 at the proper time. The gate in Z11 with output pin 11 responds to the "tune command" code at the end of the message. If a "clear" code is sent the gate in Z9 with output pin 11 issues a signal. If a "blank" code comes through, the gate in Z11 with output pin 10 issues a signal.

Flip-flop Z8 forms the final unit of a shift register in associated circuitry on 5A2 or 9A2.

(2) Test Data - Test data for the 5A3 assembly is included in timing chart, figure 4-13.

au. 5A4, 5A5, 9A4 GATING CIRCUIT

(1) Circuit Description (figure 5-124/5-125)- This gating circuit is used in the receiver's remote tuning section only (see figures 4-10, 4-10A and paragraph 4-31.). Timing Chart, figure 4-13, illustrates the operation of the logic components. Bits 2, 3 and 4 of the receiver selection code (1-5 for 5A4, 6-10 for 5A5 and 1-5 for 9A4) enter at pins P, U, R, M, N and T. Polarities and inverted polarities represent each of the three bits. This information is placed at the inputs of five gates, each representing a receiver, in assemblies Z10 and Z11. At the same time, a signal entering at pin X (indication that bits #1 and #5 are correct for the 1-5 or 6-10 code) and another signal entering at pin W (the "letters clear" signal) opens a gate (with output pin 6) in Z7. This signal travels, via two inverters in assembly Z6, to act as a release pulse for the Z10 and Z11 gates. According to the code, one of the Z10 or Z11 gates opens. The gate that opens then sets a flip-flop in the group of Z1 through Z5. The set flip-flop then places a charge on one input of one gate in the group of five formed by the four in assembly Z9 and the one made of diodes CR7 and 8. The flip-flop remains set and the charge remains at the gate throughout the tuning message. Upon the arrival of the "E" (tune command) code, a signal at pin K releases the gate and the output, the receiver "start tune" signal, leaves at the appropriate pin

(12, B, 7, 6 or C). At this time, a flip-flop reset signal enters at pin 5, resetting all 5 flip-flops. This places similar charges on all four inputs to a gate (with output pin 11) in Z7. This gate then sends a signal, via pin Y, to the external A-E gate on 5A3 or 9A3, resetting it for the next message. Diodes CR1 through CR5 and output pins J, H, 5, 3 and 2 are not used in this receiver.

(2) Test Date - Test data for the 5A4, 5A5 or 9A4 assembly is included in timing chart, figure 4-13.

av. 5A6, 9A6 SHIFT TIMING CIRCUIT

(1) Circuit Description (figure 5-126/5-127 - The circuitry in 5A6 assembly is used in the receiver's remote tuning section only (see figure 4-10, 4-10A and paragraph 4-31.). Timing Chart, figure 4-13, illustrates the operation of the logic components. Mainly, 5A6 controls the sequencing through the rest of the remote tuning circuit. Timing generator Z1 is for pacing a "fast-shift" in the memory section; this occurs after the "E" has been received and the code bits in the associated memory storage are being shifted towards the output. Timing generator Z2 generates the "single shift" into the memory in the reciprocating signals that occur during code transfer into the associated decoder. Both timing generators work (Z2 works via Z3 inverter output pin 9) through an andgate (with output pin 11) in Z5 and an inverter in Z3 (output pin 11) to fire single-shot Z7, producing the negative 2 microsecond shift pulses required. In the initial phase in which the codes are becoming stored in the memory, pulses from an external timing generator, entering pin pin W, and a set signal via pin X, travel through an andgate in Z11 (with output pin 6) and an inverter in Z9 (output pin 7) and serve as the memory bit shift pulses. These also take the common path through Z5 andgate, Z3 inverter, and single-shot Z7. Enabling timing generator Z2 are two signals: (1) the "E" signal working through an andgate (with output pin 11) in Z11 and the set for that gate at pin 21 and flip-flop Z8 to diode CR4 and (2) the "memory advance" signal entering via pin U and brought to diode CR3. Diodes CR3 and CR4 form an andgate in such a way that the signal entering via pin U will pass through the gate and to Z3 inverter (output pin 7) except during the time that the gate is inhibited by the tune signal (pin 19, via Z11 output pin 11 and Z8). The signal on pin 7 of Z3 will trigger the timing generator Z2 to produce a single pulse. There are three signals enabling timing generator Z1: (1) "letters gate clear" signal which occurs during the first character of a program (pin 7 via Z9 inverter output pin 11), (2) "bit 1 'A' monitor" signal via pin J and (3) a "clear" signal which occurs only during the program input of a "clear" character (pin 6 via Z9 inverter, output pin 6, and Z10 amplifier, output pin 11). Either the "letters gate clear" or the "clear" signal will trigger the timing generator Z1 via Z4 inverter (output pin 7) to produce a series of fast shift pulses (30kc). The "bit 1 'A' monitor" signal (pin J) will inhibit andgate Z5 (output pin 6) during the tuning process as soon as the first "1" bit comes out of memory.

Two andgates in Z6 assembly (with output pins 10 and 11) act as "E" and "clear" code reset gates for the receiver selector section. The two other andgates Z6 (with output pins 5 and 6) serve as input controls for the associated memory sections. In Receiving Set AN/FRR-85 only the gate with output pin 6 is used. Z9 (output pin 9), inverts the incoming signal on pin L to produce the "blank reject" signal (pin K). Z3 inverter (output pin 6), produces the "decoder inhibit" signal (pin P). A "letters gate inhibit" signal enters on pin D and is inverted by Z4 (output pin 6). This inverted output leaves the card on pin 2; however, this signal is used only in a system as the "dual control" signal. The signal at Z4 (pin 6), is also routed to a second inverter (Z4 output pin 9) and to CR2. The inverted signal (at pin E) is routed externally to "stunt relay" 5K1 or 9K1 and acts as an "equipment select" control signal. CR2 functions as a part of andgate Z6 (output pin 10).

(2) Test Data - Test data for the 5A6 assembly is included in timing chart, figure 4-13.

aw. 5A7, 9A7, 9A8 INTEGRATED SHIFT REGISTER

(1) Circuit Description (figure 5-128/5-129) - The circuitry in 5A7, 9A7 and 9A8 assemblies is used in the receiver's remote tuning section only (see figure 4-10, 4-10A and paragraph 4-31.). Timing Chart, figure 4-13, illustrates the operation of the logic components. Z1 through Z5 are integrated shift registers for storage of code bits #1 through #5, respectively. Bit #1 input enters at pin 2 of the P/C board and goes directly to Z1. Bits #2-5 come in at pins U, X, Y and W, respectively, and when the memory input gate is received via pin V, travel through the four andgates in Z11. As each shift pulse arrives at pin 6, the normally open gate Z6 transmits the pulse to the five shift-registers; this moves the 5 bits of the code by one place in the memory storage. This last statement is true for Receiving Set AN/FRR-85. In the Dual System, however, Z6 is controlled by an input at pins 7 and 8 of the P/C board. In this case, the shift pulse entering pin 6 of 9A8 (the "B" memory) is the opposite polarity of that entering pin 6 of 9A7 (the "A" memory). Z6 gate will open only if a release charge of similar polarity has been presented at pin 7 or 8. For the "A" memory (9A7) it is pin 7; for the "B" memory (9A8) it is pin 8. Each bit output leaves its shift-register to travel through two successive inverters located in inverter assemblies Z7 through Z10. There are two parallel isolated outputs for each bit. Bit outputs appear on pins D, 9, 11, 10 and J. Bit outputs also appear (but are not used) on pins 14, T, S, 13.

The "monitor" pulse from Z1 output is applied (after inversion in Z8) to an andgate (with output pin 6) in Z6. When a charge arrives via pin 5 of the P/C board (as a result of the "E" code)

this monitor pulse is released via an inverter in Z8 and pin E.

(2) Test Data - Test data for the 5A7, 9A7 and 9A8 assemblies is included in timing chart, figure 4-13.

ax. 5A10, 9A10 POWER SUPPLY

(1) Circuit Description (figure 5-130/5-131) - Power supply 5A10 and 9A10 contains three separate, but nearly identical, sections, producing various regulated voltages for use by the memory section.

As operation of this board is nearly identical to that of 4A13, the reader is referred to text section 4 ap for a detailed explanation of circuit theory.

Note that the only differences in configuration of 5A10 and 9A10 occur in actual component values of the error feedback divider (R5 and R17, R23 and R25, R10 and R18), current limiter bucking divider (R4 and R16, R7 and R8, R12 and R13), the current limiter series resistor (R2, R24, R27), and the voltage rating of output bypass capacitor C1. The particular values used on this board differ from those of 4A13 due to the different output voltage requirements. Also, note that both the rectifier and the series-pass transistor associates with regulator Z2 are mounted external to the board.

(2) Test Data - Pertinent test data for power supply 5A10 and 9A10 may be found by referring to figures 5-130/5-131, and to servicing block diagrams, figures 4-10 and 4-10A.

ay. 5A11 READBACK SELECTOR

(1) Circuit Description - Readback selector 5A11 allows up to ten decoders to read back on a single teletype line, the status of their respective receivers. Selection of the particular decoder to be read back at a given time is accomplished by depressing the proper alphanumeric code buttons on the EQUIPMENT SELECTION row of the remote programmer: the code thus generated will, besides opening the proper memory, initiate a readback from the selected receiver. Readback switching is performed by 5A11, by means of a control voltage applied to the appropriate position of the notch-homing wafer of rotary solenoid stepping switch 10S1: this voltage appears at one of the following board pins, depending upon the particular readback selected: pin 1, 2, 3, 4, 5, 6, 7, 8, C, or D.

Because selection of any position proceeds in identical fashion for all positions, only one readback position need be explained. Consider selection of readback number 3: a negative voltage generated by the equipment select circuitry appears at pin 3 of A11, and is routed directly to switch connector 5; connector 5 is wired directly to position 3 of 10S1's notch homing wafer. Assuming 10S1 is not presently at position 3, the voltage is routed out through the common wiper to switch connector 9, thence to A11 pin F. The negative voltage (low logic level) therefore appearing at pin F is inverted externally, and the resulting high logic level (virtual ground) is reapplied to pin W of A11. The now-high logic level proceeds through an isolation and transient-suppression network consisting of L1, CR2, and R1 and is applied to the gate of CR1, a silicon-controlled rectifier (SCR). CR1 is in series with the -30 VDC supply, the drive coil of 10S1, the drive interrupter switch, and ground return. A high level at CR1's gate causes it to fire, thus providing a ground return for -30 VDC, and completing the drive circuit. 10S1 therefore advances one position, whereupon the drive interrupter switch momentarily opens the drive circuit, stopping 10S1's rotation, and resetting CR1 to a non-conductive condition. If position 3 has not yet been selected by this single advance, the high logic level will continue to appear at the gate of CR1, repeating the entire single-advance cycle. What results is a rapid, almost continuous series of advances, until the notch homing wafer of 10S1 achieves position 3, at which time the CR1 gate activation voltage is removed, causing 10S1 to remain in position 3.

Ganged to 10S1's notch homing wafer are three other wafers: space, common, and mark, which carry the readback information itself. The readbacks enter and exit the switch via connector 10J2, at the following connector pins (readback number 1 through 10, respectively): Mark: 3, 4, 5, 6, 2, z, y, x, w, p; Common: g, h, j, k, l, m, n, Y, Z, a; Space: K, L, E, F, G, H, J, A, C. Readback output appears at 10J2 pins D (space), b (common), and r (mark). 10J2 pins N and M carry -30 VDC drive voltage.

CR3 is an arc suppressor diode, and capacitor C1 functions to eliminate transient mis-firing of CR1.

(2) Test Data - Test Data for 5A11 will be found within figures 4-11, 5-116, 5-117, 5-132 and 5-133.

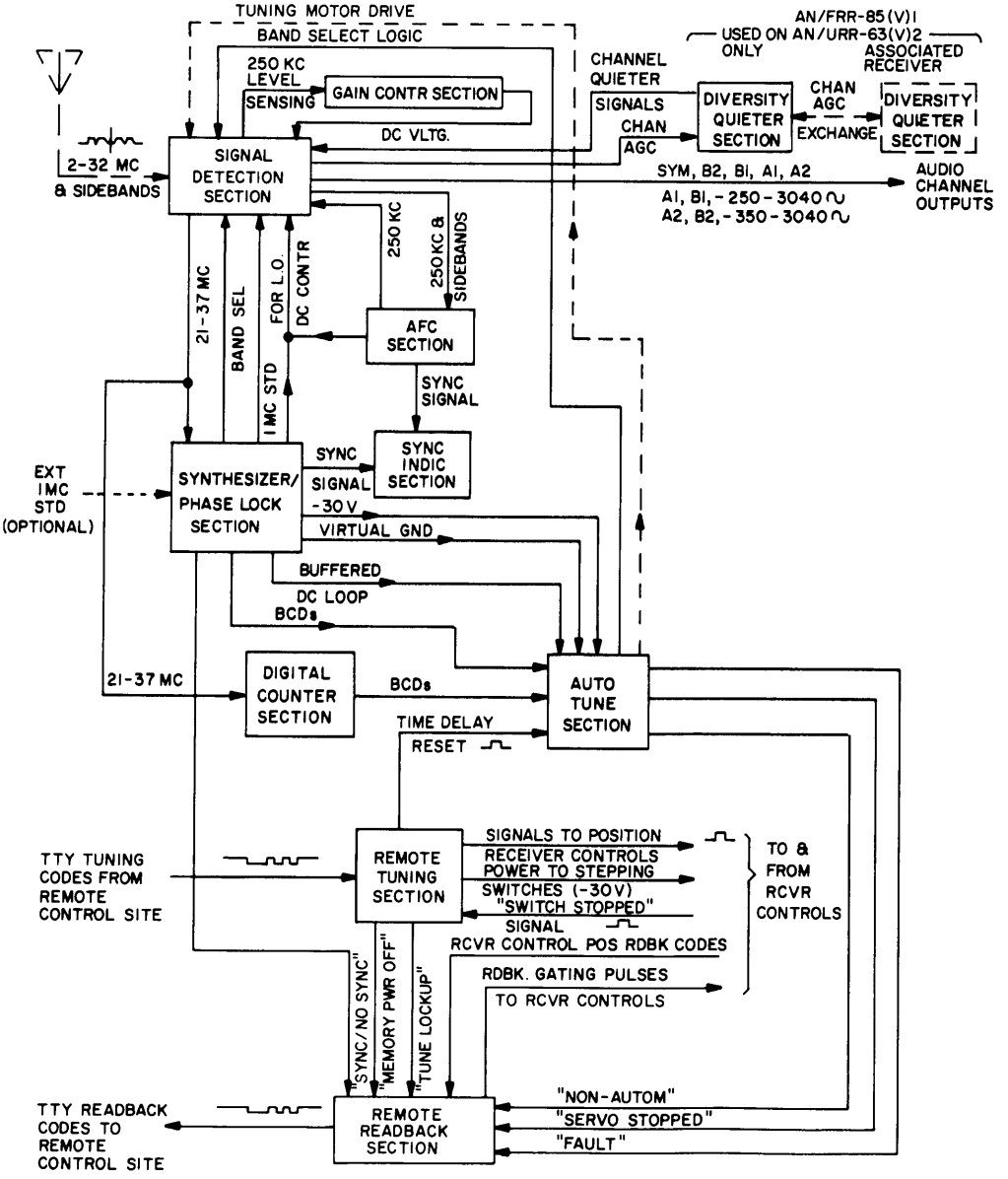
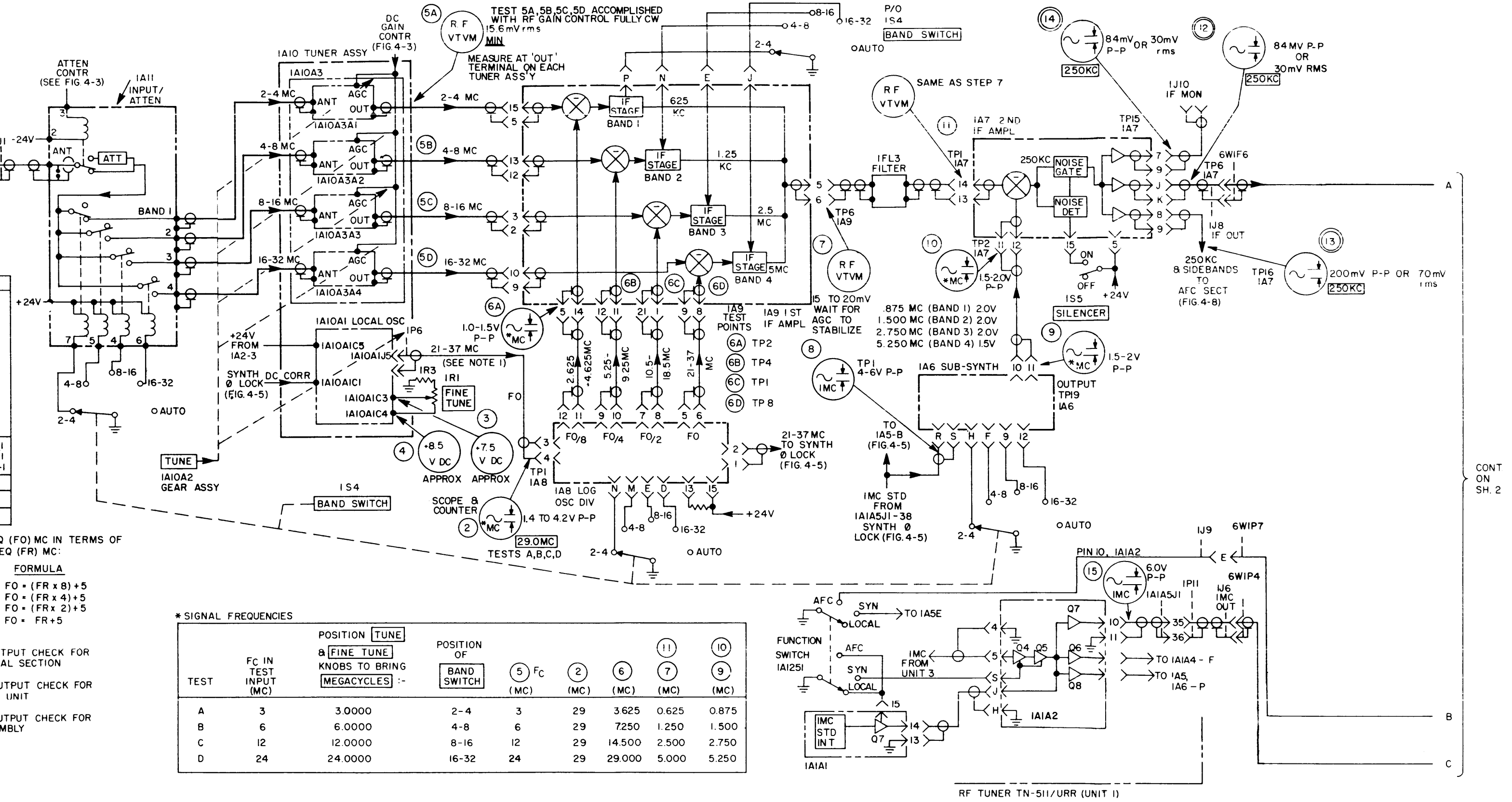


Figure 4-1. Overall Functional Block Diagram, Single Receiver



* SIGNAL FREQUENCIES

TEST	FC IN TEST INPUT (MC)	POSITION TUNE & FINE TUNE KNOBS TO BRING MEGACYCLES :-	POSITION OF BAND SWITCH	(5) FC (MC)	(2) (MC)	(6) (MC)	(11) (7) (MC)	(10) (9) (MC)
A	3	3.0000	2-4	3	29	3.625	0.625	0.875
B	6	6.0000	4-8	6	29	7.250	1.250	1.500
C	12	12.0000	8-16	12	29	14.500	2.500	2.750
D	24	24.0000	16-32	24	29	29.000	5.000	5.250

Q (FO) MC IN TERMS OF EQ (FR) MC:

FORMULA

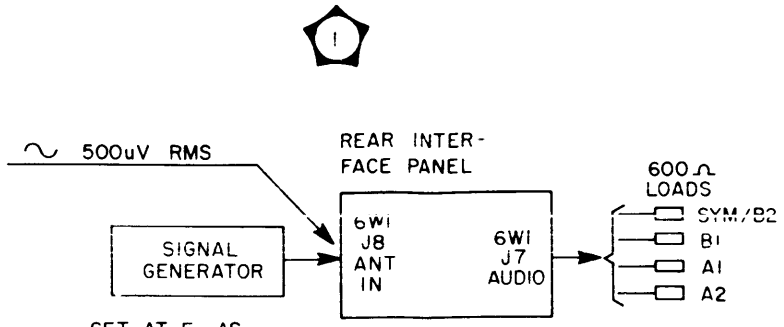
FO = (FR x 8) +5
FO = (FR x 4) +5
FO = (FR x 2) +5
FO = FR +5

TPUT CHECK FOR AL SECTION

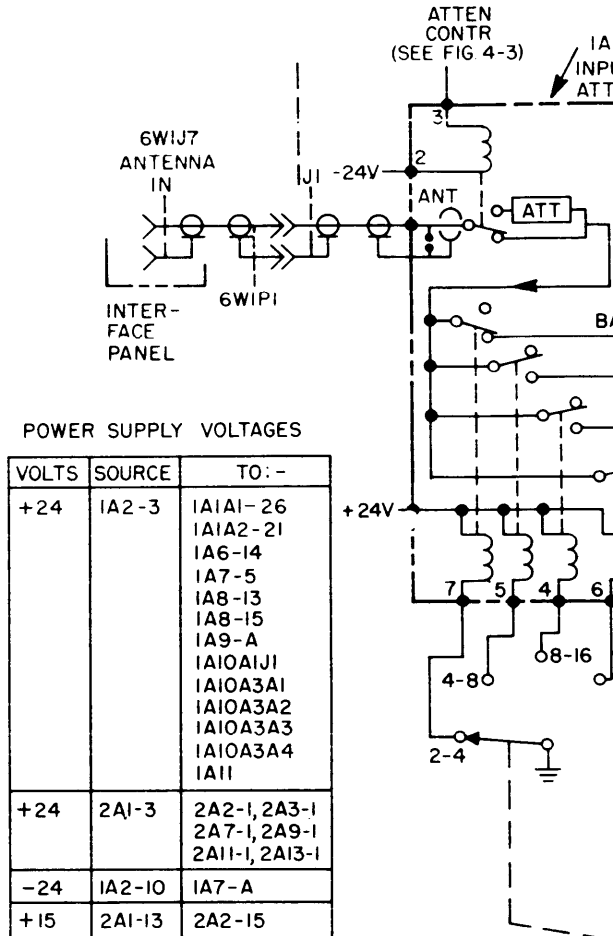
UTPUT CHECK FOR UNIT

UTPUT CHECK FOR MBLY

Figure 4-2. Servicing Block Diagram, Signal Detection Section, ISB Mode (Sheet 1 of 2)



TEST SETUP - SIGNAL DETECTION



CONTROL POSITIONS FOR TEST

MODULAR UNIT	CONTROL	POSITION
KY-661/URR	POWER SWITCH	OFF
CV-2520(V)/URC (OR CV-2521( )/URC)	POWER SWITCH	OFF
TN-511/URR (OR TN-525/FRR)	ATTENUATOR SWITCH	DOWN
"	RF GAIN KNOB	#AGC
"	SILENCER SWITCH	DOWN
"	POWER SWITCH	ON
"	FUNCTION SWITCH	LOCAL
"	COUNTER MODE SWITCH	REC
"	BAND SWITCH	AS SHOWN IN TEST
"	TUNE KNOB	"
"	FINE TUNE KNOB	MAX CCW
TD-915/URR (OR TD-969/FRR)	METER SENSITIVITY SWITCH	0
"	SYM/B2 AGC SOURCE	B2
"	B1	B1
"	A1	A1
"	A2	A2
"	AGC TIME CONSTANT SWITCHES (211)	MED
"	MODE SWITCH	ISB
"	POWER SWITCH	ON
"	LINE LEVEL ADJ KNOBS	**
O-1510/URR	POWER SWITCH	OFF

** ADJUST EACH KNOB FOR "0 DBM" ON LINE-DBM METER USING MONITOR SELECTOR SWITCH

EXCEPT FULLY CW FOR TEST 5 ONLY

POWER SUPPLY VOLTAGES

VOLTS	SOURCE	TO:-
+24	1A2-3	1A1A1-26 1A1A2-21 1A6-14 1A7-5 1A8-13 1A8-15 1A9-A 1A10A1J1 1A10A3A1 1A10A3A2 1A10A3A3 1A10A3A4 1A11
+24	2A1-3	2A2-1, 2A3-1 2A7-1, 2A9-1 2A11-1, 2A13-1
-24	1A2-10	1A7-A
+15	2A1-13	2A2-15
+5	2A1-E	2A3-2

NOTES: 1. LOCAL OSC FREQ (FO) MC IN TERMS OF RCVR TUNED FREQ (FR) MC:

BAND (MC)	FORMULA
2-4	FO = (FR x 8) + 5
4-8	FO = (FR x 4) + 5
8-16	FO = (FR x 2) + 5
16-32	FO = FR + 5

2 INPUT/OUTPUT CHECK FOR FUNCTIONAL SECTION

INPUT/OUTPUT CHECK FOR MODULAR UNIT

INPUT/OUTPUT CHECK FOR SUBASSEMBLY

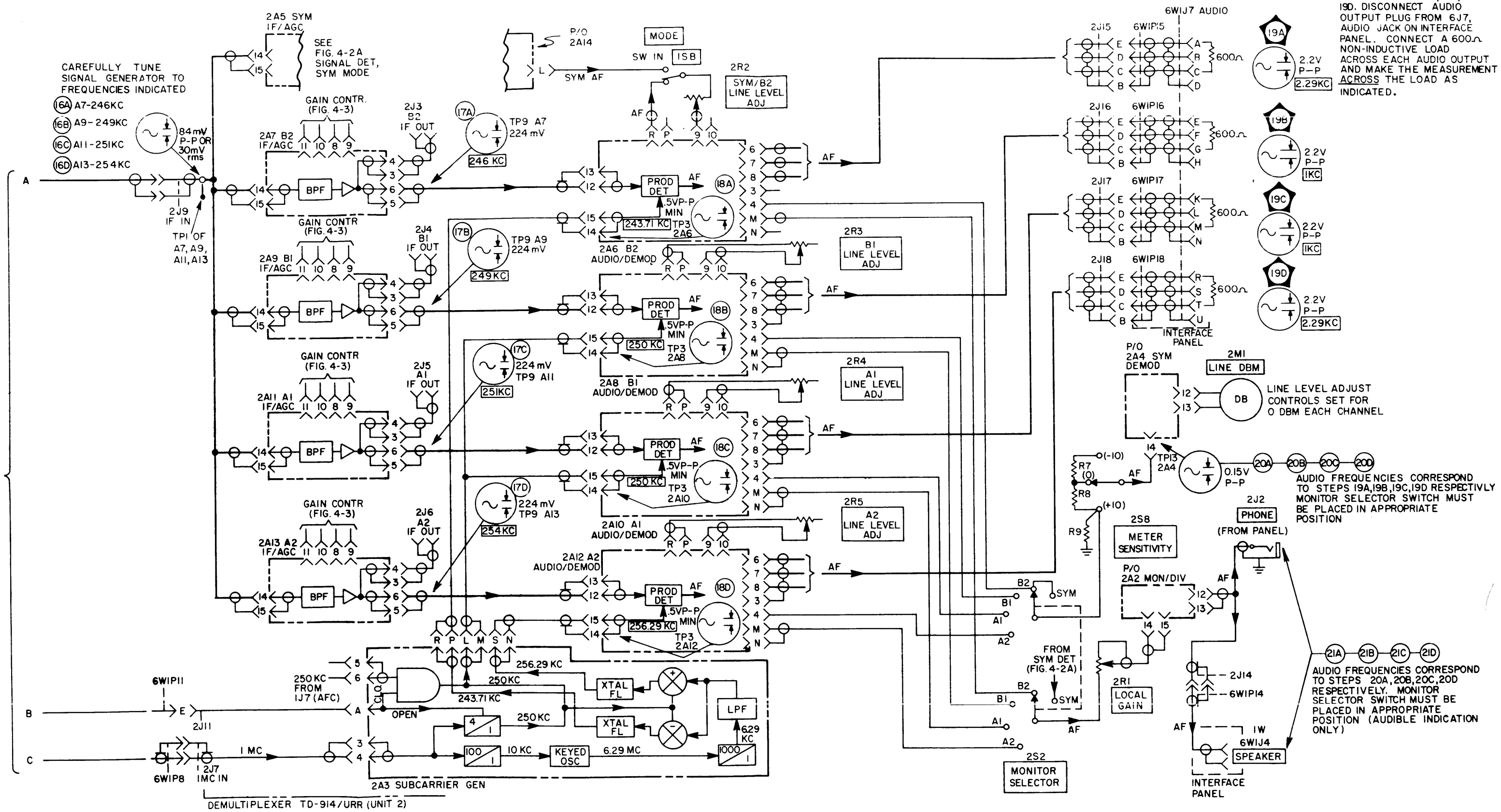
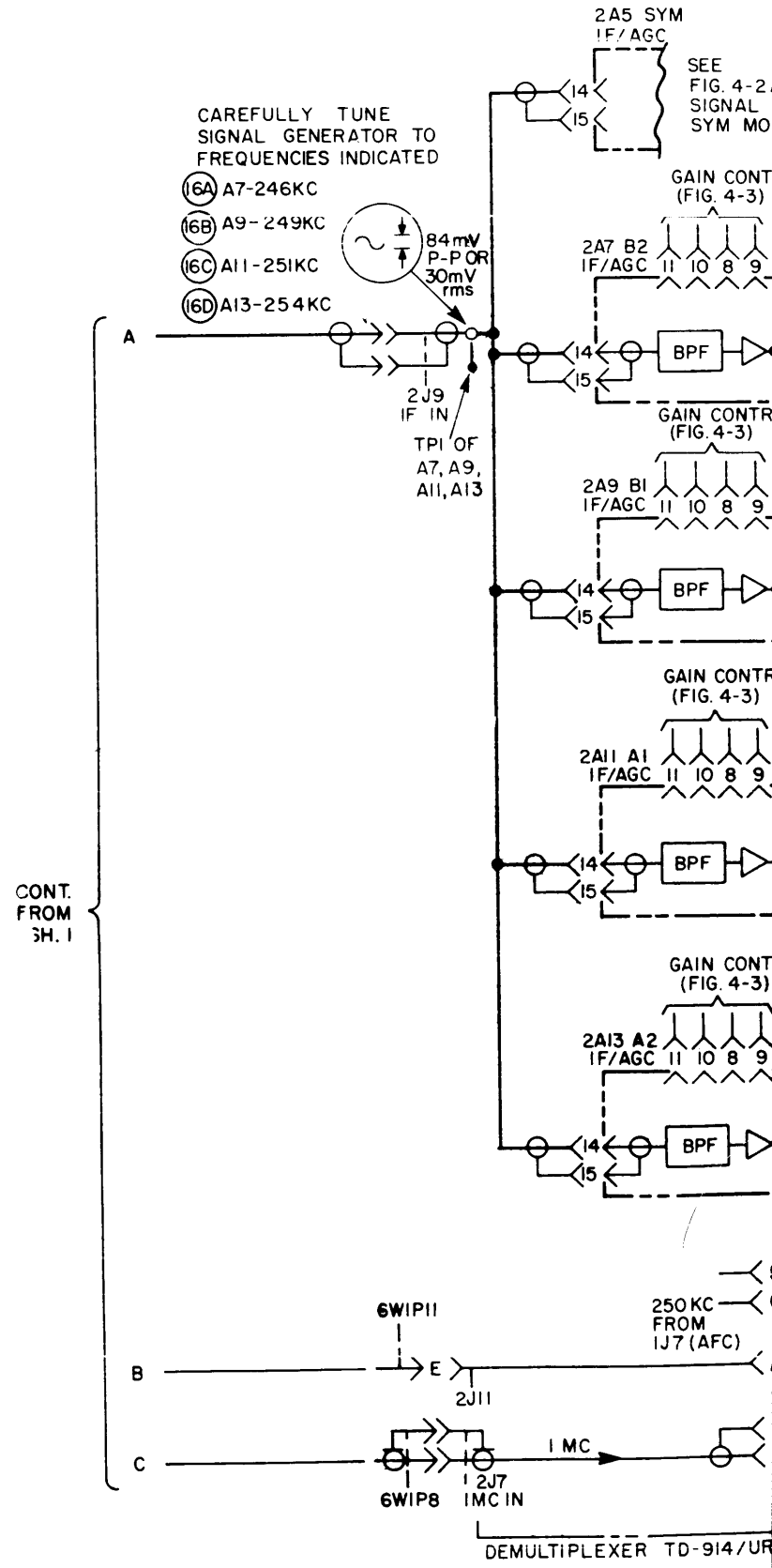


Figure 4-2. Servicing Block Diagram, Signal Detection Section, ISB Mode (Sheet 2 of 2)


2A5 SYM IF/AGC
SEE FIG. 4-2
SIGNAL SYM MO
GAIN CONT (FIG. 4-3)
2A7 B2 IF/AGC 11 10 8 9
BPF
GAIN CONTR (FIG. 4-3)
2A9 B1 IF/AGC 11 10 8 9
GAIN CONTR (FIG. 4-3)
2A11 A1 IF/AGC 11 10 8 9
GAIN CONT (FIG. 4-3)
2A13 A2 IF/AGC 11 10 8 9
CAREFULLY TUNE SIGNAL GENERATOR TO FREQUENCIES INDICATED
16A A7-246KC
16B A9-249KC
16C A11-251KC
16D A13-254KC
84mV P-P OR 30mV rms
A
2J9 IF IN
TP1 OF A7, A9, A11, A13
CONT. FROM SH. 1
6W1P11
250KC FROM 1J7 (AFC)
B
E
2J11
C
1 MC
2J7 1MC IN
6W1P8
DEMULTIPLEXER TD-914/UR

VOLTAGES

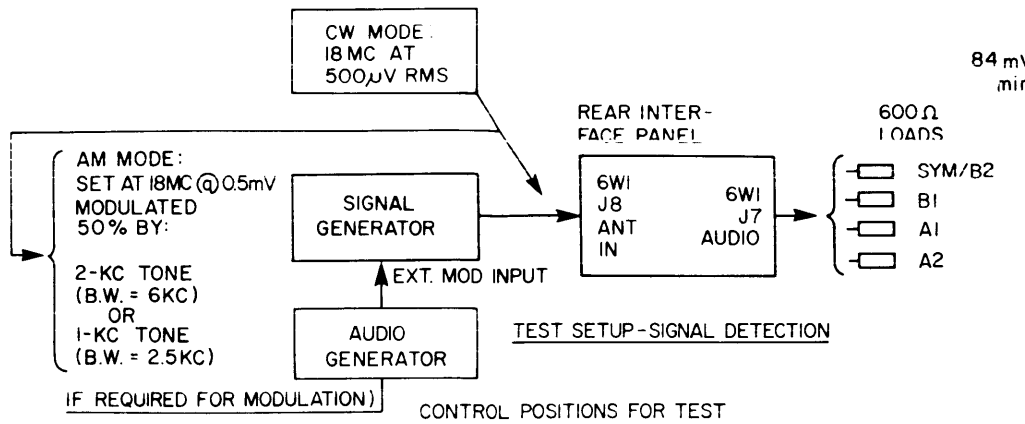
CE	TO:-
3	2A4-S, 2A4-1 2A5-1, 2A6-1

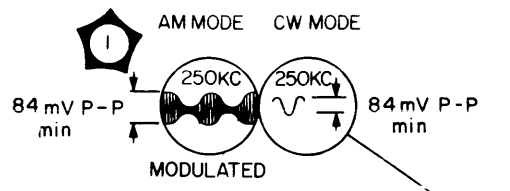
PUT/OUTPUT CHECK FOR FUNCTIONAL SECTION

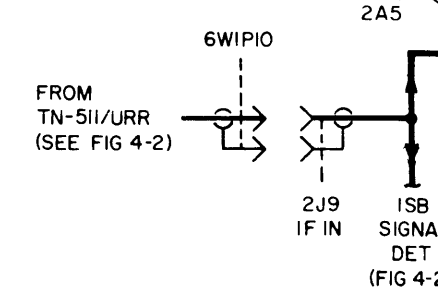
PUT/OUTPUT CHECK FOR MODULAR UNIT

PUT/OUTPUT CHECK FOR SUBASSEMBLY

Figure 4-2A. Servicing Block Diagram, Signal Detection Section, SYM Mode







CONTROL POSITIONS FOR TEST

MODULAR UNIT	CONTROL	POSITION
TN-512/URR (OR TN-525/FRR)	ATTENUATOR SWITCH	DOWN
"	RF GAIN KNOB	AGC
"	SILENCER SWITCH	DOWN
"	POWER SWITCH	ON
"	FUNCTION SWITCH	LOCAL
"	COUNTER MODE SWITCH	REC
"	BAND SWITCH	16-32
"	TUNE KNOB, FINE TUNE KNOB	TO OBTAIN 18.0000 ON MEGACYCLES DISPLAY
TD-915/URR (OR TD-969/FRR)	METER SENSITIVITY SWITCH	0
"	SYM/B2 AGC SOURCE SWITCH	B2
"	SYM/B2 AGC TIME CONSTANT SWITCH	MED
"	MODE SWITCH	AM 6KC (FOR AM); CW 2.5KC (FOR CW)
"	POWER SWITCH	ON
"	SYM/B2 LINE LEVEL ADJ KNOB	*
"	SYM BFO KNOB	+3KC
O-4510/URR	POWER SWITCH	OFF
KY-661/URR	POWER SWITCH	OFF
CV-2520(V)/ORC OR CV-2521(V)/ORC	POWER SWITCH	OFF

* ADJUST THIS KNOB FOR "0DBM" ON LINE-DBM METER, WITH MONITOR SELECTOR SWITCH AT SYM POSITION

POWER SUPPLY VOLTAGES

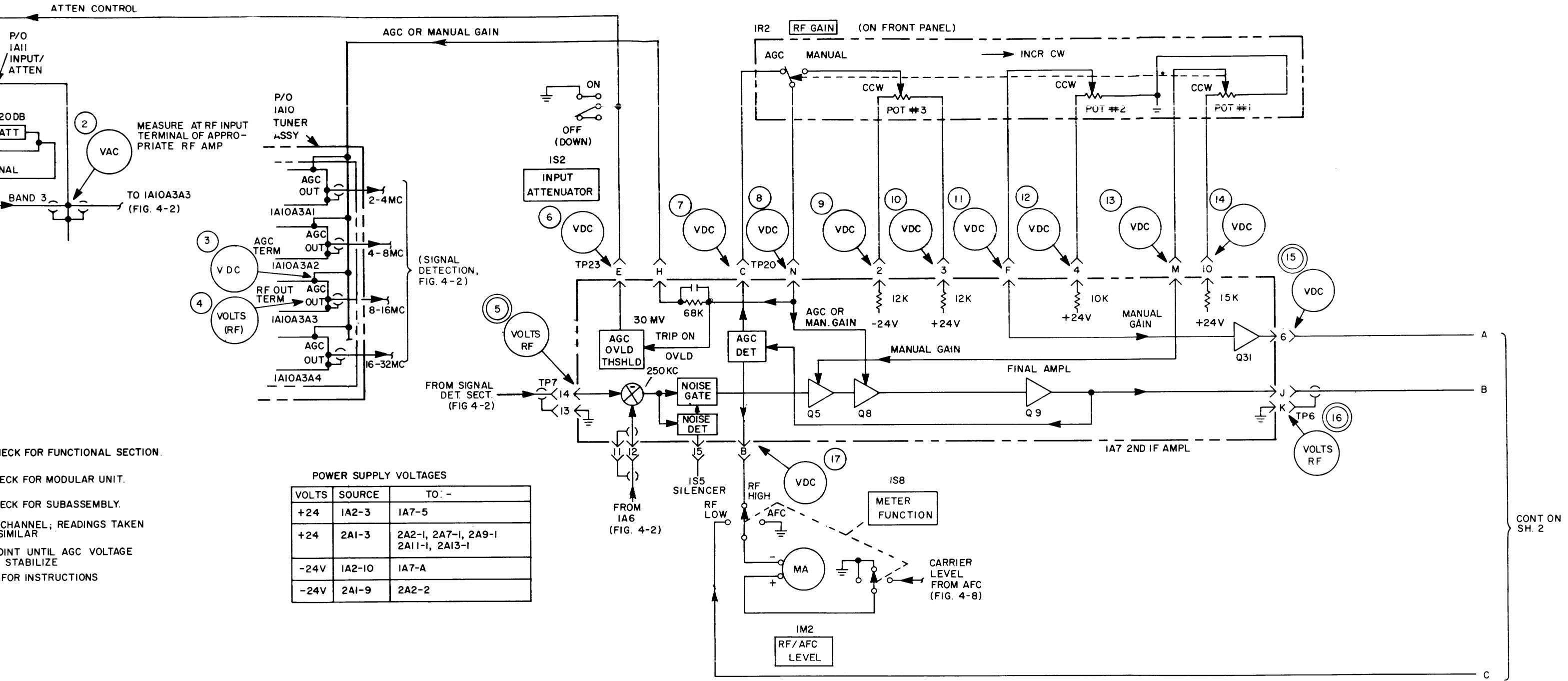
VOLTS	SOURCE	TO:-
+24	1A2-3	2A4-S, 2A4-1 2A5-1, 2A6-1

NOTES:

INPUT/OUTPUT CHECK FOR FUN

INPUT/OUTPUT CHECK FOR MOD

INPUT/OUTPUT CHECK FOR SUB



ECK FOR FUNCTIONAL SECTION.

ECK FOR MODULAR UNIT.

ECK FOR SUBASSEMBLY.

CHANNEL; READINGS TAKEN SIMILAR

OINT UNTIL AGC VOLTAGE STABILIZE

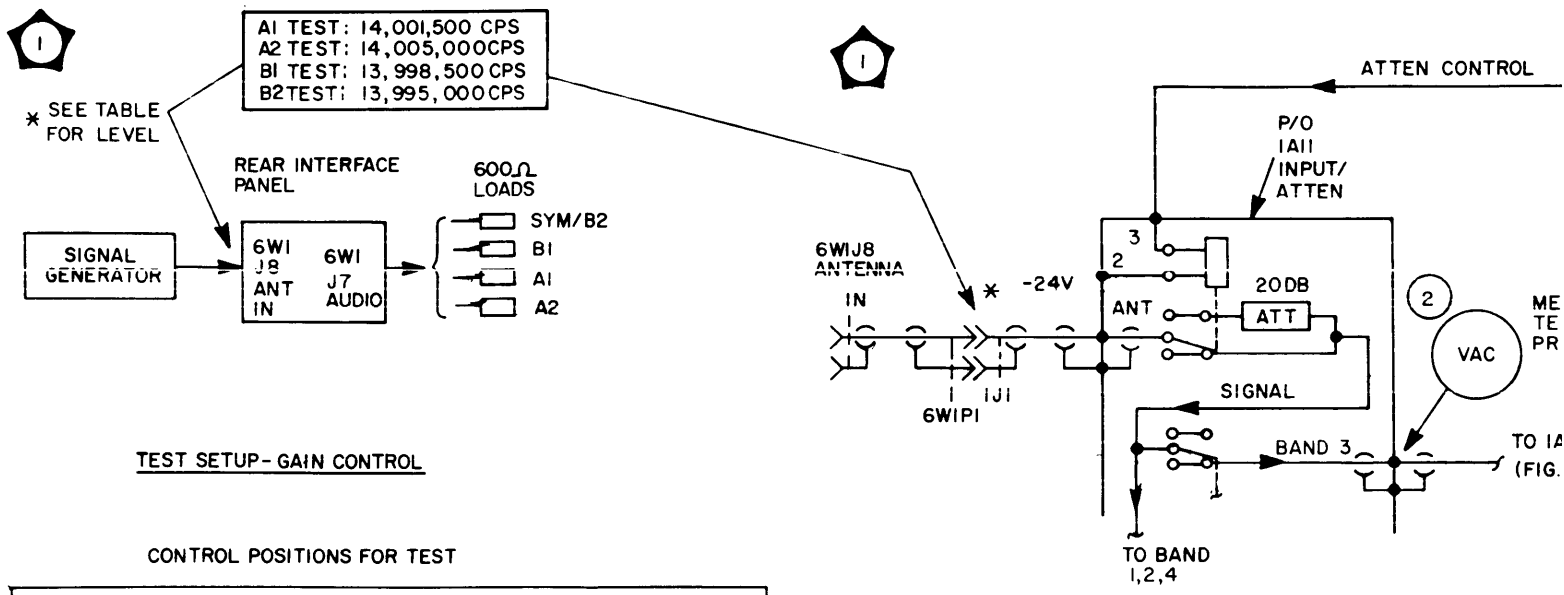
FOR INSTRUCTIONS

POWER SUPPLY VOLTAGES

VOLTS	SOURCE	TO: -
+24	1A2-3	1A7-5
+24	2A1-3	2A2-1, 2A7-1, 2A9-1 2A11-1, 2A13-1
-24V	1A2-10	1A7-A
-24V	2A1-9	2A2-2

(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)	(12)	(13)	(14)	(15)	(16)	(17)	(18)	(19)				
RMS	VDC	RMS	RMS	VDC	VDC	VDC	VDC	VDC	VDC	VDC	VDC	VDC	VDC	RMS	VDC	RMS					
—	0	—	12mV	-24	0	0	—	—	—	—	—	—	—	1mV	0	76mV	0				
68mV	-2	60mV	.5V	-.6	-11.0	-11.0	—	—	—	—	—	—	—	165mV	-.2	100mV	-.2				
00mV	-2.05	90mV	.57V	-.6	-11.0	—	—	—	—	—	—	—	—	—	—	—	—				
.0mV	-3.2	2.4mV	10mV	—	—	—	-13.0	+12.5	+7.4	+7.2	+1.7	+1.65	+2.4	4 mV	+.2	76mV	—				
1.1mV	+.15	8.2mV	95mV	—	—	—	-20.0	+.65	0	+7.8	0	+10.4	0	1.65V	0	410 mV	—				

Figure 4-3. Servicing Block Diagram, Gain Control Section, ISB Mode (Sheet 1 of 2)



TEST SETUP- GAIN CONTROL

CONTROL POSITIONS FOR TEST

MODULAR UNIT	CONTROL	POSITION
KY-661/URR	POWER SWITCH	ON
CV-2520(V)/URC OR CV-2521(V)/URC	POWER SWITCH	ON
TN-511/URR (OR TN-525/FRR)	ATTENUATOR SWITCH	OFF (DOWN)
	RF GAIN KNOB (TESTS A,B,C)	AGC
"	" (TEST D)	FULLY CCW
"	" (TEST E)	FULLY CW
"	SILENCER SWITCH	OFF (DOWN)
"	POWER SWITCH	ON
"	FUNCTION SWITCH	SYN
"	COUNTER MODE SWITCH	REC
"	BAND SWITCH	AUTO
"	TUNE AND FINE TUNE KNOBS	WILL SERVO TUNE TO OBTAIN 14.0000 ON MEGACYCLES DISPLAY
"	METER FUNCTION SWITCH	RF HIGH
TD-914/URR (OR TD-969/FRR)	METER SENSITIVITY SWITCH	0
	SYM/B2 AGC SOURCE SWITCH	B2
"	B1 " "	B1
"	A1 " "	A1
"	A2 " "	A2
"	AGC TIME CONSTANT SWITCHES	FAST
"	MODE SWITCH	ISB
"	POWER SWITCH	ON
"	LINE LEVEL ADJ KNOBS	**
0-1510/URR	POWER SWITCH	ON
	FREQUENCY SELECTORS	14.0000

** ADJUST EACH KNOB FOR "0 DBM" ON LINE-DBM METER, USING MONITOR SELECTOR SWITCH.

NOTES:

1. INPUT/OUTPUT CHECK FOR FUNCTIONAL SECTIO
   INPUT/OUTPUT CHECK FOR MODULAR UNIT.
   INPUT/OUTPUT CHECK FOR SUBASSEMBLY.
2. READINGS TAKEN FOR B1 CHANNEL; READINGS TAKEN FOR A2,A1,A3 SHOULD BE SIMILAR
3. LEAVE METER AT TEST POINT UNTIL AGC VOLTAGE AND/OR SIGNAL VOLTAGES STABILIZE
4. REFER TO PARAGRAPH 4 FOR INSTRUCTIONS

* SIGNAL VARIATIONS

TEST	①	②	③	④	⑤	⑥
		RMS	VDC	RMS	RMS	VDC
A AGC (MIN SIGNAL)	1uV	—	0	—	12mV	-24
B AGC (MAX SIGNAL)	1.0V	68mV	-2	60mV	.5V	-.6
C AGC OVERLOAD	1.5V	100mV	-2.05	90mV	.57V	-.6
D MANUAL GAIN (MIN)	500uV	1.0mV	-3.2	2.4mV	10mV	—
E MANUAL GAIN (MAX)		1.1mV	+.15	8.2mV	95mV	—

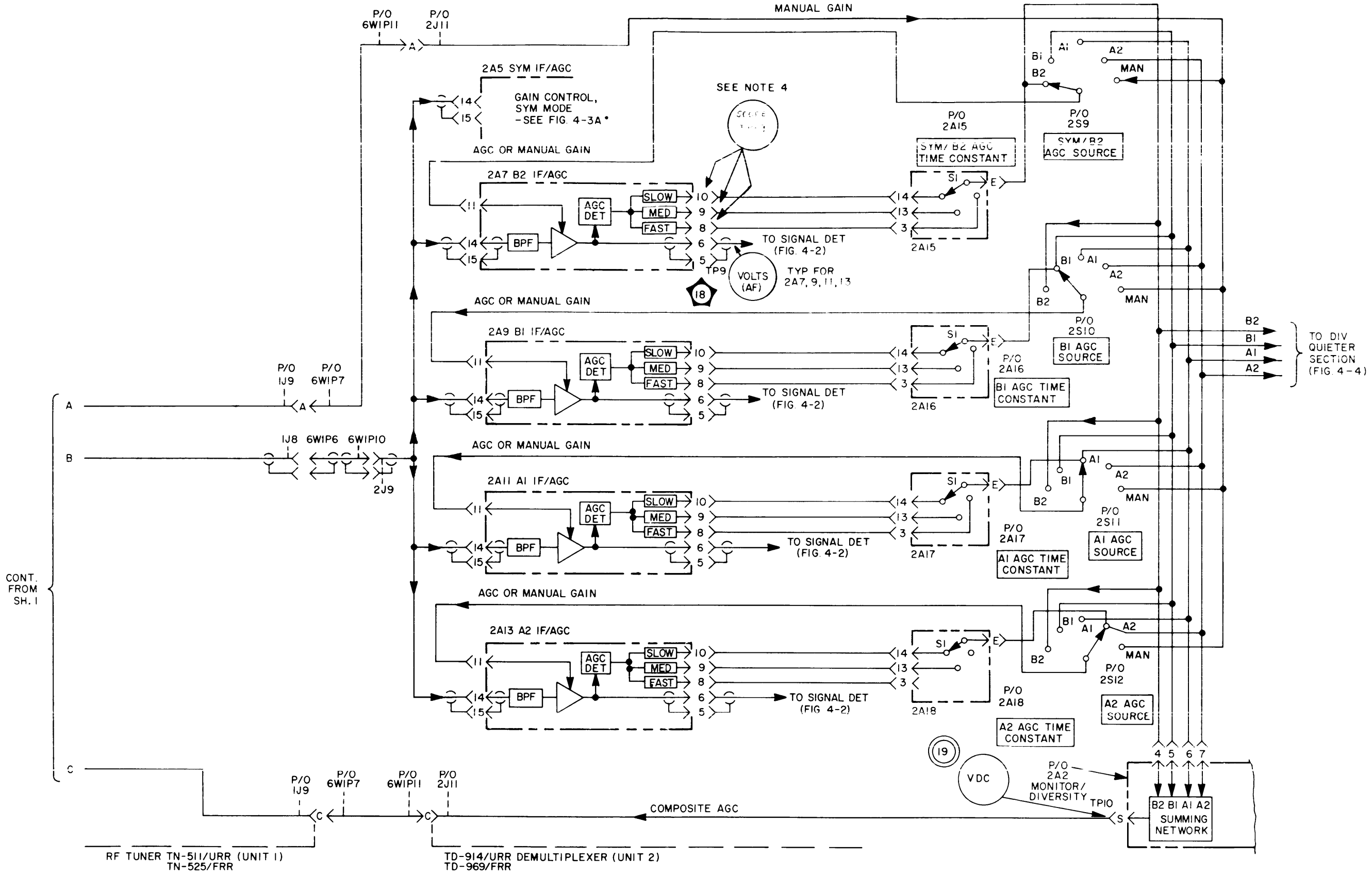
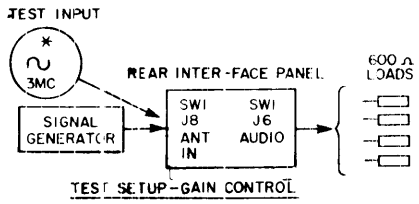


Figure 4-3. Servicing Block Diagram, Gain Control Section, ISB Mode (Sheet 2 of 2)

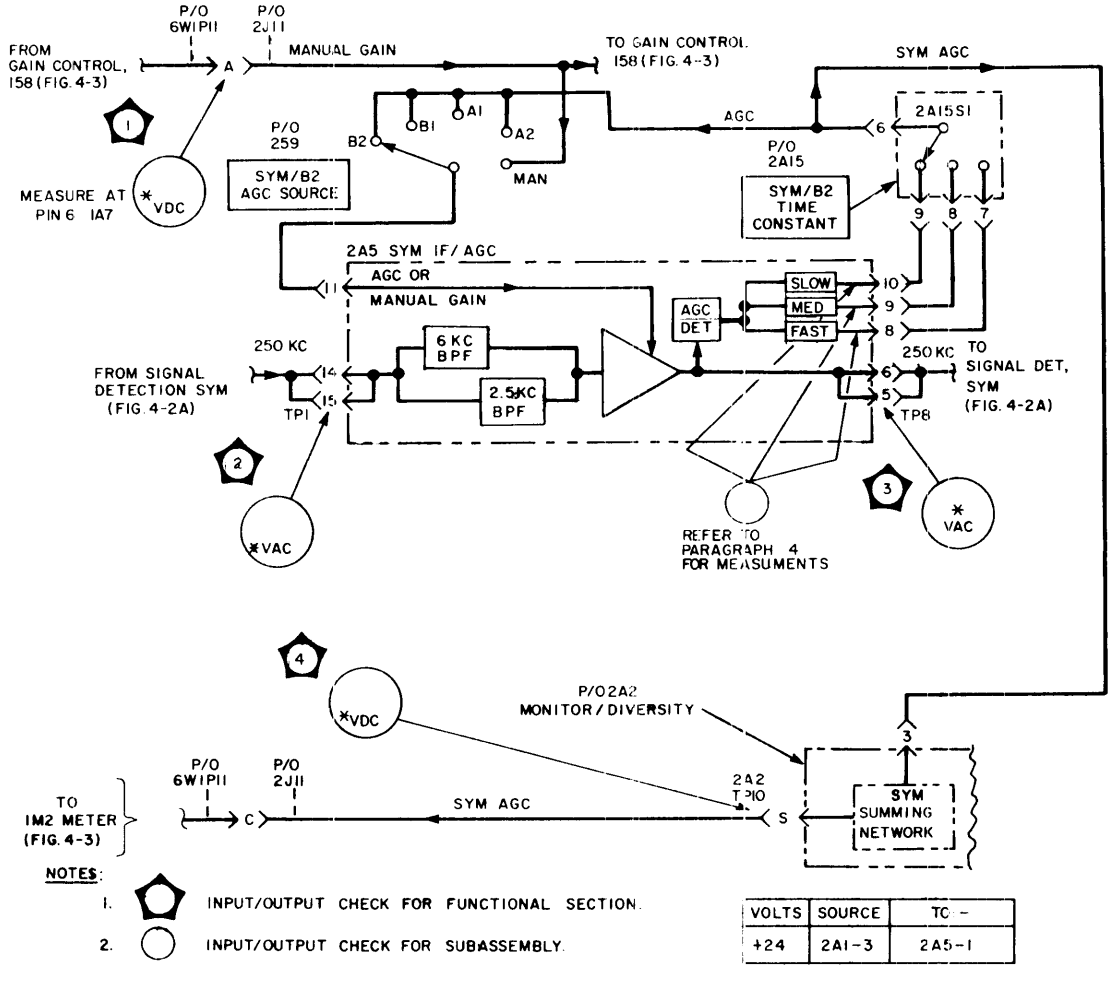


TEST SETUP-GAIN CONTROL

CONTROL POSITIONS FOR TEST

MODULAR UNIT	CONTROL	POSITION
KY-661/URR	POWER SWITCH	OFF
CV-2520(V)/URC		
OR		
CV-2521(V)/URC	POWER SWITCH	OFF
TN-511/URR	ATTENUATOR SWITCH	OFF(DOWN)
(OR TN-525/FAR)	RF GAIN KNOB(TESTS A,B)	AGC
" "	" " (TEST C)	FULLY CCW
" "	" " (TEST D)	FULLY CW
" "	SILENCER SWITCH	OFF (DOWN)
" "	POWER SWITCH	ON
" "	FUNCTION SWITCH	LOCAL
" "	COUNTER MODE SWITCH	REC
" "	BAND SWITCH	2-4
" "	TUNE AND FINE TUNE KNOBS	TO OBTAIN 3.0000 ON MEGACYCLES DISPLAY
" "	METER FUNCTION SWITCH	RF LOW
TD-914/URR	METER SENSITIVITY SWITCH	0
(OR TD-969/FRR)	SYM/B2 AGC SOURCE (TESTS A,B)	B2
" "	" " (TESTS C,D)	MAN
" "	B,A1,A2, AGC SOURCE SWITCH	OPTIONAL
" "	MODE SWITCH	AM 6KC
" "	POWER SWITCH	ON
" "	SYM/B2 LINE LEVEL ADJ KNOB	* *
" "	B1,A1,A2, LINE LEVEL ADJ KNOBS	OPTIONAL
" "	SYM/B2 AGC TIME CONSTANT SWITCH	SLOW
" "	B1,A1,A2, AGC TIME CONSTANT SWITCHES	OPTIONAL
0-1510/URR	POWER SWITCH	OFF

* * SET MONITOR SELECTOR SWITCH AT SYM AND ADJUST KNOB FOR "0 DBM" ON LINE DBM METER.



NOTES:

1. INPUT/OUTPUT CHECK FOR FUNCTIONAL SECTION.
2. INPUT/OUTPUT CHECK FOR SUBASSEMBLY.

VOLTS	SOURCE	TO -
+24	2A1-3	2A5-1

* SIGNAL VARIATIONS

TEST	3MC TEST INPUT (MV)	1 VDC	2 RMS	3	4 VDC
A AGC (MIN SIGNAL)	1uV	—	1mV	76mV	0V
B AGC (MAX SIGNAL)	1V	—	200mV	100mV	-.2V
C MANUAL GAIN (MIN)	500uV	+2.4V	5mV	76mV	—
D MANUAL GAIN (MAX)	500uV	0V	2V	410mV	—

Figure 4-3A. Servicing Block Diagram, Gain Control Section, SYM Mode

600 Ω LOADS
SYM/B2
B1
A1
A2

600 Ω LOADS
SYM/B2
B1
A1
A2

POSITION
OFF
OFF
OFF(DOWN)
AGC
OFF(DOWN)
ON
LOCAL
REC
2-4
TO OBTAIN 3.0000 ON MEGACYCLES DISPLAY
RF HIGH
0
B2
B1
A1
A2
FAST
ISB
ON
* *
OFF
SWITCH

UNIT 2(TD-914/URR RCVR "A")

P/O 2A6 — SQUELCH IN — AUDIO OUT CH SYM/B2 — VAC (5)
P/O 2A8 — SQUELCH IN — AUDIO OUT CH B1 — VAC
P/O 2A10 — SQUELCH IN — AUDIO OUT CH A1 — VAC
P/O 2A12 — SQUELCH IN — AUDIO OUT CH A2 — VAC

TYPICAL (4) VDC
(3) VDC

2A2 DIV/MON
M N P R

RCVR "A" CHAN AGC SIGNALS FROM GAIN CONTROL SECT SEE FIG. 4-3
SYM B
B2 C
B1 D
A1 E
A2 F

COMP
H J K L
P/O 2J12

(1) VDC TYPICAL
(2) VDC TYPICAL
11 10 9 8
F H J K
P/O 2J13

RECEIVER "A" INTERCONNECT PANEL
10W1J14 DIVERSITY
B C D E
P/O 10W1P13
J B I N
10W17P1
D G E F
P/O 10W1P14

10W17

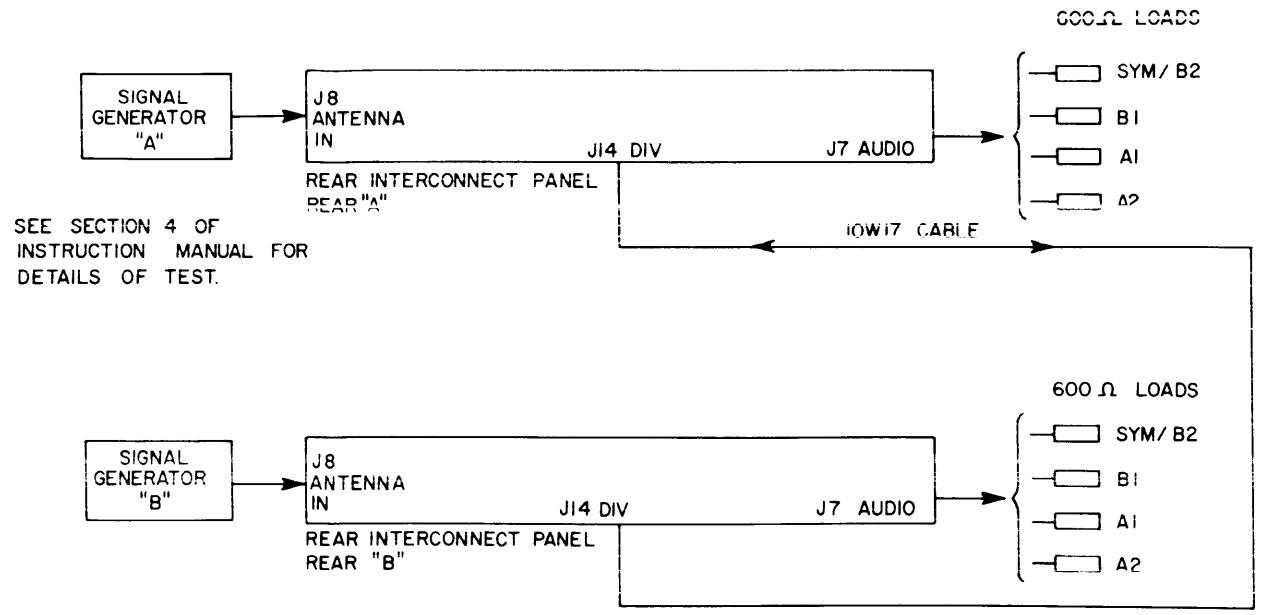
RECEIVER "B" INTERCONNECT PANEL
10W17P2
10W2J14 DIVERSITY
D G I N
J B E F
A B C D E F G H
CONT ON SH. 2

* SIGNAL VARIATIONS

TEST	SIGNAL GEN "A"	SIGNAL GEN "B"	(1) (VDC)	(2) (VDC)	(3) (VDC)	(4) (VDC)	(5) (VAC)	(6) (VDC)	(7) VDC	(8) (VAC)
A RCVR "A" WEAK RCVR "B" STRONG	10 uv	30uv	+2.5V	+1.5	+2.0V	+0.6V	0V	+3.0V	-0.6V	.78 V
B RCVR "B" WEAK RCVR "A" STRONG	30 uv	10 uv	+3.0V	+2.0V	+1.5V	-0.6V	.78V	+2.5V	+0.6V	0V

Figure 4-4. Servicing Block Diagram, Diversity Quieter Section (Sheet 1 of 2)

011690392



TEST SETUP-DIVERSITY QUIETER
CONTROL POSITION FOR TEST

MODULAR UNIT	CONTROL	POSITION
KY-661/URR (UNITS 4 & 8)	POWER SWITCHES	OFF
CV-2321(V)/URC	POWER SWITCH	OFF
TN-511/URR (UNITS 1 & 5)	ATTENUATOR SWITCH	OFF(DOWN)
	RF GAIN-KNOB	AGC
	SILENCER SWITCH	OFF(DOWN)
	POWER SWITCH	ON
	FUNCTION SWITCH	LOCAL
	COUNTER MODE SWITCH	REC
	BAND SWITCH	2-4
	TUNE AND FINE TUNE KNOBS	TO OBTAIN 3.0000 ON MEGACYCLES DISPLAY
	METER FUNCTION SWITCH	RF HIGH
TD-914/URR (UNITS 2 & 6)	METER SENSITIVITY SWITCH	0
	SYM/B2 AGC SOURCE SWITCH	B2
	B1 AGC SOURCE SWITCH	B1
	A1 " " "	A1
	A2 " " "	A2
	AGC TIME CONSTANT SWITCH (ALL)	FAST
	MODE SWITCH	ISB
	POWER SWITCH	ON
	LINE LEVEL ADJ KNOBS (ALL)	* *
O-1510/URR (UNITS 3 & 7)	POWER SWITCH	OFF

* * ADJUST EACH KNOB FOR "0" dbm ON LINE DBM METER USING MONITOR SELECTOR SWITCH

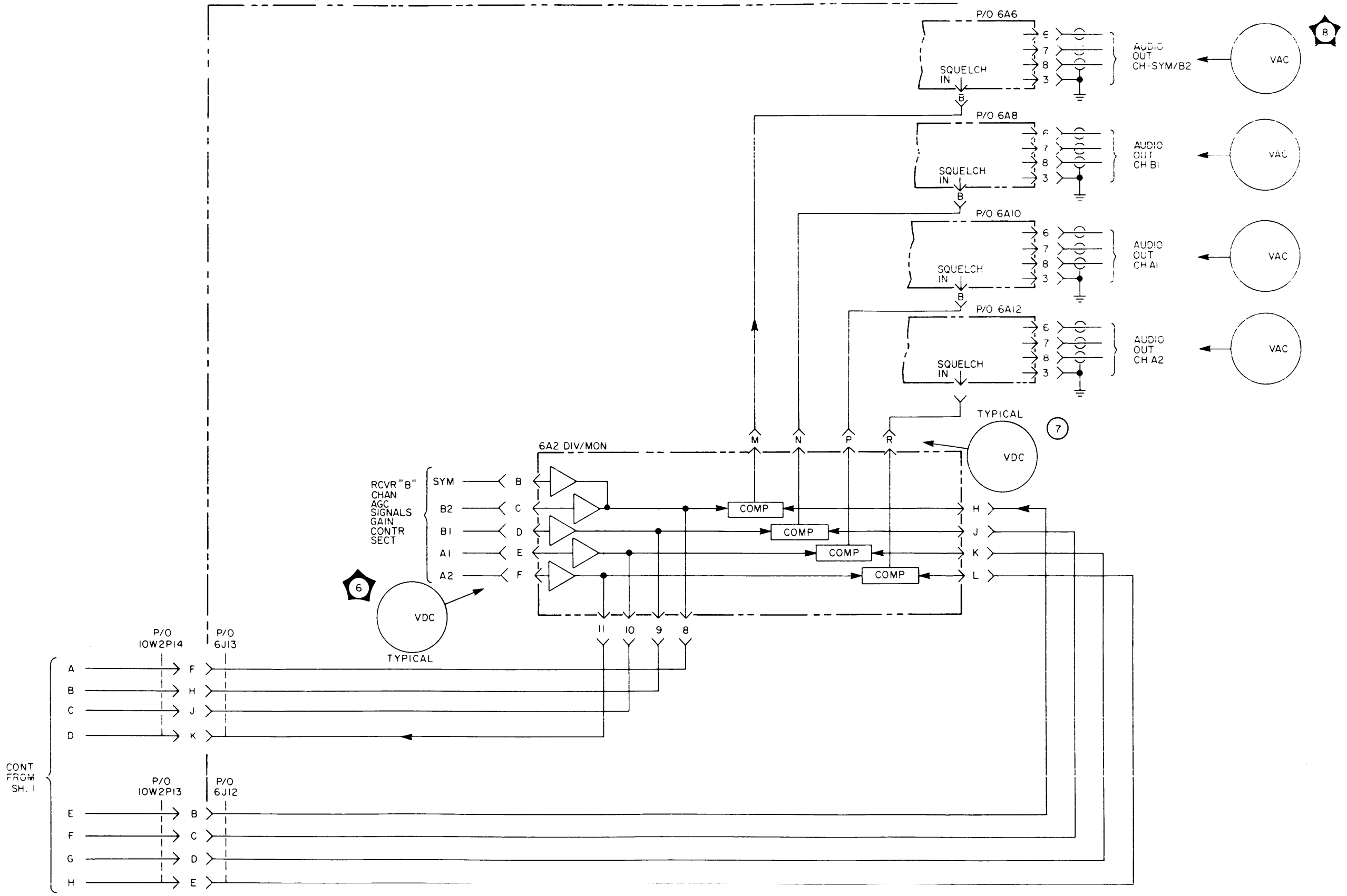


Figure 4-4. Servicing Block Diagram, Diversity Quieter Section (Sheet 2 of 2)

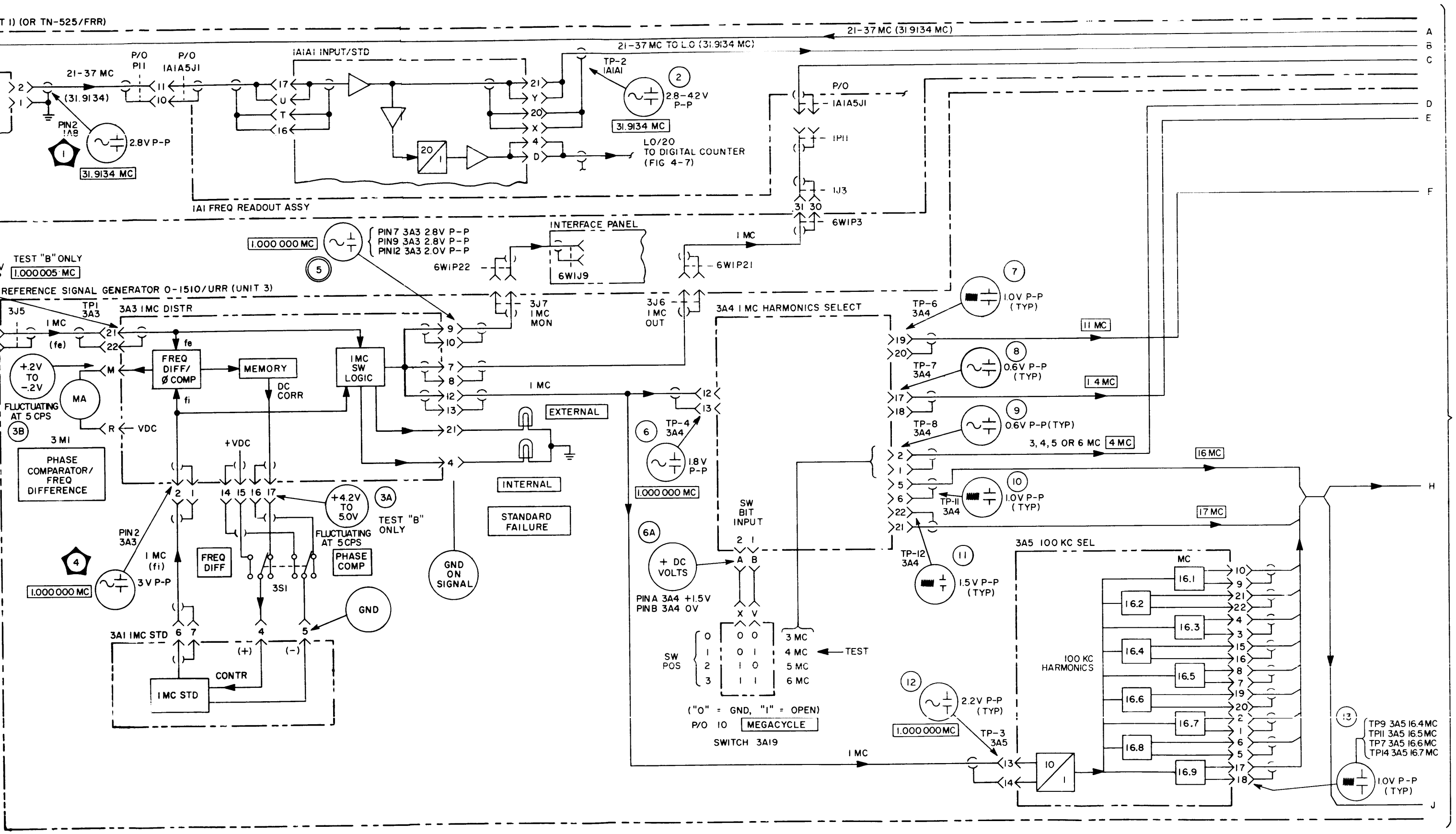
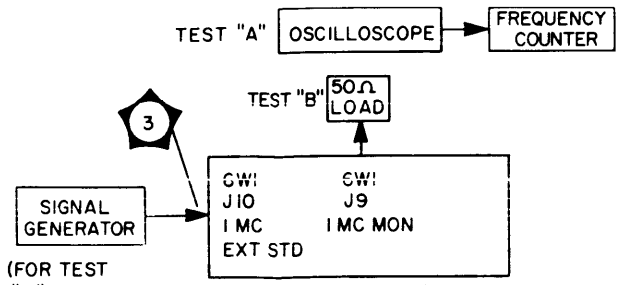


Figure 4-5. Servicing Block Diagram, Synthesizer/Phase Lock Section (Sheet 1 of 3)



SET AT 1.000 005 Hz MC @ 1.0 VRMS

TEST SETUP - SYNTHESIZER/PHASE LOCK

CONTROL POSITIONS FOR TEST *

MODULAR UNIT	CONTROL	POSITION
KY-661/URR	POWER SWITCH	OFF
CV-2520(V)/URC (OR CV-2521(V)/URC	POWER SWITCH	OFF
TN-511/URR (OR TN-525/FRR)	POWER SWITCH	ON
"	FUNCTION SWITCH	SYN
"	COUNTER MODE SWITCH	REC
"	BAND SWITCH	8-16
0-1510/URR	10 MEGACYCLE SWITCH	1
"	1 " "	3
"	0.1 " "	4
"	.01 " "	5
"	.001 " "	6
"	.0001 " "	7
"	PHASE COMPARATOR/ FREQ DIFFERENCE SW (TEST "A" & "C")	PHASE COMPARATOR
	(TEST "B")	FREQ DIFFERENCE
"	POWER SWITCH	ON

* POSITIONS OF CONTROLS NOT LISTED ARE OPTIONAL

NOTES

1 ⬠ INPUT/OUTPUT CHECKS FOR FUNCTIONAL SECTION

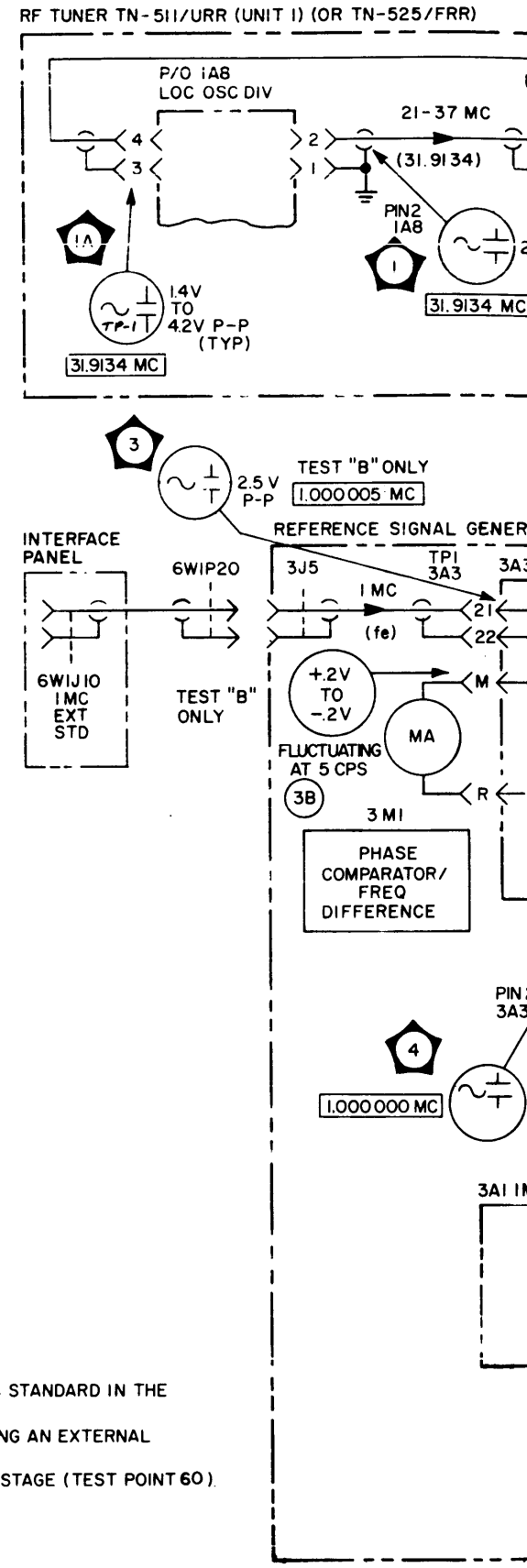
◎ INPUT/OUTPUT CHECKS FOR MODULAR UNITS

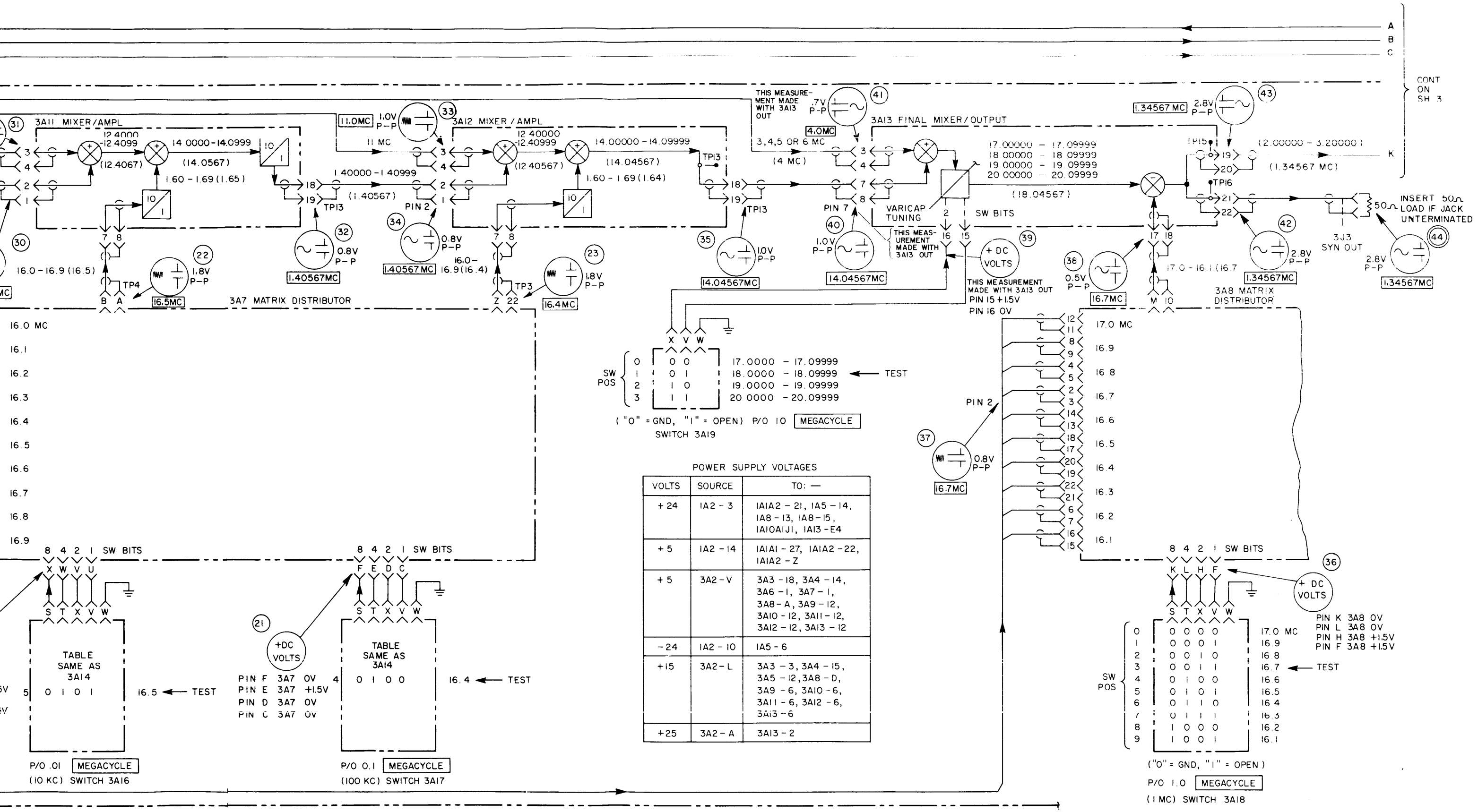
○ INPUT/OUTPUT CHECKS FOR SUBASSEMBLIES

2 TEST "A" IS A GENERAL OVERALL TEST USING THE INTERNAL 1MC STANDARD IN THE 0-1510/URR AND SYNCHRONIZING THE RECEIVER ON 13.4567 MC.

TEST "B" TESTS THE 1-MC AUTOMATIC TRANSFER SWITCHING, USING AN EXTERNAL 1 MC STANDARD (TEST POINTS 3, 3A & 3B).

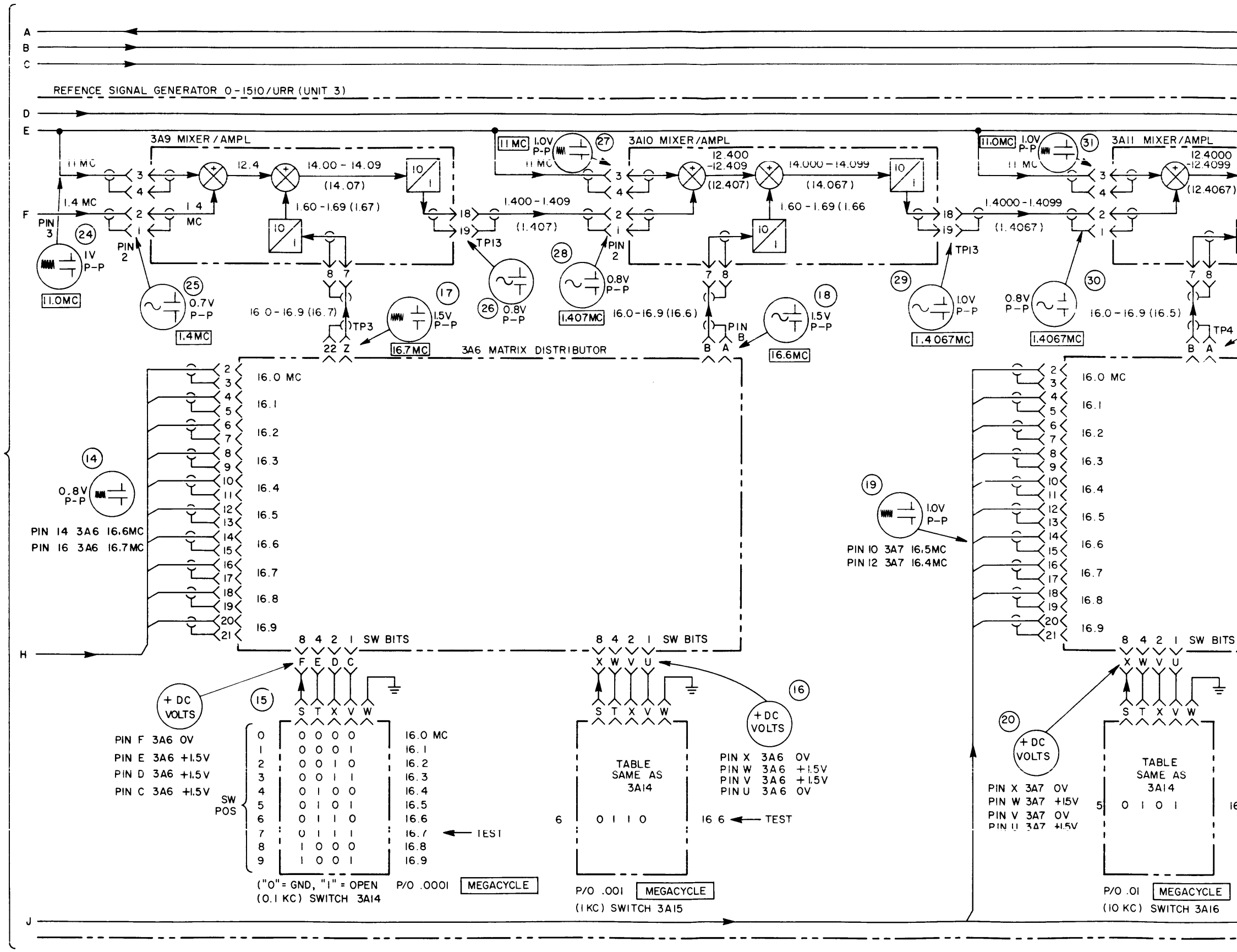
TEST "C" TESTS THE PULL-IN FUNCTIONING OF THE PHASE LOCK STAGE (TEST POINT 60).





VOLTS	SOURCE	TO: —
+24	1A2 - 3	1A1A2 - 21, 1A5 - 14, 1A8 - 13, 1A8 - 15, 1A10A1J1, 1A13 - E4
+5	1A2 - 14	1A1A1 - 27, 1A1A2 - 22, 1A1A2 - Z
+5	3A2 - V	3A3 - 18, 3A4 - 14, 3A6 - 1, 3A7 - 1, 3A8 - A, 3A9 - 12, 3A10 - 12, 3A11 - 12, 3A12 - 12, 3A13 - 12
-24	1A2 - 10	1A5 - 6
+15	3A2 - L	3A3 - 3, 3A4 - 15, 3A5 - 12, 3A8 - D, 3A9 - 6, 3A10 - 6, 3A11 - 6, 3A12 - 6, 3A13 - 6
+25	3A2 - A	3A13 - 2

Figure 4-5. Servicing Block Diagram, Synthesizer/Phase Lock Section (Sheet 2 of 3)


A
B
C
REFENCE SIGNAL GENERATOR 0-1510/URR (UNIT 3)
D
E
F
H
J
CONT FROM SH. 1
3A9 MIXER/AMPL
11 MC
1.4 MC
PIN 3
PIN 2
1.4 MC
12.4
14.00 - 14.09
(14.07)
1.60 - 1.69 (1.67)
24
1V P-P
11.0MC
25
0.7V P-P
1.4MC
16.0 - 16.9 (16.7)
TP3
17
1.5V P-P
16.7MC
26
0.8V P-P
TP13
3A10 MIXER/AMPL
11.1MC
1.0V P-P
27
1.400 - 1.409
(1.407)
28
0.8V P-P
1.407MC
16.0 - 16.9 (16.6)
12.400 -12.409
(12.407)
14.000 - 14.099
(14.067)
1.60 - 1.69 (1.66
29
1.0V P-P
1.4067MC
3A11 MIXER/AMPL
11.0MC
1.0V P-P
31
1.4000 - 1.4099
(1.4067)
30
0.8V P-P
1.4067MC
16.0 - 16.9 (16.5)
TP4
TP13
18
1.5V P-P
16.6MC
PIN B
3A6 MATRIX DISTRIBUTOR
16.0 MC
16.1
16.2
16.3
16.4
16.5
16.6
16.7
16.8
16.9
14
0.8V P-P
PIN 14 3A6 16.6MC
PIN 16 3A6 16.7MC
19
1.0V P-P
PIN 10 3A7 16.5MC
PIN 12 3A7 16.4MC
8 4 2 1 SW BITS
F E D C
S T X V W
15
+ DC VOLTS
PIN F 3A6 0V
PIN E 3A6 +1.5V
PIN D 3A6 +1.5V
PIN C 3A6 +1.5V
SW POS
0 0 0 0 16.0 MC
0 0 0 1 16.1
0 0 1 0 16.2
0 0 1 1 16.3
0 1 0 0 16.4
0 1 0 1 16.5
0 1 1 0 16.6
0 1 1 1 16.7
1 0 0 0 16.8
1 0 0 1 16.9
TEST
("0" = GND, "1" = OPEN
(0.1 KC) SWITCH 3A14
P/O .0001 MEGACYCLE
8 4 2 1 SW BITS
X W V U
S T X V W
16
+DC VOLTS
PIN X 3A6 0V
PIN W 3A6 +1.5V
PIN V 3A6 +1.5V
PIN U 3A6 0V
TABLE SAME AS 3A14
6
0 1 1 0
16 6 TEST
P/O .001 MEGACYCLE
(1KC) SWITCH 3A15
8 4 2 1 SW BITS
X W V U
S T X V W
20
+ DC VOLTS
PIN X 3A7 0V
PIN W 3A7 +1.5V
PIN V 3A7 0V
PIN U 3A7 +1.5V
TABLE SAME AS 3A14
5
0 1 0 1
P/O .01 MEGACYCLE
(10 KC) SWITCH 3A16

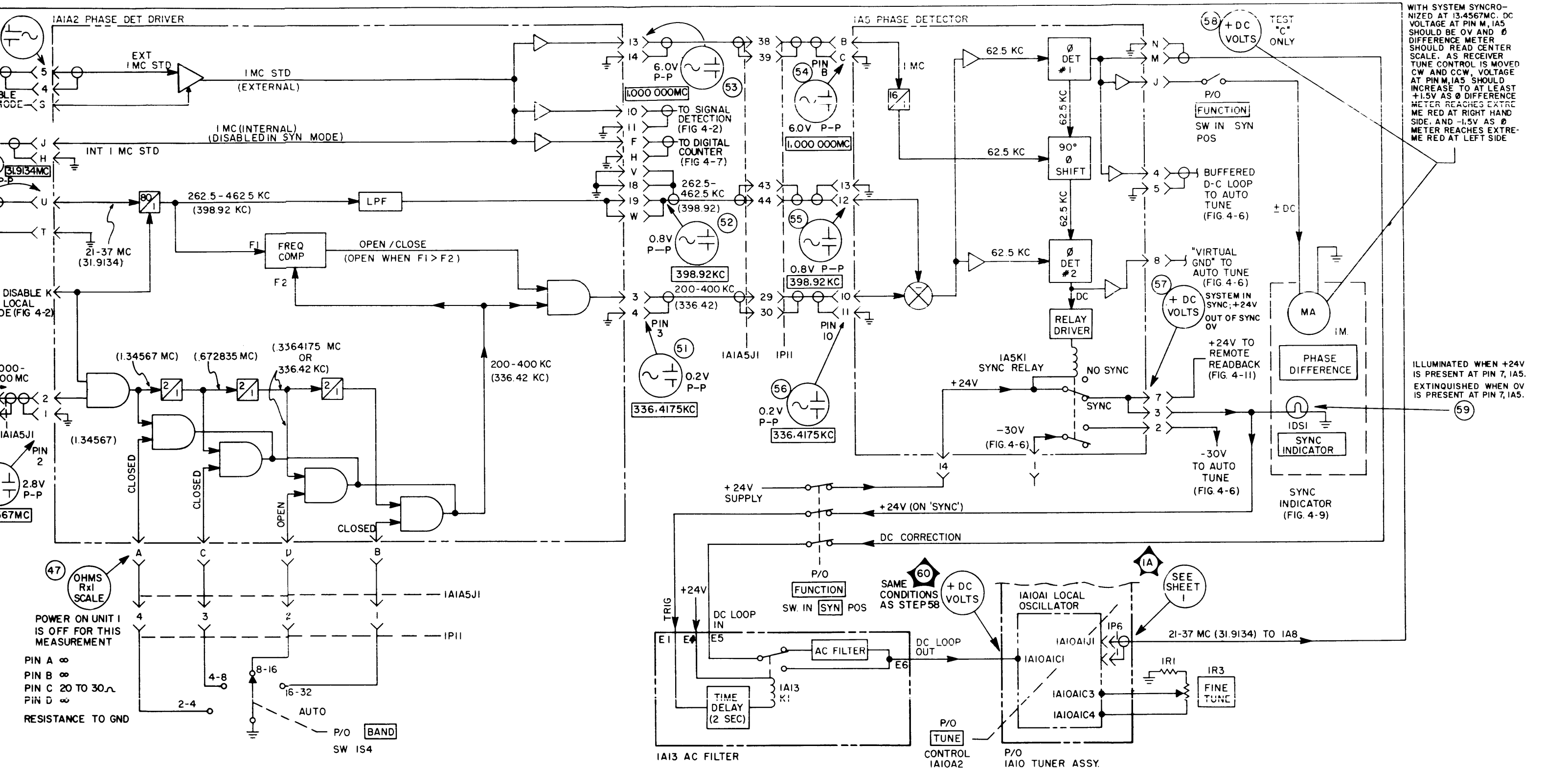
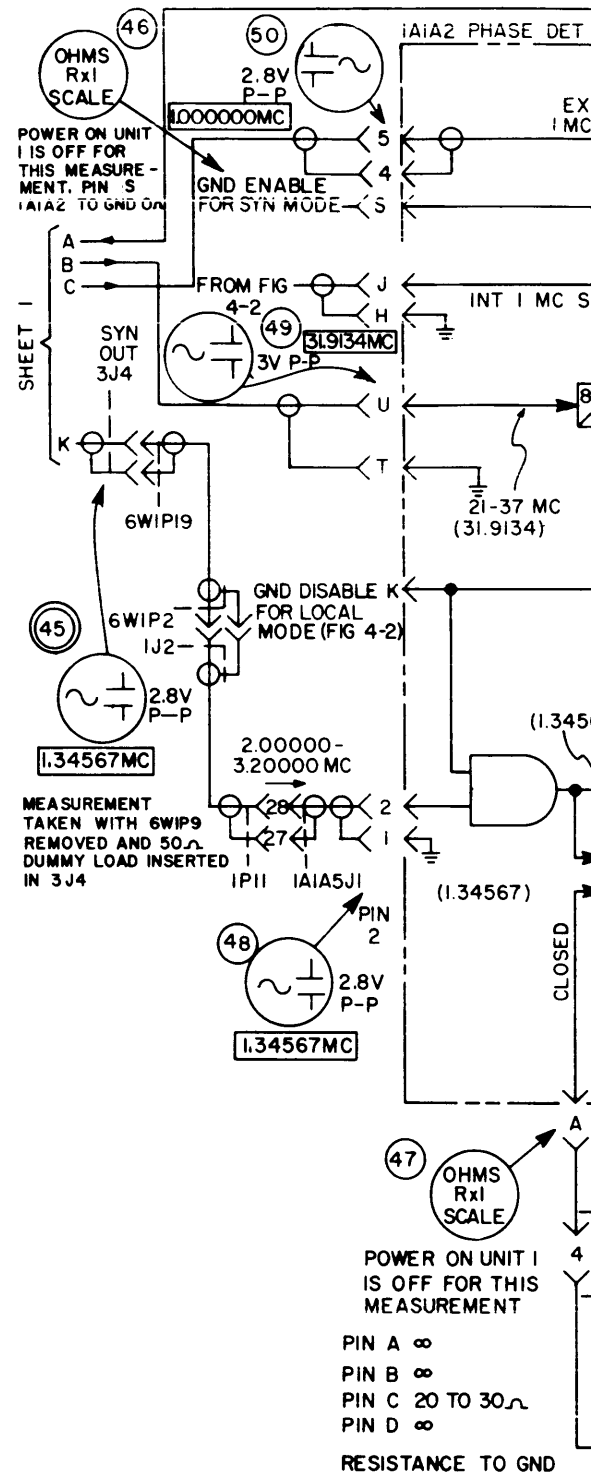


Figure 4-5. Servicing Block Diagram, Synthesizer/Phase Lock Section (Sheet 3 of 3)


1A1A2 PHASE DET
OHMS Rx1 SCALE
46
50
2.8V P-P
1000000MC
POWER ON UNIT 1 IS OFF FOR THIS MEASUREMENT. PIN S 1A1A2 TO GND ON
GND ENABLE FOR SYN MODE
FROM FIG 4-2
INT 1 MC S
SHEET 1
SYN OUT 3J4
49
31.9134MC
3V P-P
6W1P19
21-37 MC (31.9134)
GND DISABLE FOR LOCAL MODE (FIG 4-2)
6W1P2
1J2
45
2.8V P-P
1.34567MC
2.00000-3.20000 MC
MEASUREMENT TAKEN WITH 6W1P9 REMOVED AND 50Ω DUMMY LOAD INSERTED IN 3J4
1P11
1A1A5J1
(1.34567)
CLOSED
48
PIN 2
2.8V P-P
1.34567MC
47
OHMS Rx1 SCALE
POWER ON UNIT 1 IS OFF FOR THIS MEASUREMENT
PIN A ∞
PIN B ∞
PIN C 20 TO 30Ω
PIN D ∞
RESISTANCE TO GND

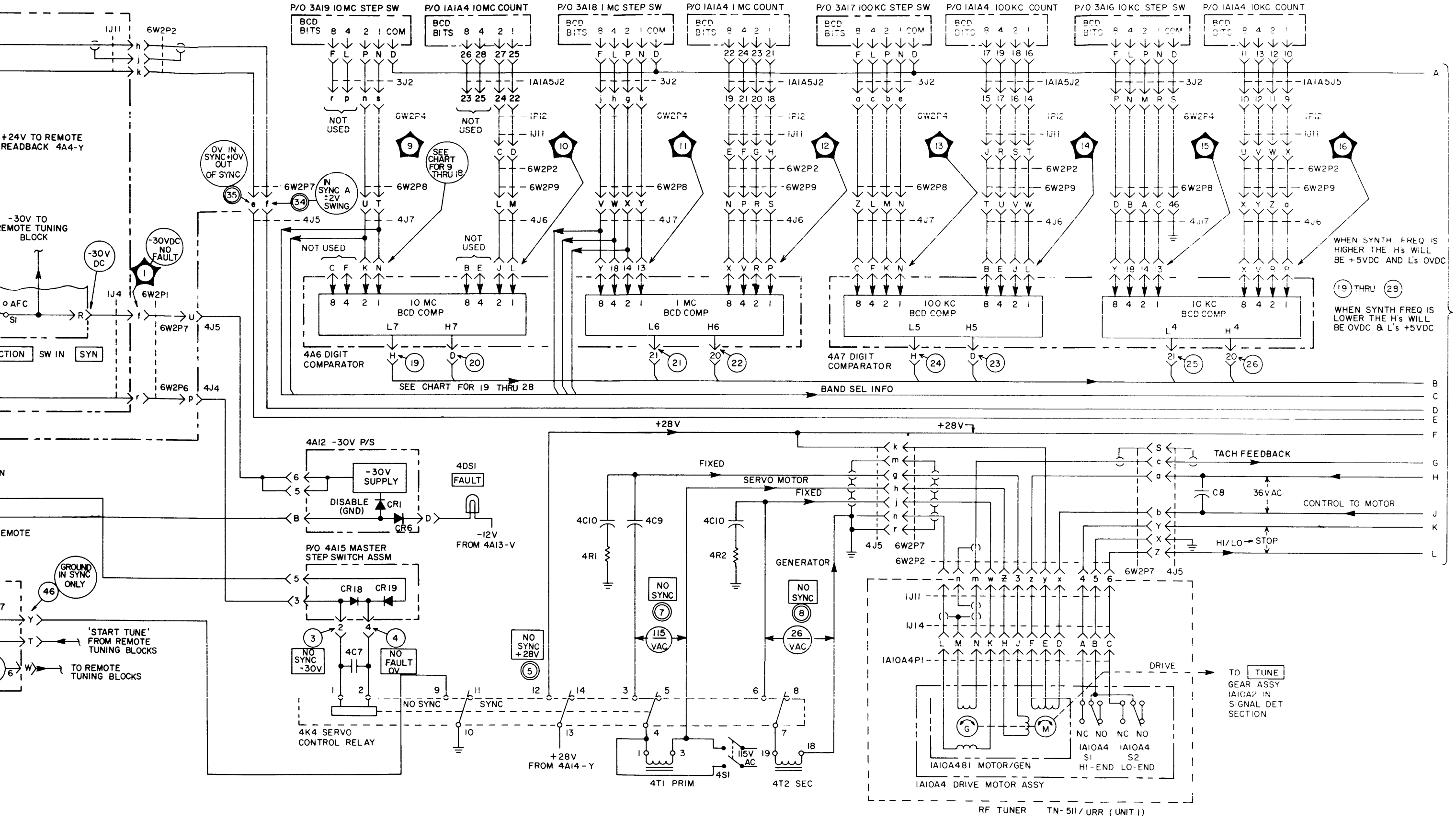


Figure 4-6. Servicing Block Diagram, Automatic Tuning Section (Sheet 1 of 2)

CONTROL POSITIONS FOR TEST *

MODULAR UNIT	CONTROL	POSITION
CV-2520(V)/URC OR CV-2521(V)/URC	POWER SWITCH	ON
KY-661/URR	POWER SWITCH	(SEE TEST PROCEDURE BELOW)
TN-511/URR (OR TN-525/FRR	POWER SWITCH	ON
"	FUNCTION SWITCH	SYN
"	COUNTER MODE SW.	REC
"	BAND SWITCH	AUTO
"	TUNE AND FINE TUNE KNOBS	(SEE TEST PROCEDURE BELOW)
O-1510/URR	POWER SWITCH	ON
"	PHASE COMPARATOR/ FREQ. DIFFERENCE SW.	PHASE COMPARATOR
"	SIX MEGACYCLE SWITCHES	(SEE TEST PROCEDURE BELOW)

* POSITIONS OF CONTROLS NOT LISTED ARE OPTIONAL.

TEST PROCEDURE: (REFER TO TIMING CHART, FOR MEASUREMENTS.) AND WAVE FORMS.

I. FAST TUNING TESTS

A (HIGH-TO-LOW): FOR FIRST MEASUREMENT, SET KY-661/URR POWER SWITCH AT OFF AND THE SIX O-1510/URR MEGACYCLE SWITCHES FOR 06.6897 MC, THEN SET TUNE & FINE TUNE KNOBS TO BRING "31.9768" ON TN-511/URR MEGACYCLE DISPLAY. FOR EACH NEW MEASUREMENT, SET KY-661/URR POWER SWITCH AT OFF, TUNE & FINE TUNE KNOBS FOR 31.9768 MC AND KY-661/URR POWER SWITCH AT ON.

B (LOW-TO-HIGH): FOR FIRST MEASUREMENT, SET KY-661/URR POWER SWITCH AT OFF AND THE SIX O-1510/URR MEGACYCLE SWITCHES FOR 31.9768 MC; THEN SET TUNE & FINE TUNE KNOBS TO BRING "06.6897" ON TN-511/URR MEGACYCLE DISPLAY. FOR EACH NEW MEASUREMENT, SET KY-661/URR POWER SWITCH AT OFF, TUNE & FINE TUNE KNOBS FOR 06.6897 MC AND KY-661/URR POWER SWITCH AT ON.

II SLOW TUNING TESTS

A. SYNTHESIZE SYSTEM TO ANY FREQUENCY BETWEEN 02 AND 32 MCS. WHEN TESTING FOR VOLTAGES AND WAVE FORMS HOLD TUNE CONTROL ON TN-511 SO THAT SYSTEM IS 'IN' SYNC BUT PHASE DIFFERENCE METER INDICATES IN THE RED AREA AND SERVO SYSTEM PULSING.

NOTES:

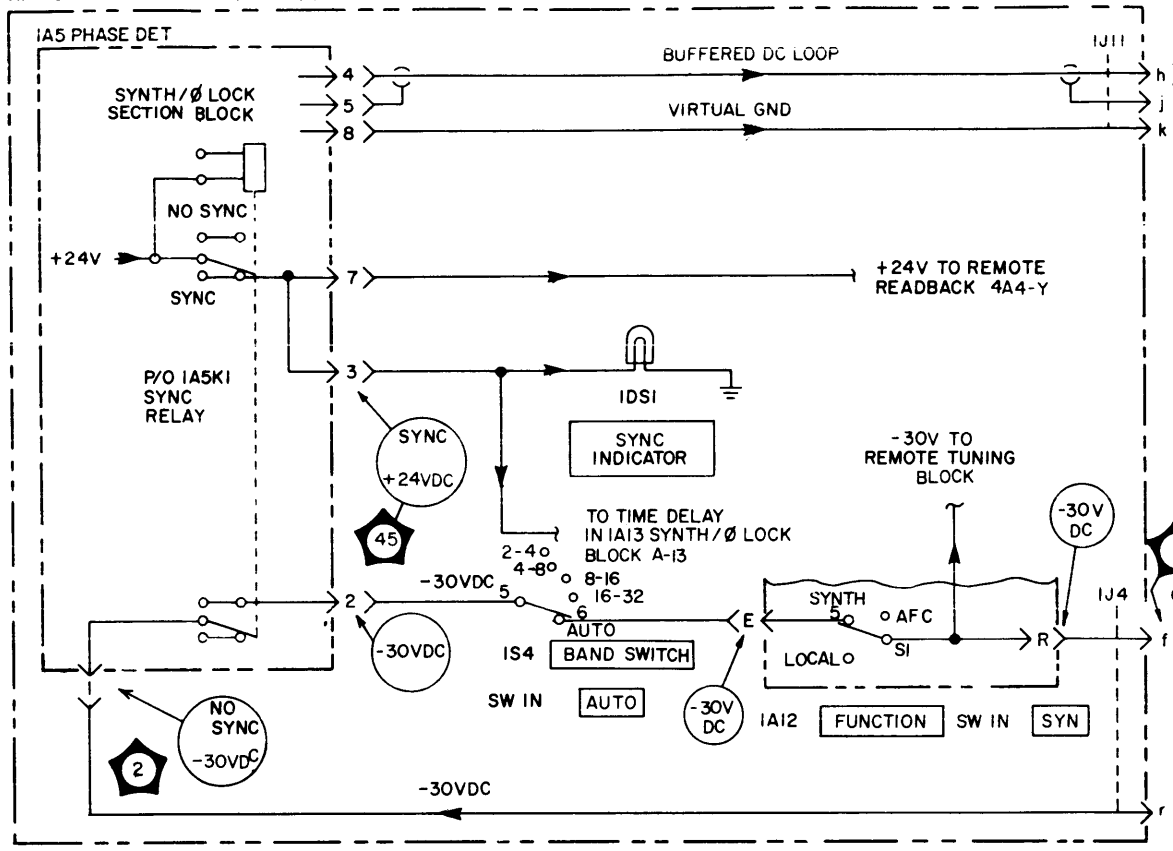
1 ⬠ INPUT/OUTPUT CHECKS FOR FUNCTIONAL SECTION

◎ INPUT/OUTPUT CHECKS FOR MODULE UNIT

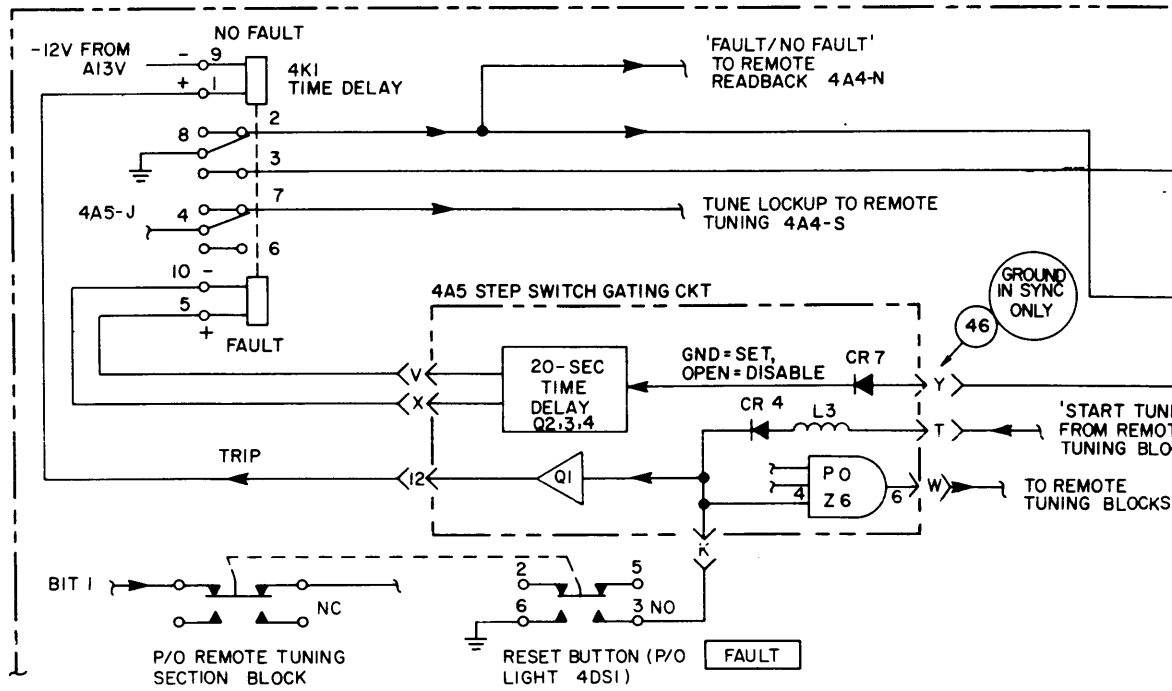
○ INPUT/OUTPUT CHECKS FOR SUBASSEMBLIES

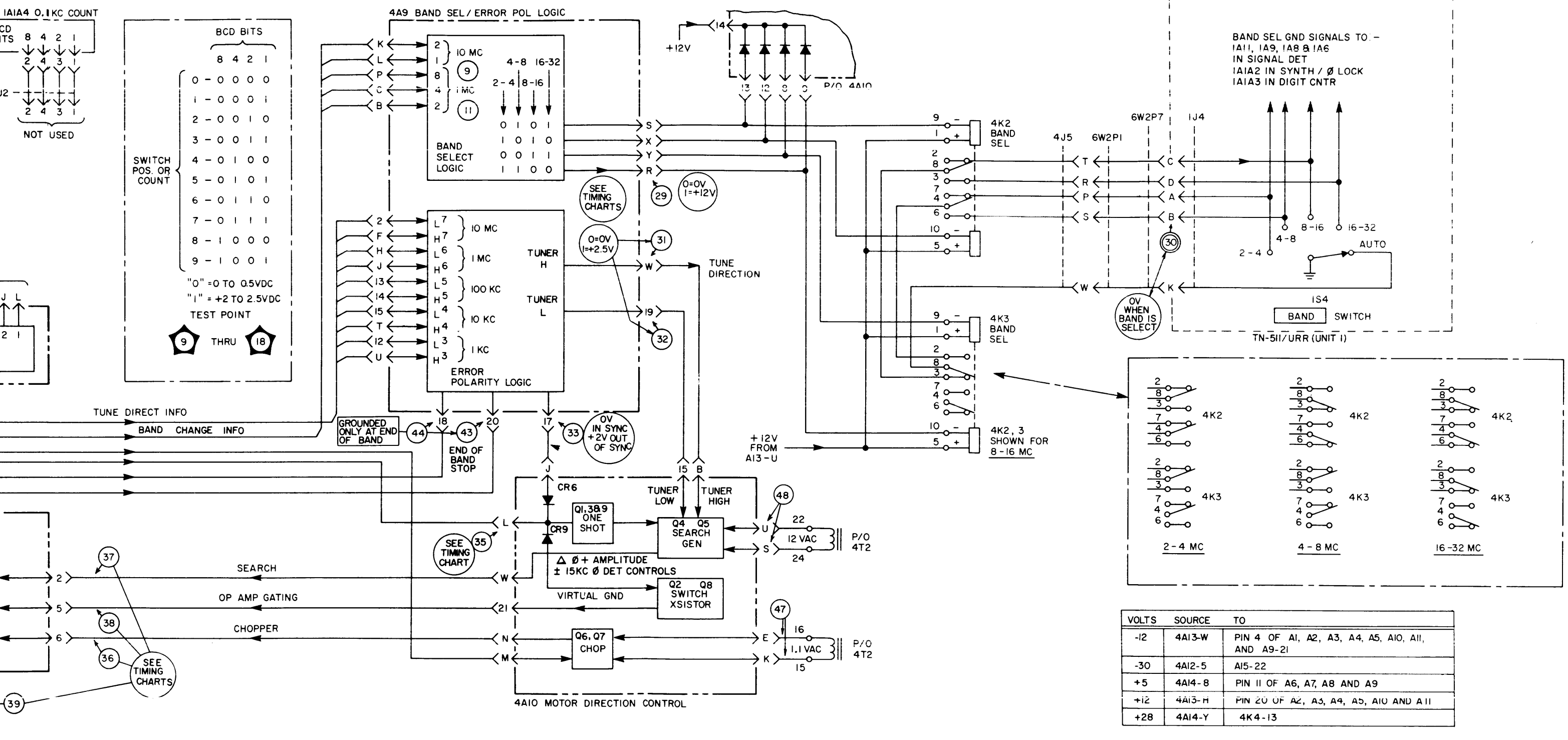
2 A DUAL TRACE SCOPE WILL HAVE TO BE USED TO COMPARE ONE WAVEFORM WITH ANOTHER ONE.

RF TUNER TN-511/URR (UNIT 1) (OR TN-525/FRR)



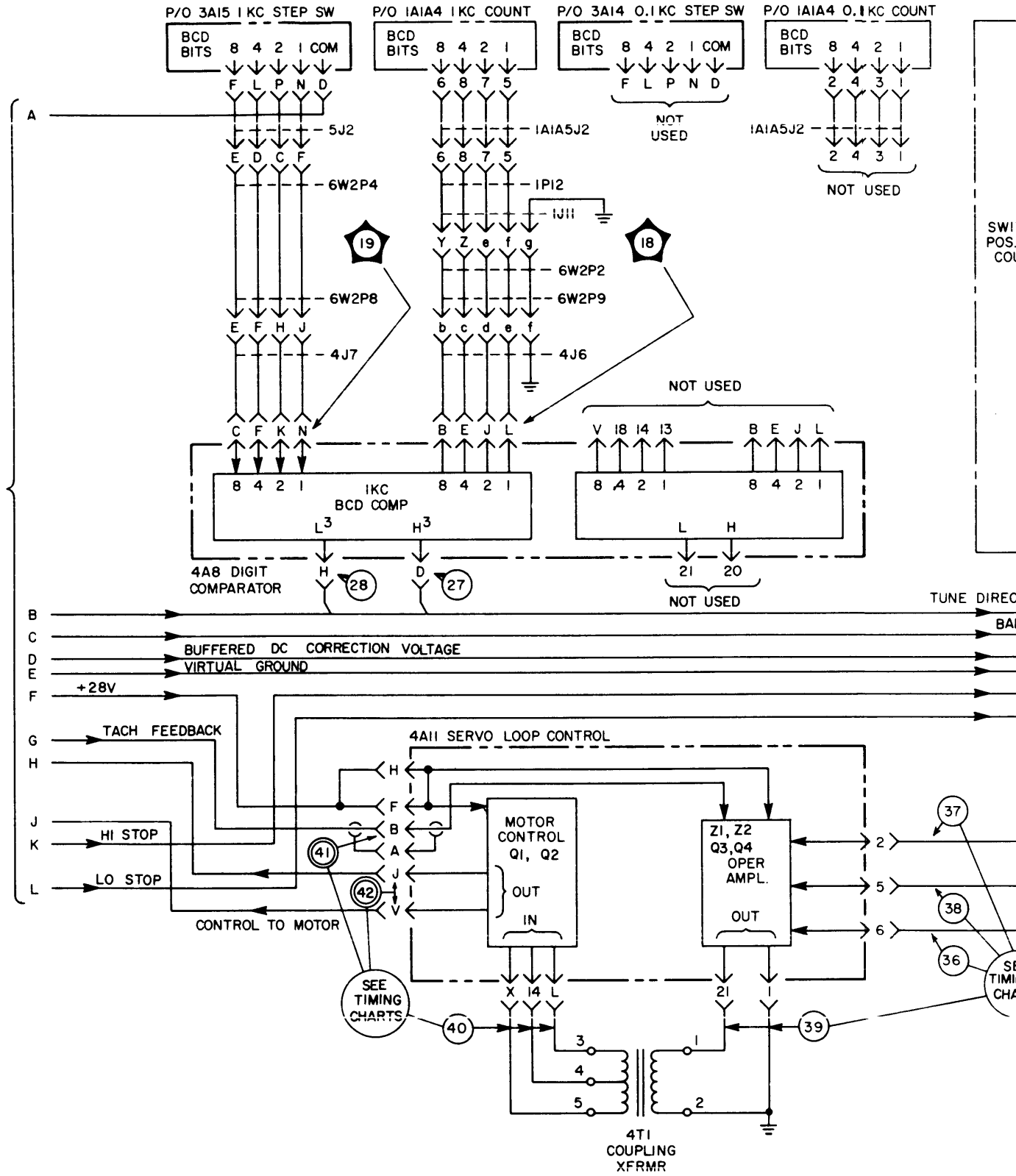
COMMAND SIGNAL DECODER KY-661/URR (UNIT 4)

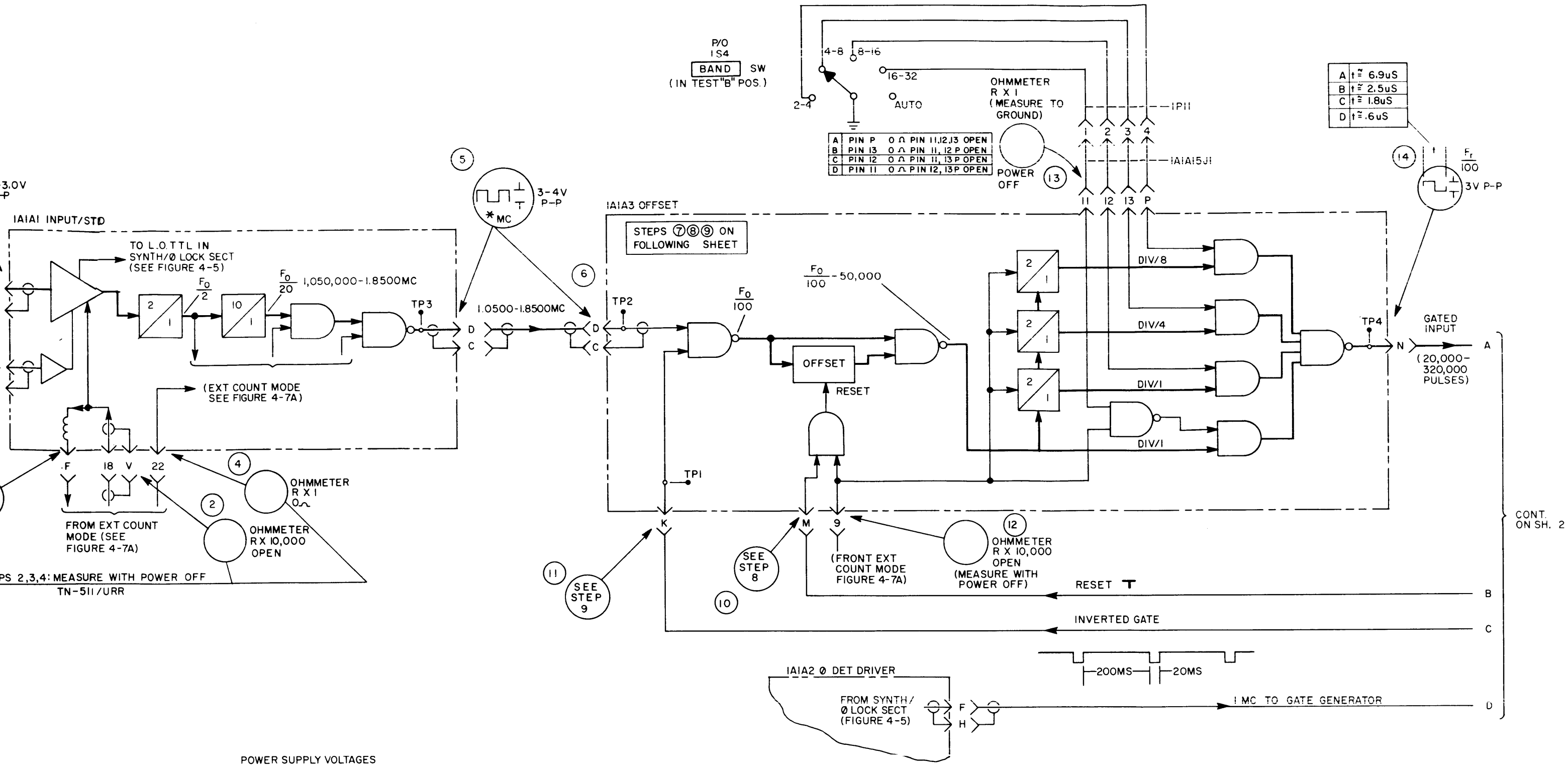




VOLTS	SOURCE	TO
-12	4A13-W	PIN 4 OF A1, A2, A3, A4, A5, A10, A11, AND A9-21
-30	4A12-5	A15-22
+5	4A14-8	PIN 11 OF A6, A7, A8 AND A9
+12	4A13-H	PIN 20 OF A2, A3, A4, A5, A10 AND A11
+28	4A14-Y	4K4-13

Figure 4-6. Servicing Block Diagram, Automatic Tuning Section (Sheet 2 of 2)


P/O 3A15 1 KC STEP SW
P/O 1A1A4 1 KC COUNT
P/O 3A14 0.1 KC STEP SW
P/O 1A1A4 0.1 KC COUNT
BCD BITS 8 4 2 1 COM
F L P N D
6 8 7 5
2 4 3 1
NOT USED
1A1A5J2
5J2
6W2P4
1P12
6W2P2
6W2P9
6W2P8
4J7
4J6
E D C F
Y Z e f g
b c d e f
C F K N
B E J L
V 18 14 13
8 4 2 1
8 A 2 1
1KC BCD COMP
L3 H3
4A8 DIGIT COMPARATOR
21 20
CONT. FROM SH. 1
TUNE DIREC
BA
BUFFERED DC CORRECTION VOLTAGE
VIRTUAL GROUND
+28V
TACH FEEDBACK
HI STOP
LO STOP
CONTROL TO MOTOR
4A11 SERVO LOOP CONTROL
MOTOR CONTROL Q1, Q2
OUT
IN
Z1, Z2 Q3,Q4 OPER AMPL.
SEE TIMING CHARTS
X 14 L
21 1
4T1 COUPLING XFRMR
SE TIMI CHA



POWER SUPPLY VOLTAGES

VOLTS	SOURCE	TO:
+.5	1A2-14	1A1A1-27, 1A1A1-2, 1A1A13-2, 1A1A4-2
+200	1A2-M	1A1A5J1-24

Figure 4-7. Servicing Block Diagram, Digital Counter Section, Receiver Mode (Sheet 1 of 2)

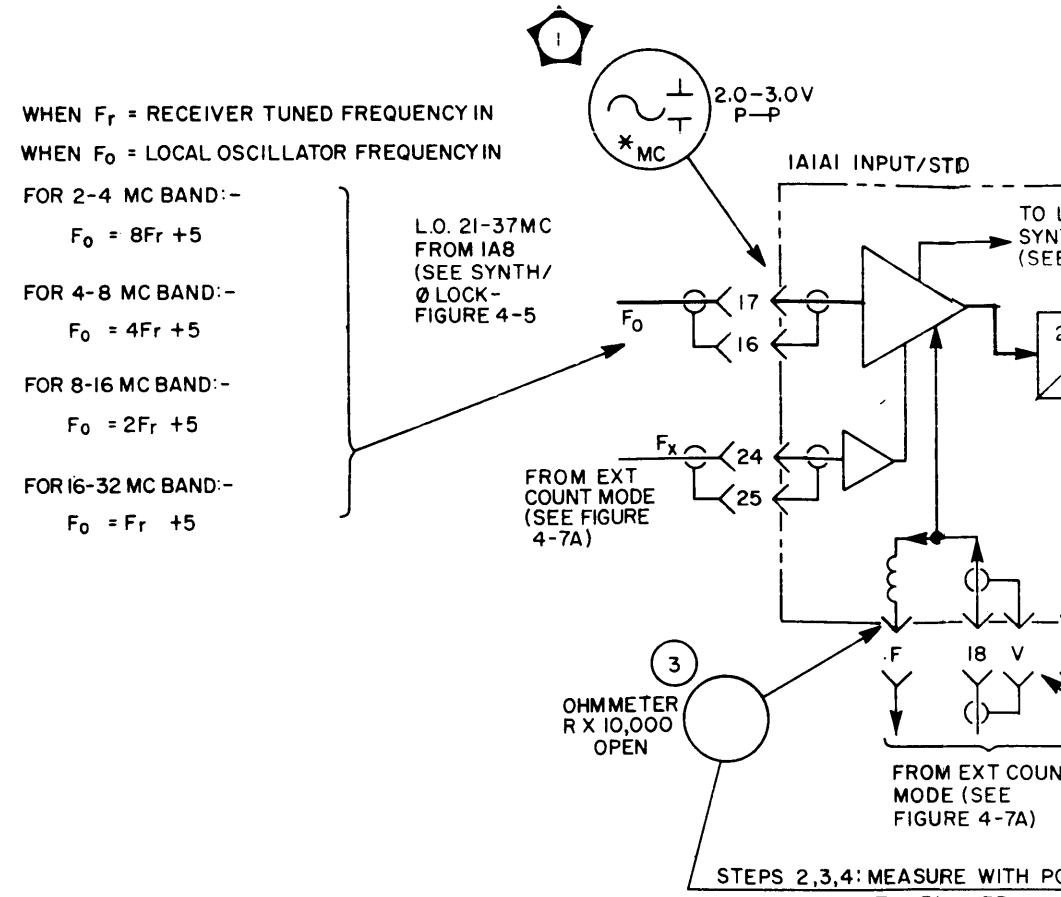
DIGITAL COUNT SECTION		
RECEIVING MODE TEST		
CONTROL POSITIONS FOR TEST		
MODULAR UNIT	CONTROL	POSITION
TN-511/URR OR TN-525/URR	POWER SWITCH	ON
	FINE TUNE	MID POSITION
	LOCK	OFF
	TUNE	ADJUST FOR FREQENCY INDICATED IN TEST TABLE
	BAND SWITCH	SEE TEST TABLE
	FUNCTION	SYN
	COUNTER MODE	REC
	OTHER CONTROLS	OPTIONAL
0-1510/URR	POWER SWITCH FREQUENCY SELECTOR OTHER CONTROLS	ON SEE TEST TABLE OPTIONAL
KY-661/URR	POWER SWITCH	OFF
TD-914/URR	POWER SWITCH	OFF
CV-2520/URC OR CV-2521/URC	POWER SWITCH	OFF

1. SET 0-1510/URR FREQUENCY SELECTORS TO TEST FREQUENCY
2. ON RF TUNER, SET BANDSWITCH TO APPROPRIATE POSITION AND ADJUST TUNE CONTROL FOR EXTERNAL COUNTER READING SPECIFIED IN TEST TABLE. SYNCRONIZE RECEIVER.
3. CARRY OUT TESTS A,B,C AND D AT EACH TEST POINT (IF APPROPRIATE) BEFORE PROCEEDING TO NEXT STEP.

* SIGNAL VARIATIONS

TEST TABLE

TEST	1S4 BAND SWITCH	① Fo INPUT (MC)	⑥ ⑤ Fo/20 (MC)	⑱ MEGACYCLE DISPLAY	⑭	⑯
A	2—4	23.1424	1.15712	2.2678	SEE TABLE AT TEST POINT ⑭	SEE INSTRUCTIONS AT STEP ⑯ AND TABLE AT ⑱
B	4—8	32.5048	1.62524	6.8762		
C	8—16	22.4572	1.12286	8.7286		
D	16-32	32.6827	1.63414	27.6827		



NOTES:

1. ⬠ INPUT/OUTPUT CHECKS FOR FUNCTIONAL SECTION
2. ◯ INPUT/OUTPUT CHECKS FOR SUBASSEMBLIES
3. HEAVY LINES INDICATE PATH OF COUNT SIGNAL

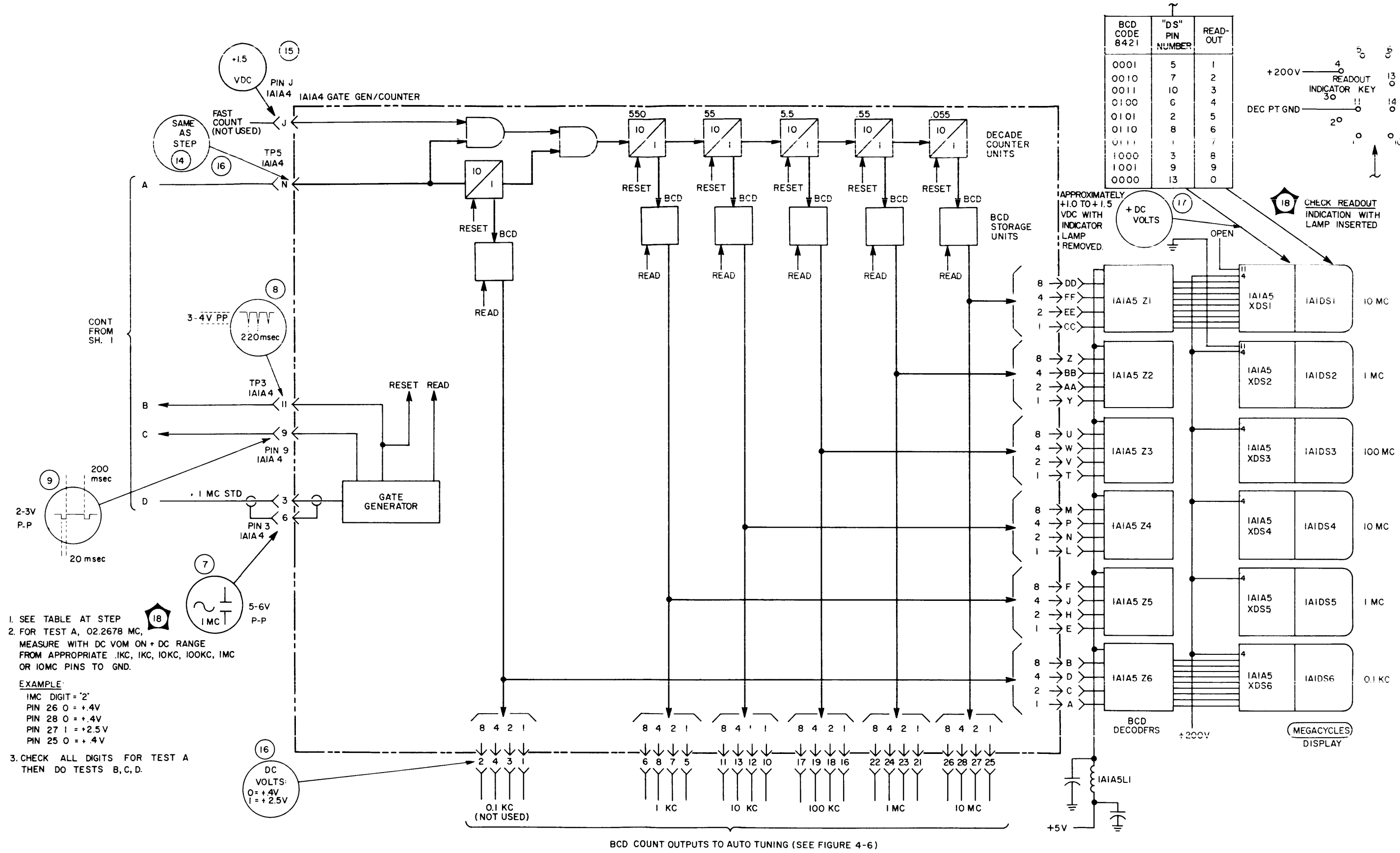
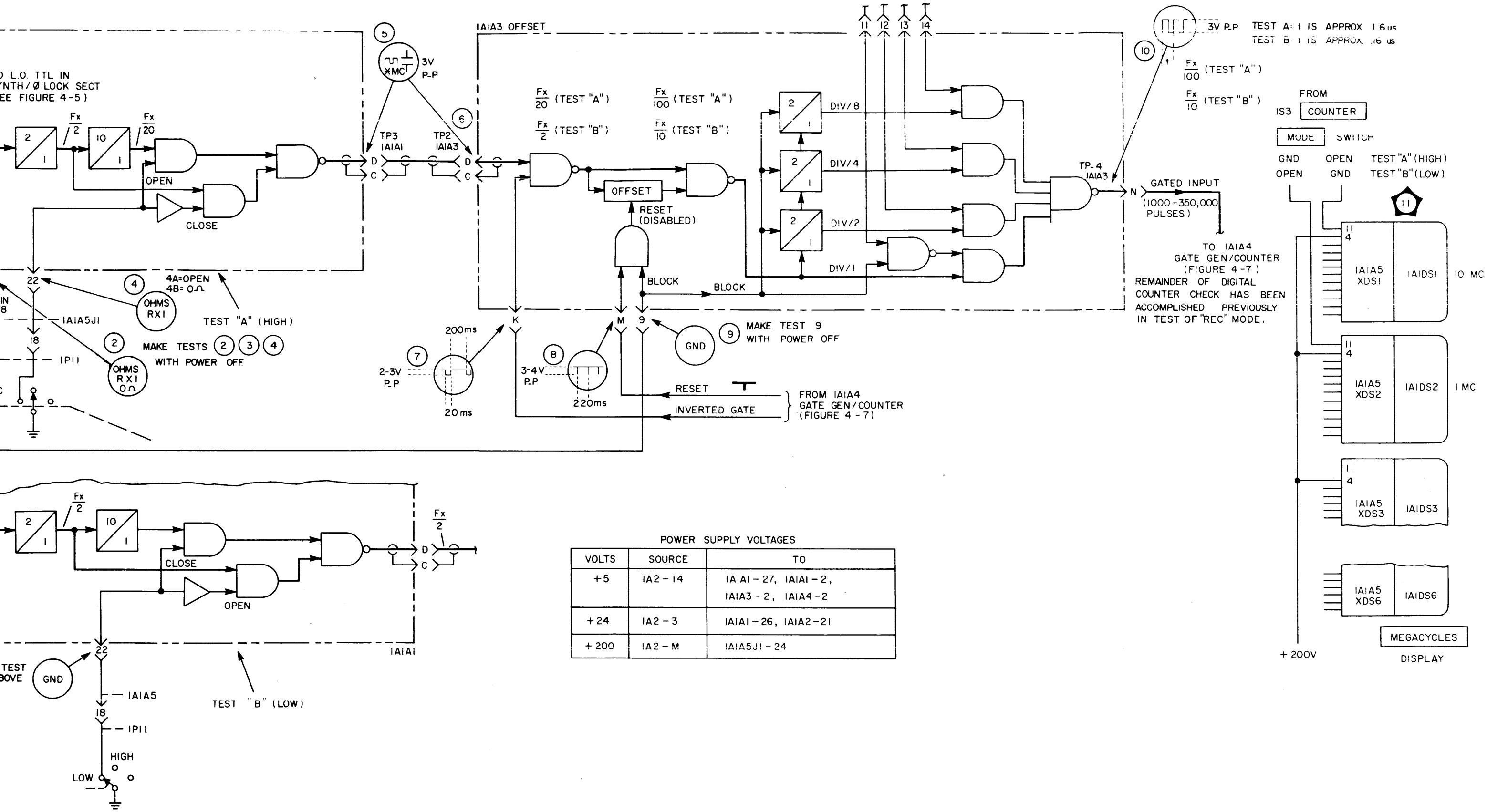


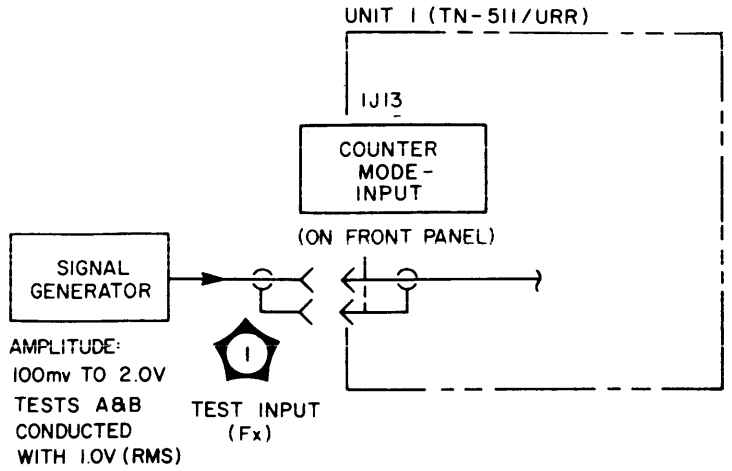
Figure 4-7. Servicing Block Diagram, Digital Counter Section, Receiver Mode (Sheet 2 of 2)



POWER SUPPLY VOLTAGES

VOLTS	SOURCE	TO
+5	IA2-14	IAIAI-27, IAIAI-2, IAIA3-2, IAIA4-2
+24	IA2-3	IAIAI-26, IAIA2-21
+200	IA2-M	IAIA5J1-24

Figure 4-7A. Servicing Block Diagram, Digital Counter Section, External Count Mode



TEST SETUP - DIGITAL COUNTER
(EXTERNAL MODE)

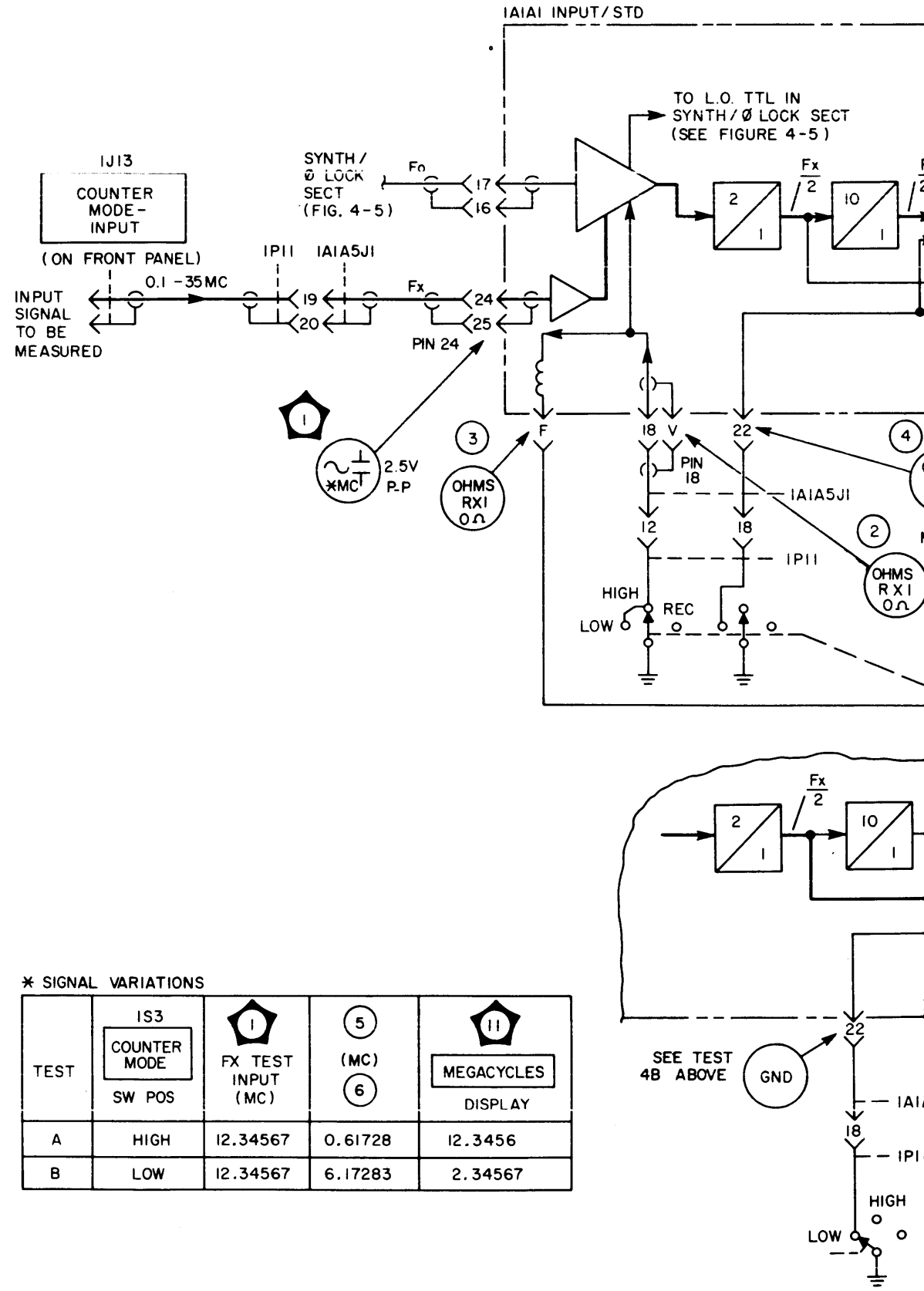
CONTROL POSITIONS FOR TEST **

MODULAR UNIT	CONTROL	POSITION
TN-511/URR OR TN-525/FRR	POWER SWITCH	ON
"	FUNCTION SWITCH	SYN
"	COUNTER MODE SW	AS SHOWN IN TEST
O-1510/URR	POWER SWITCH	ON
KY-661/URR	POWER SWITCH	OFF
CV-2520(V)/URC OR CV-2521(V)/URC	POWER SWITCH	OFF

** POSITIONS OF CONTROLS NOT SHOWN ARE OPTIONAL

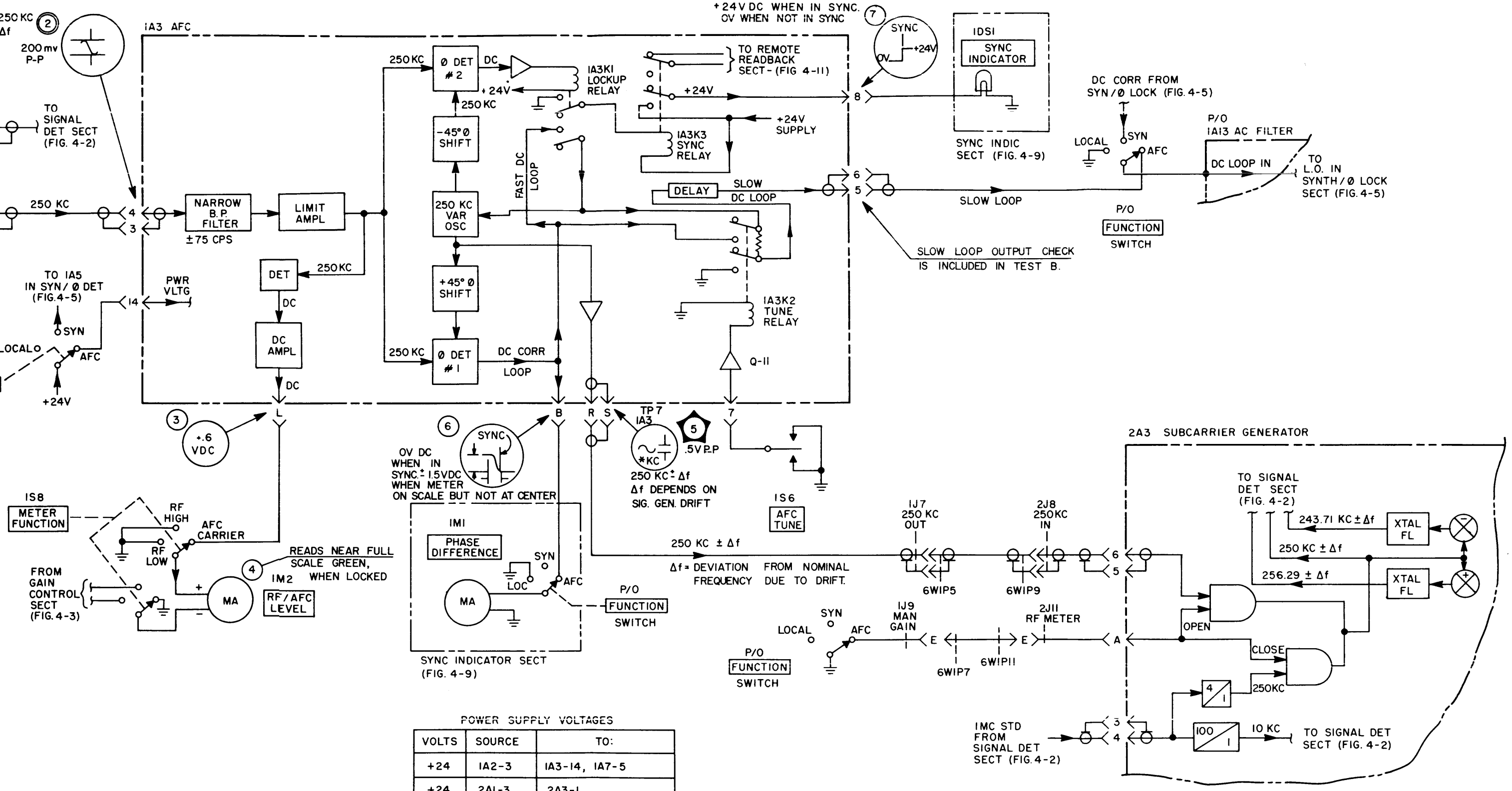
NOTES:

1. ⬠ INPUT/OUTPUT CHECKS FOR FUNCTIONAL SECTION
2. ◯ INPUT/OUTPUT CHECKS FOR SUBASSEMBLIES
3. —— HEAVY LINES INDICATE PATH OF COUNT SIGNAL
4. THE CHECK OF THE DIGITAL COUNTER SECTION IN THE "REC" MODE SHOULD BE CONDUCTED PRIOR TO THIS TEST



* SIGNAL VARIATIONS

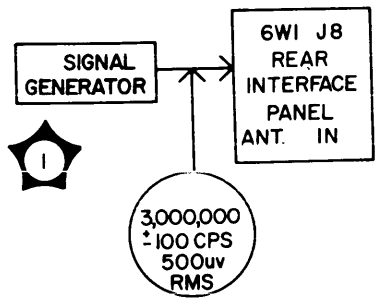
TEST	1S3 COUNTER MODE SW POS	① FX TEST INPUT (MC)	⑤ (MC) ⑥	⑪ MEGACYCLES DISPLAY
A	HIGH	12.34567	0.61728	12.3456
B	LOW	12.34567	6.17283	2.34567



POWER SUPPLY VOLTAGES

VOLTS	SOURCE	TO:
+24	1A2-3	1A3-14, 1A7-5
+24	2A1-3	2A3-1
-24	1A2-10	1A3-P

Figure 4-8. Servicing Block Diagram, AFC Section



CONTROL POSITIONS FOR TEST

MODULAR UNIT	CONTROL	POSITION
CV-2520/URC	POWER SWITCH	OFF
KY-661/URR	POWER SWITCH	OFF
O-1510/URR	POWER SWITCH	OFF
TD-914/URR	POWER SWITCH	OFF
TN-511/URR	POWER SWITCH	ON
	BAND SWITCH	2-4
	COUNTER MODE	REC
	RF GAIN	FULL CCW (AGC)
	FUNCTION	AFC
	SILENCER	OFF (DOWN)
	METER FUNCTION	AFC CARRIER
	FINE TUNE	MID POSITION
	INPUT ATTENUATOR	OUT (DOWN)
	TUNE	ADJUST FOR 03.0000 ON RCVR COUNTER

INPUT / OUTPUT CHECKS FOR FUNCTIONAL SECTION.

INPUT / OUTPUT CHECKS FOR MODULE UNIT.

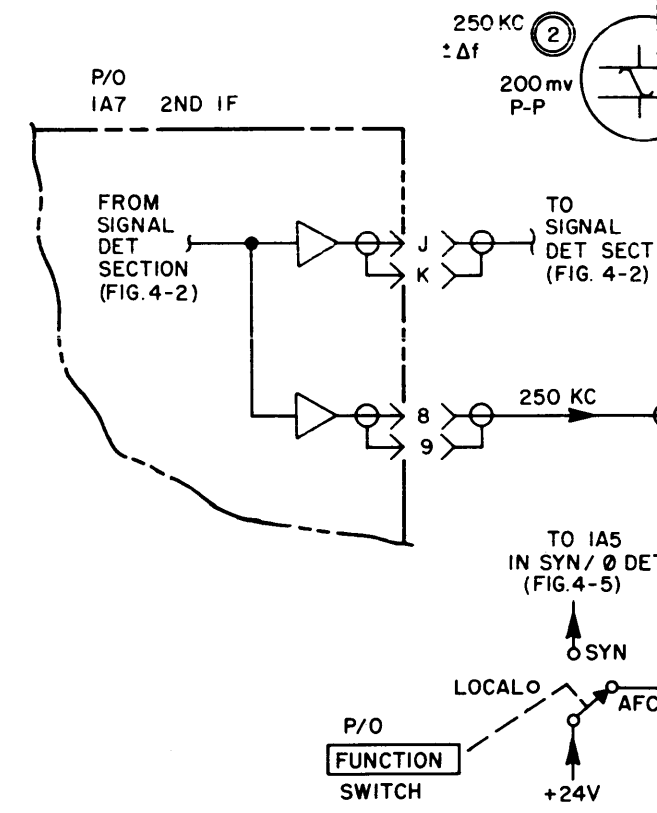
INPUT / OUTPUT CHECKS FOR SUBASSEMBLIES.

TEST A

WITH SIGNAL GENERATOR SET AT 3MC ± 100~ 500uv, AND WITH OTHER CONTROLS SET AS INDICATED, DEPRESS AFC TUNE SWITCH AND ADJUST TUNE / FINE TUNE CONTROLS FOR MAXIMUM INDICATION ON AFC CARRIER LEVEL METER AND CENTER SCALE ON PHASE DIFFERENCE METER. RELEASE AFC TUNE SWITCH. PROCEED WITH STEPS (2), (3), (4), (5), (6), (7)

TEST B (WITH SIGNAL GENERATOR CONNECTED AS FOR TEST A.)

1. MOVE RECEIVER FINE TUNE CONTROL FULLY CLOCKWISE.
2. DEPRESS AFC TUNE SWITCH AND ADJUST RECEIVER TUNE CONTROL CAREFULLY UNTIL RF/AFC LEVEL METER READS IN THE GREEN, PHASE DIFFERENCE METER READS CENTER SCALE AND SYNC LAMP IS LIGHTED. RELEASE AFC TUNE SWITCH, AFTER RECORDING RECEIVER COUNTER INDICATION.
3. CAREFULLY AND SLOWLY, IN SMALL INCREMENTS, MOVE THE RECEIVER FINE TUNE CONTROL COUNTERCLOCKWISE, ALLOWING THE PHASE DIFFERENCE METER TO STABILIZE AFTER EACH MOVEMENT, UNTIL THE SYNC LAMP GOES OUT.
4. DEPRESS AFC TUNE SWITCH AND RECORD RECEIVER COUNTER INDICATION. THE SECOND READING SHOULD BE AT LEAST ONE KILOCYCLE BELOW THE FIRST READING.
5. REPEAT STEPS 2, 3, AND 4 EXCEPT THAT THE RECEIVER FINE TUNE CONTROL SHOULD BE MOVED CLOCKWISE DURING THE MEASURMENTS. THE SECOND COUNTER READING SHOULD BE AT LEAST ONE KILOCYCLE HIGHER THAN THE FIRST READING.



INITIAL SWITCH POSITIONS		
UNIT	SWITCH	POSITION
CV-2520/URR	POWER	OFF
KY-661/URR	POWER	OFF
TD-914/URR	POWER	OFF
TN-511/URR	POWER	ON
O-1510/URR	POWER	ON

TEST OF SYNTHESIZED MODE

1. SET FREQUENCY SELECTORS ON O-1510/URR TO 09.0000
2. SET TUNER FUNCTION SWITCH TO SYN
3. SET TUNER BANDSWITCH TO 8-16 POSITION
4. SET COUNTER MODE SWITCH TO REC
5. SET TUNER FINE TUNE CONTROL TO MID POSITION
6. ADJUST TUNE CONTROL FOR 09.0000 ON RECEIVER COUNTER, AND CAUSE SYNC INDICATOR TO LIGHT
7. CONNECT DC VOLTMETER TO TP9, IA5
8. CAREFULLY MOVE TUNE CONTROL IN SMALL INCREMENTS TO CAUSE VOLTAGE READINGS AT TP9, IA5 AS INDICATED IN THE TABLE. THE METER POINTER SHOULD APPROXIMATE THE POSITIONS INDICATED
9. MOVE THE DC VOLTMETER TO PIN 3, IA5. WHEN THE SYSTEM IS IN SYNC, THE SYNC LAMP SHOULD BE LIT AND THE VOLTAGE READING SHOULD BE +24 VOLTS WHEN THE SYSTEM IS OUT OF SYNC, THE SYNC LAMP SHOULD BE OUT AND THE VOLTAGE READING SHOULD BE 0 VOLTS.

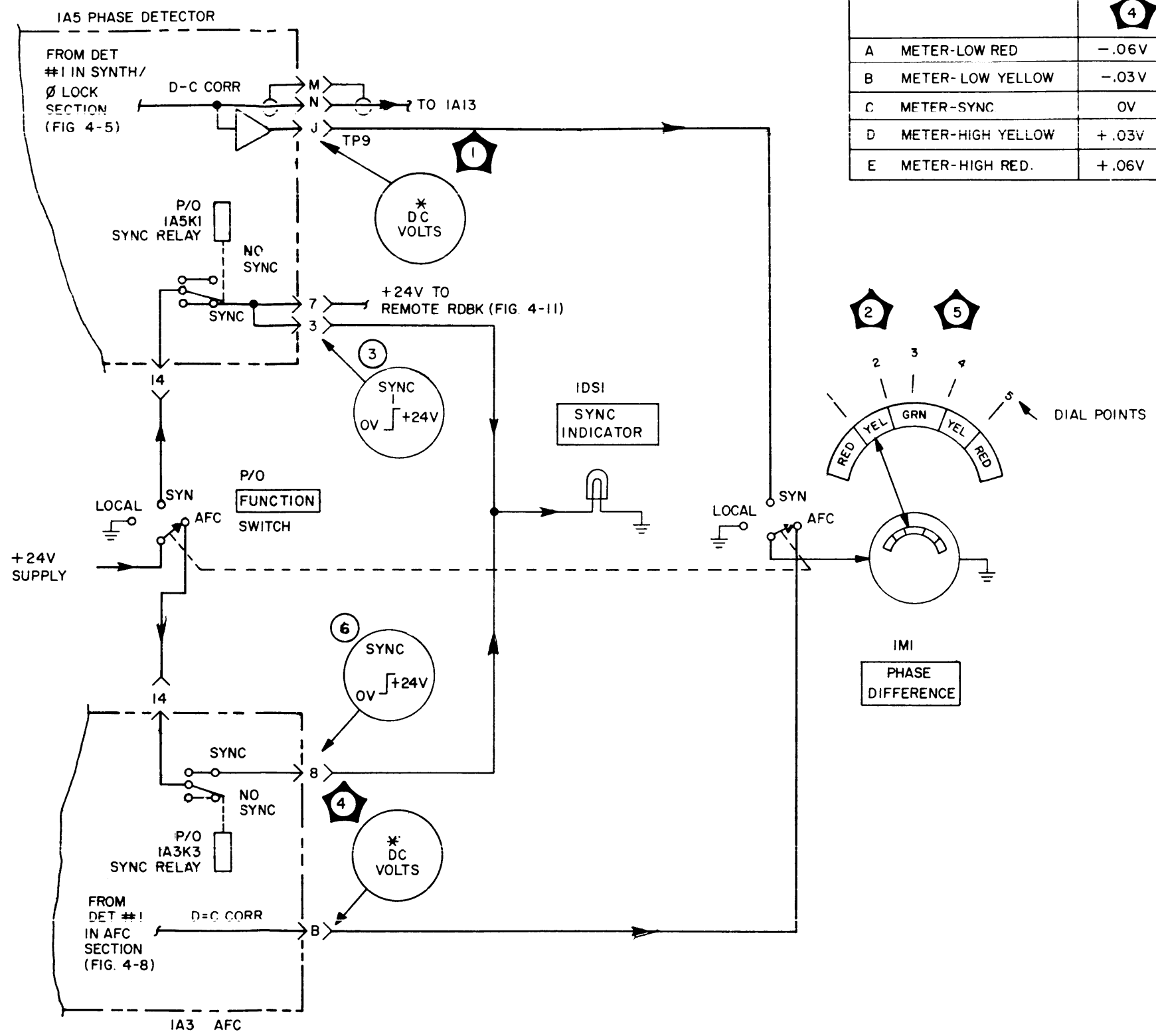
TEST OF AFC MODE

SIGNAL GENERATOR → 6WJ8 ANTENNA INPUT — SET AT 09.0000 MC ± 200 CPS AT 1mV, UNMODULATED

1. SET TUNER FUNCTION SWITCH TO AFC
2. SET METER FUNCTION SWITCH ON TUNER TO AFC
3. SET INPUT ATTENUATOR SWITCH DOWN (OUT)
4. CONNECT SIGNAL GENERATOR TO ANTENNA INPUT AT 9MC, +OR − 200 CPS, AT 1mV, UNMODULATED
5. DEPRESS AFC TUNE SWITCH AND ADJUST FINE TUNE AND TUNE CONTROLS FOR MAXIMUM INDICATION ON AFC LEVEL METER AND CENTER SCALE INDICATION ON THE PHASE DIFFERENCE METER. RELEASE THE AFC TUNE SWITCH
6. CONNECT DC VOLTMETER TO PIN B, IA3
7. CAREFULLY MOVE THE TUNE CONTROL IN SMALL INCREMENTS TO CAUSE VOLTAGE READINGS AT PIN B, IA3, AS INDICATED IN THE TABLE. THE METER POINTER SHOULD APPROXIMATE THE POSITIONS INDICATED
8. MOVE THE DC VOLTMETER TO PIN 8, IA3
9. WHEN THE SYSTEM IS IN SYNC, THE SYNC LAMP SHOULD BE LIT AND THE VOLTAGE READING SHOULD BE +24 VOLTS. WHEN THE SYSTEM IS OUT OF SYNC, THE SYNC LAMP SHOULD BE OUT AND THE VOLTAGE READING SHOULD BE O VOLTS.

NOTES:

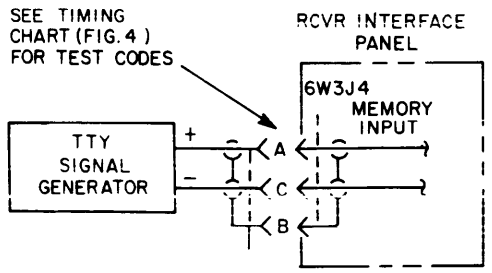
1. ⬠ INPUT/OUTPUT CHECK FOR FUNCTIONAL SECTION
   ○ INPUT/OUTPUT CHECK FOR SUBASSEMBLY



* VOLTAGE VARIATIONS

TEST	① ④	② ⑤
A METER-LOW RED	−.06V	DIAL PT 1
B METER-LOW YELLOW	−.03V	DIAL PT 2
C METER-SYNC	0V	DIAL PT 3
D METER-HIGH YELLOW	+.03V	DIAL PT 4
E METER-HIGH RED.	+.06V	DIAL PT 5

Figure 4-9. Servicing Block Diagram, Sync Indicator Section



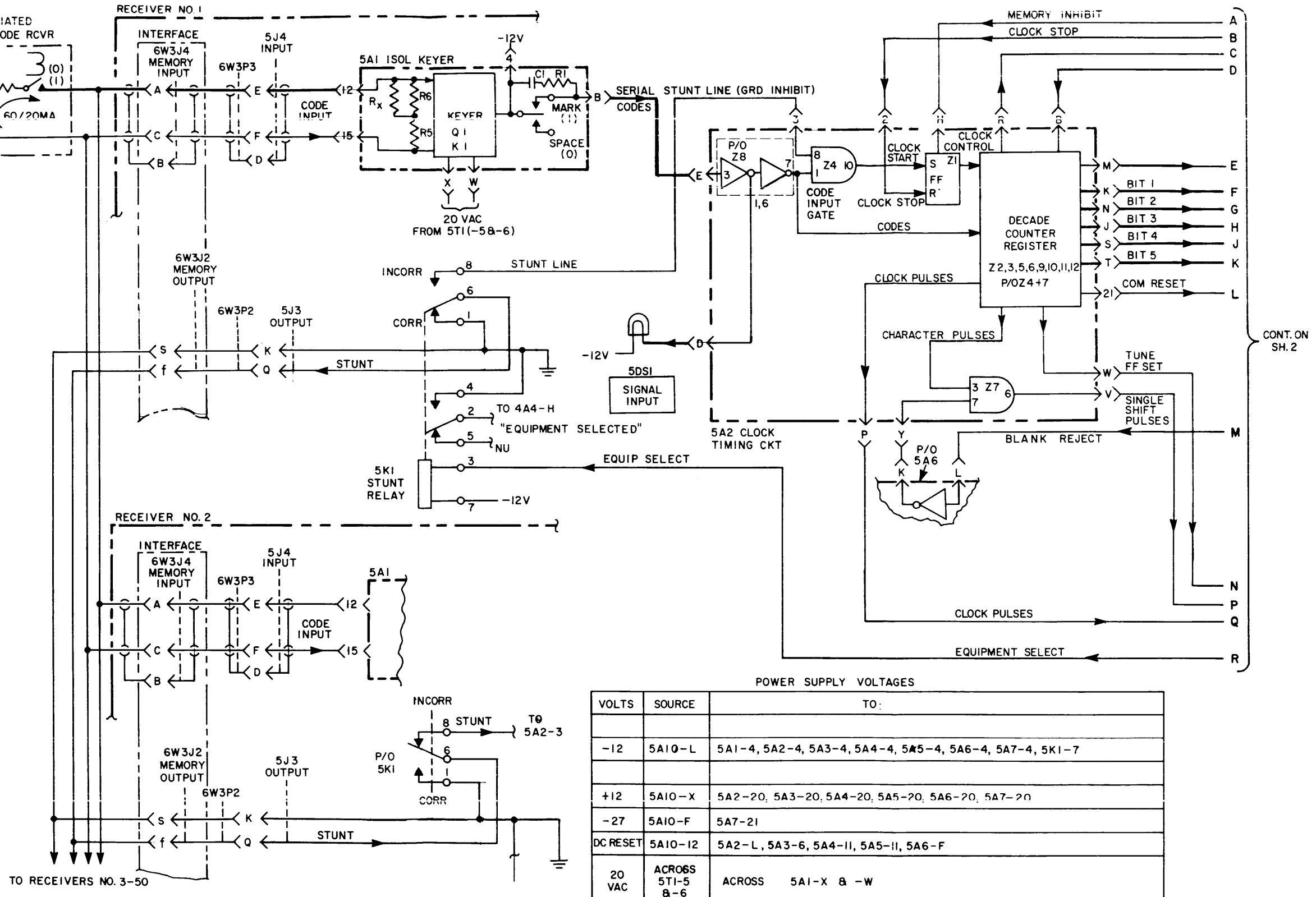
TEST SETUP-AUTOMATIC CONTROL

CONTROL POSITION FOR TEST

MODULAR UNIT	CONTROL	POSITION
TN-511/URR	RF GAIN KNOB	AGC
	POWER SWITCH	ON
	COUNTER MODE SWITCH	REC
	BAND SWITCH	AUTO
TD-914/URR	SYM BFO	0
O-1510/URR	POWER SWITCH	ON
KY-661/URR	POWER SWITCHI	ON
CV-2520(V)/URC	POWER SWITCH	ON

NOTES:

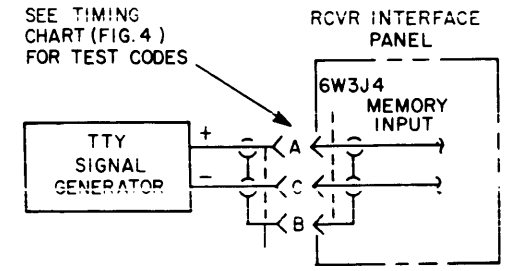
1. SEE TIMING CHART (FIG.4-) FOR ALL TEST POINT READINGS.
2. A DUAL TRACE SCOPE SHOULD BE USED TO OBTAIN TEST POINT READINGS. CHANNEL "A" AND TRIGGER OF SCOPE SHOULD BE CONNECTED TO 5A2-P.
3. NU= NOT USED IN CV-2520(V)URC
4. "S" DENOTES A SET PULSE, "R" DENOTES A RESET PULSE, ie: 2R=2 BIT RESET, 5S=5 BIT SET
5. ——— DENOTES CODE PATH



POWER SUPPLY VOLTAGES

VOLTS	SOURCE	TO:
-12	5A10-L	5A1-4, 5A2-4, 5A3-4, 5A4-4, 5A5-4, 5A6-4, 5A7-4, 5K1-7
+12	5A10-X	5A2-20, 5A3-20, 5A4-20, 5A5-20, 5A6-20, 5A7-20
-27	5A10-F	5A7-21
DC RESET	5A10-12	5A2-L, 5A3-6, 5A4-11, 5A5-11, 5A6-F
20 VAC	ACROSS 5T1-5 & -6	ACROSS 5A1-X & -W

Figure 4-10. Servicing Block Diagram, Remote Tuning Section (Sheet 1 of 6)



TEST SETUP-AUTOMATIC CONTROL

CONTROL POSITION FOR TEST

MODULAR UNIT	CONTROL	POSITION
TN-511/URR	RF GAIN KNOB	AGC
	POWER SWITCH	ON
	COUNTER MODE SWITCH	REC
	BAND SWITCH	AUTO
TD-914/URR	SYM BFO	0
O-1510/URR	POWER SWITCH	ON
KY-661/URR	POWER SWITCHI	ON
CV-2520(V)/URC	POWER SWITCH	ON

NOTES:

1. SEE TIMING CHART (FIG.4-) FOR ALL TEST POINT READINGS.
2. A DUAL TRACE SCOPE SHOULD BE USED TO OBTAIN TEST POINT READINGS. CHANNEL "A" AND TRIGGER OF SCOPE SHOULD BE CONNECTED TO 5A2-P.
3. NU= NOT USED IN CV-2520(V)URC
4. "S" DENOTES A SET PULSE, "R" DENOTES A RESET PULSE, ie: 2R=2 BIT RESET, 5S=5 BIT SET
5. ——— DENOTES CODE PATH

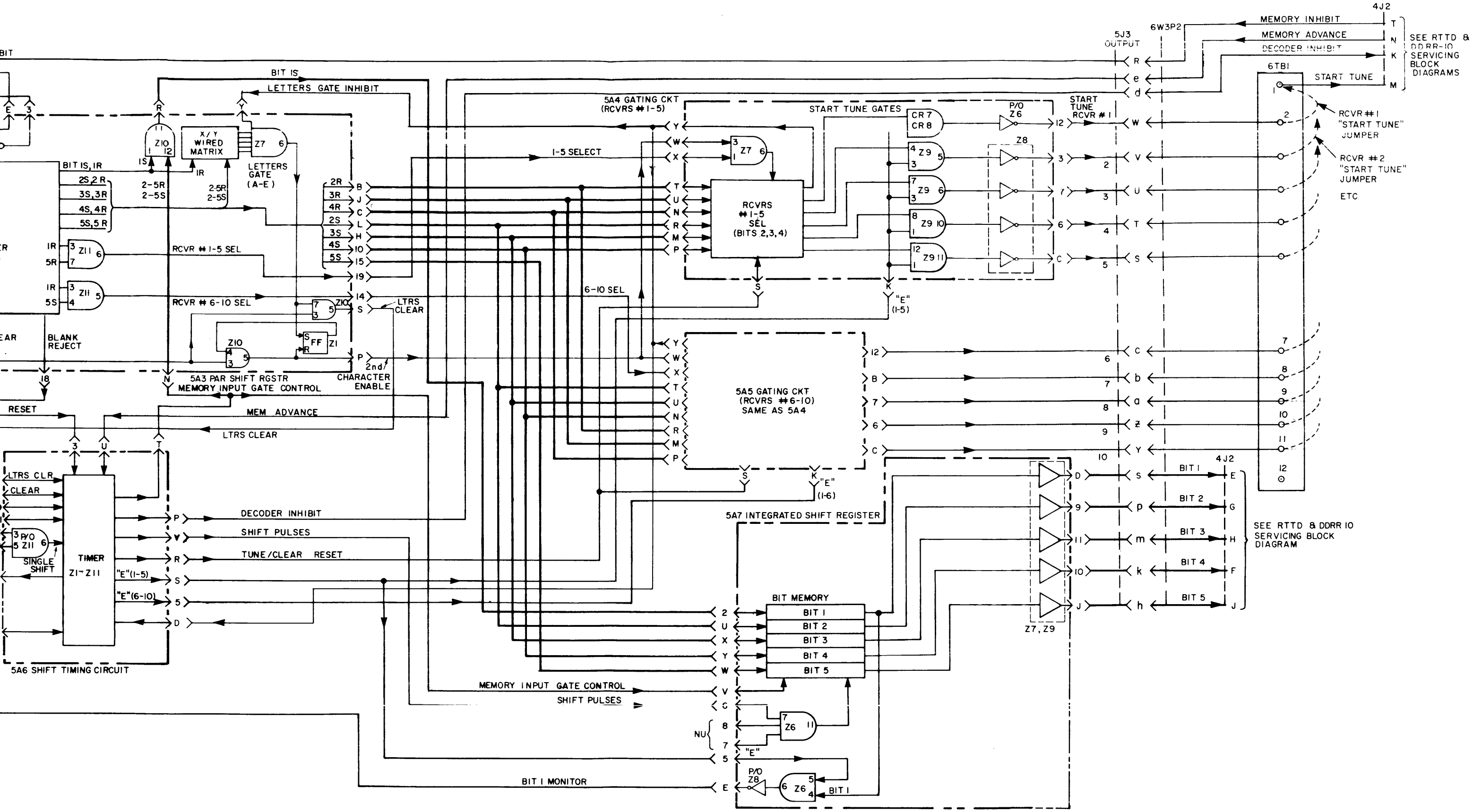
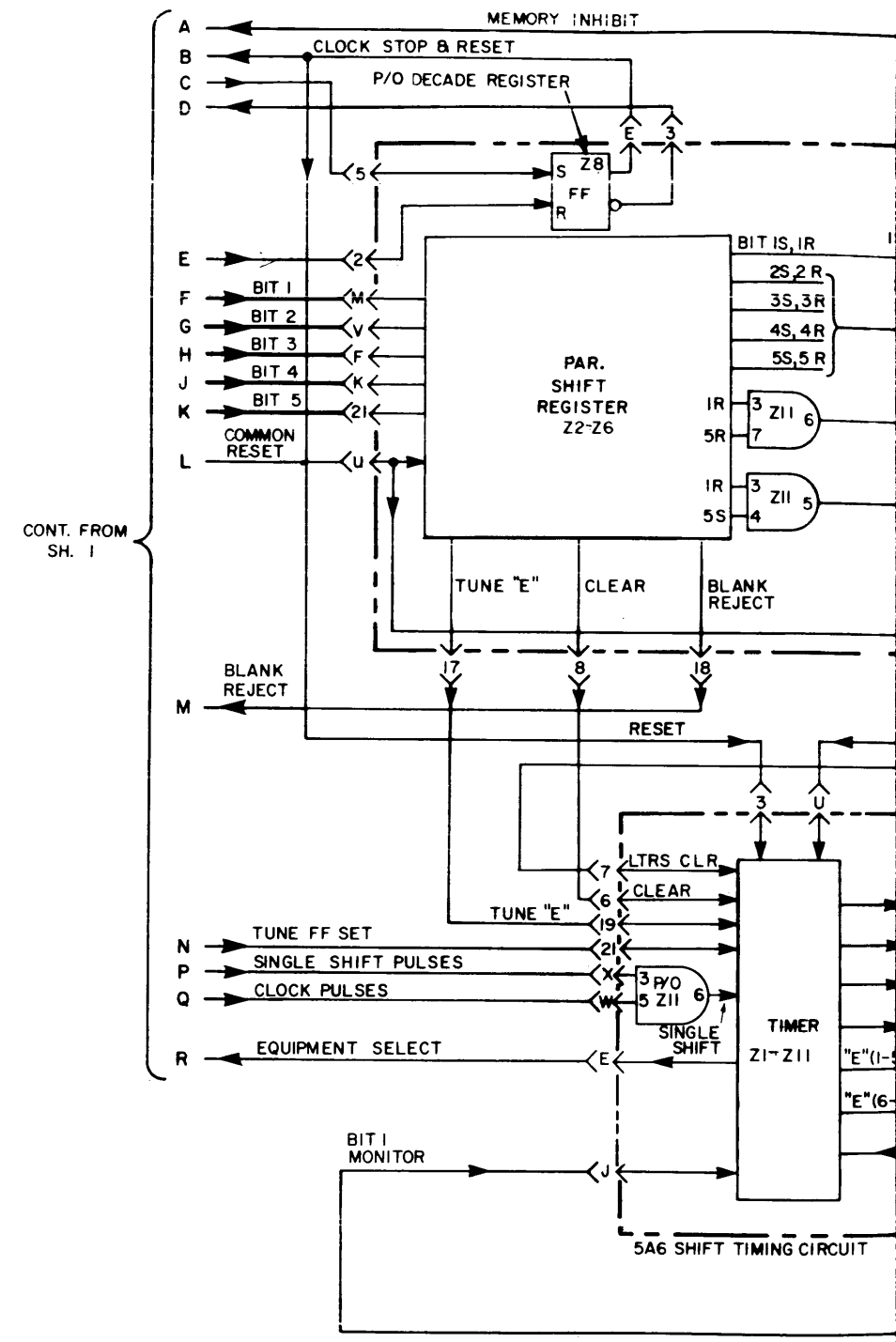


Figure 4-10. Servicing Block Diagram, Remote Tuning Section (Sheet 2 of 6)


MEMORY INHIBIT
CLOCK STOP & RESET
P/O DECADE REGISTER
A
B
C
D
E
3
5
S
Z8
FF
R
BIT IS, IR
2S,2R
3S,3R
4S,4R
5S,5R
E
F
G
H
J
K
L
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
COMMON RESET
2
M
V
F
K
21
U
PAR. SHIFT REGISTER Z2-Z6
IR
5R
3
Z11
6
7
IR
5S
3
Z11
5
4
CONT. FROM SH. 1
TUNE "E"
CLEAR
BLANK REJECT
17
8
18
BLANK REJECT
M
RESET
3
U
7
LTRS CLR
6
CLEAR
TUNE "E"
19
N
TUNE FF SET
21
P
SINGLE SHIFT PULSES
X
Q
CLOCK PULSES
W
3
P/O
5
Z11
6
SINGLE SHIFT
TIMER
Z1-Z11
R
EQUIPMENT SELECT
E
"E"(1-5
"E"(6-
BIT 1 MONITOR
J
5A6 SHIFT TIMING CIRCUIT

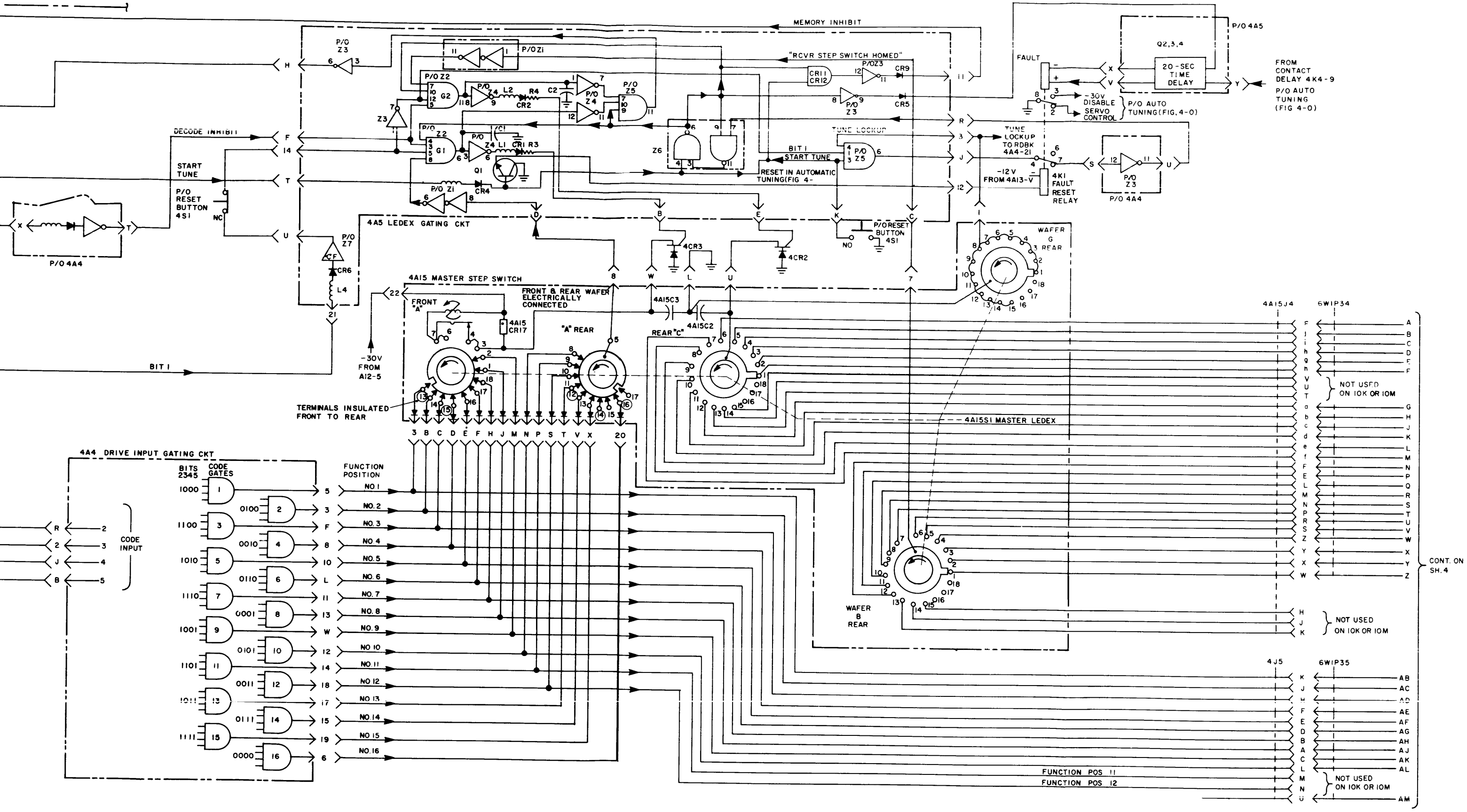
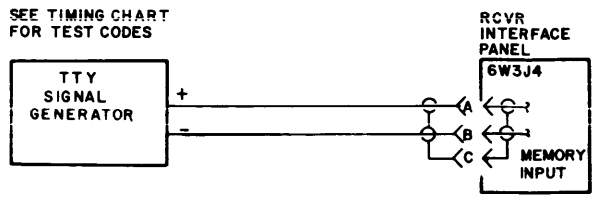


Figure 4-10. Servicing Block Diagram, Remote Tuning Section (Sheet 3 of 6)



TEST SET-UP AUTOMATIC CONTROL

CONTROL POSITION FOR TEST

MODULAR UNIT	CONTROL	POSITION
TN-511/URR	RF GAIN KNOB	AGC
	POWER SWITCH	ON
	COUNTER MODE SWITCH	REC
	BAND SWITCH	AUTO
TD-914/URR	POWER SWITCH	ON
O-1510/URR	POWER SWITCH	ON
KY-661/URR	POWER SWITCH	ON
CV-2520(V) URC	POWER SWITCH	ON

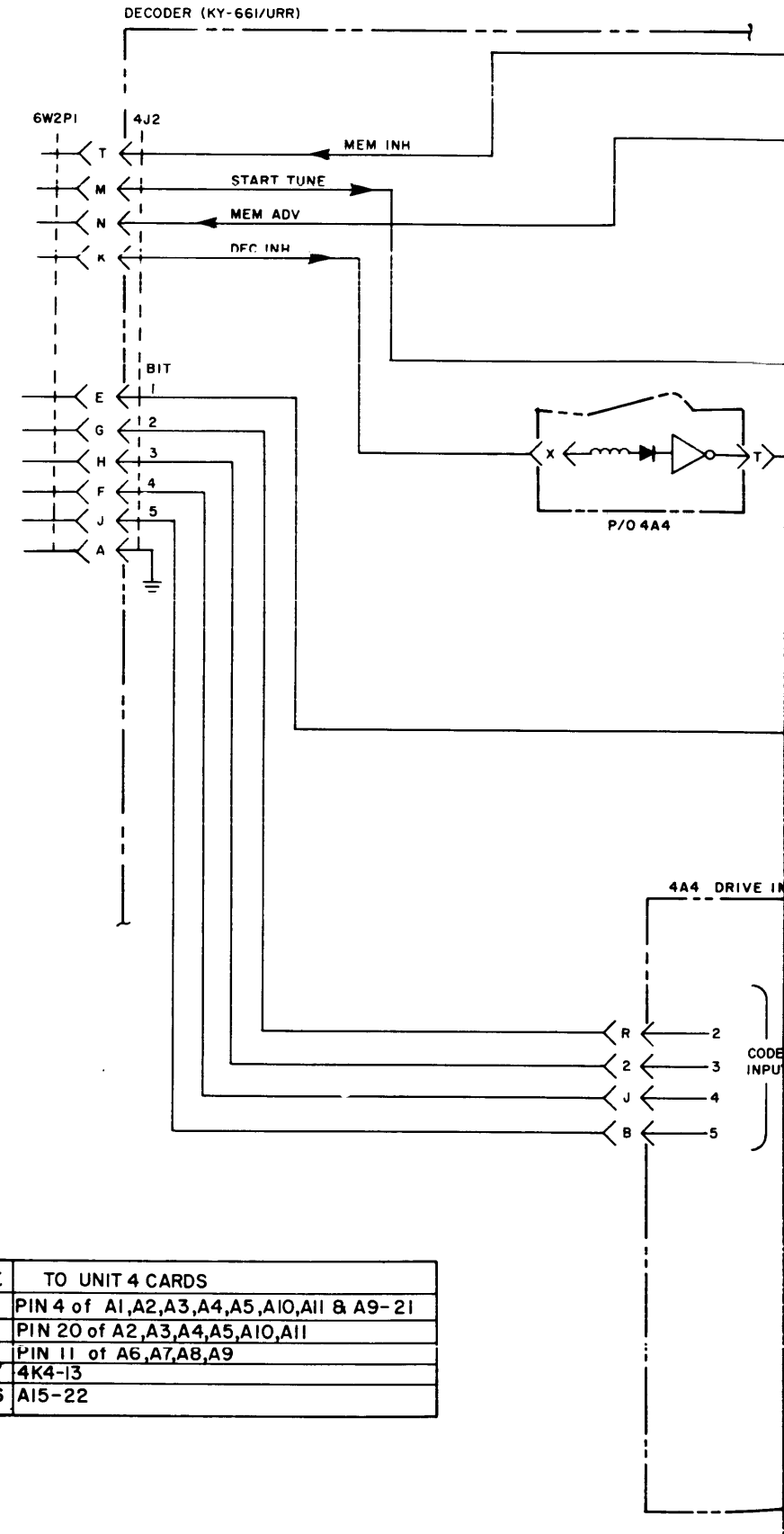
NOTES

1. SEE TIMING CHARTS(FIG 4-) TEST POINT READINGS

2. N U = NOT USED IN CV-2520(V)URC
   ——— CODE PATH

3. USE START TUNE PULSE TO EXTERNALLY SYNC SCOPE (+) TO OBSERVE WAVEFORMS ON TIMING CHART FOR THIS BLOCK

4. A DUAL TRACE SCOPE SHOULD BE USED TO COMPARE ONE WAVEFORM WITH ANOTHER



VOLTS	SOURCE	TO UNIT 4 CARDS
-12	4A13-W	PIN 4 of A1,A2,A3,A4,A5,A10,A11 & A9-21
+12	4A13-H	PIN 20 of A2,A3,A4,A5,A10,A11
+5	4A14-B	PIN 11 of A6,A7,A8,A9
+28	4A14-Y	4K4-13
-30	4A12-5,6	A15-22

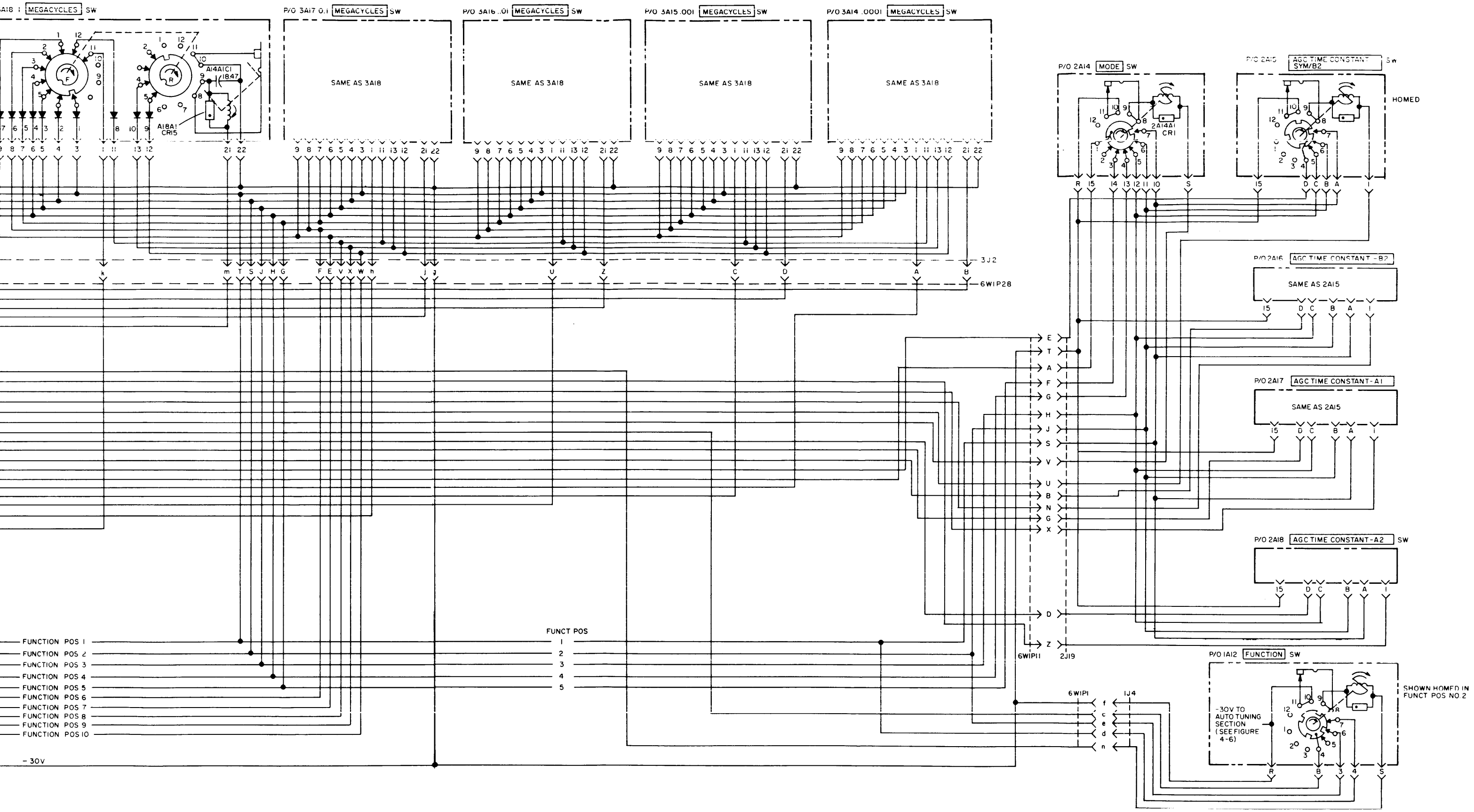
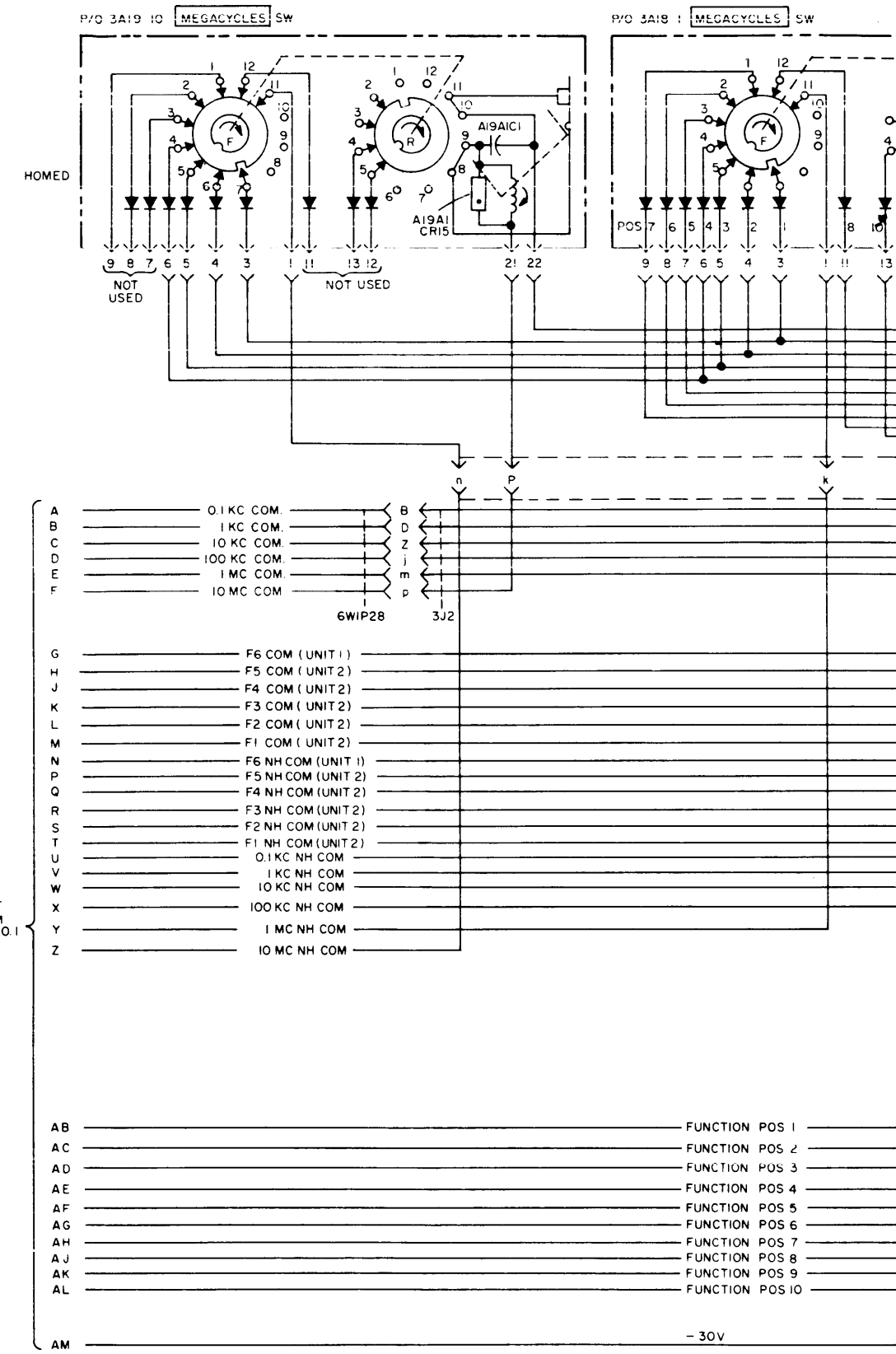
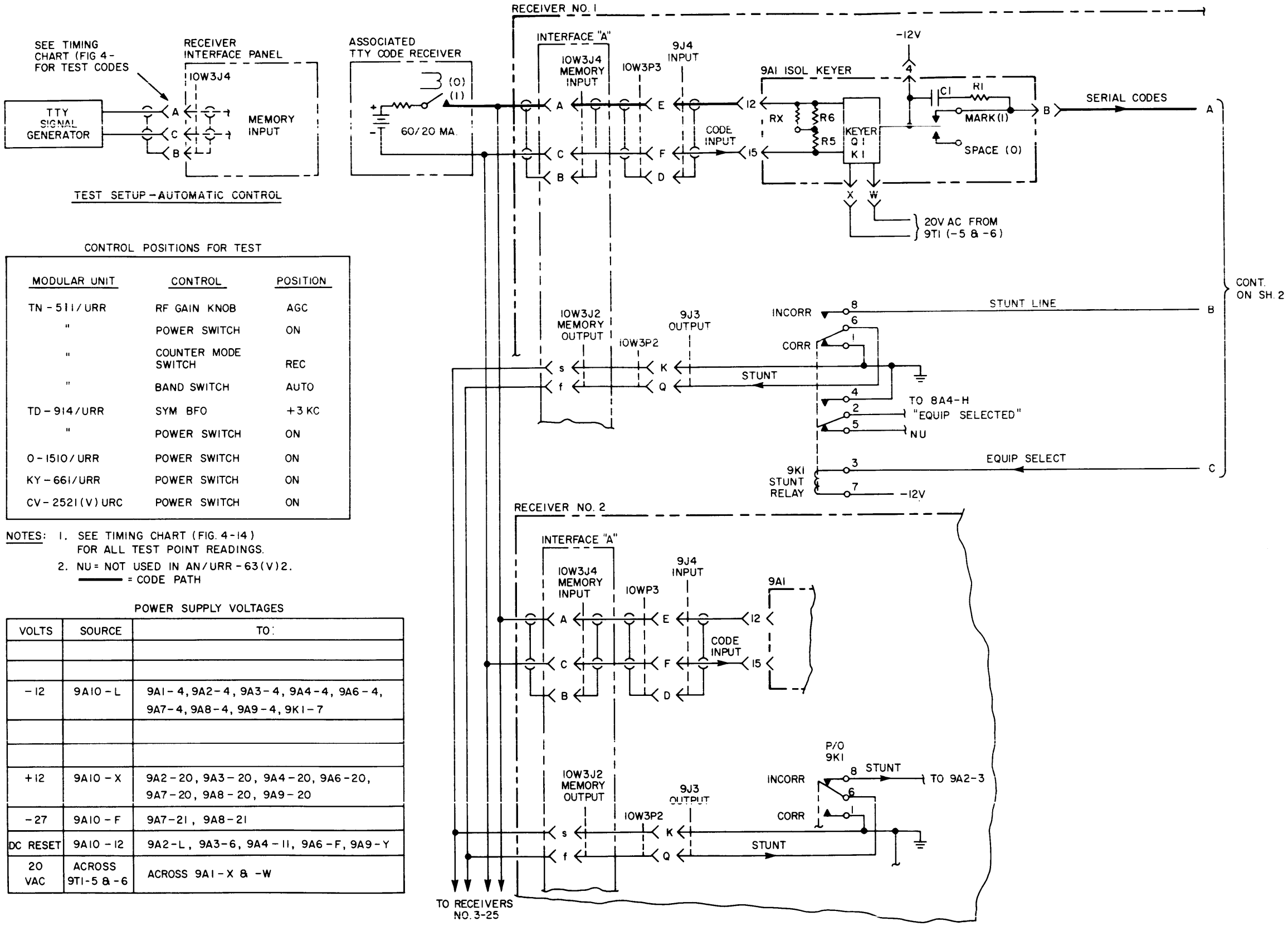


Figure 4-10. Servicing Block Diagram, Remote Tuning Section (Sheet 4 of 6)


P/O 3A19 10 MEGACYCLES SW
P/O 3A18 1 MEGACYCLES SW
HOMED
A19A1C1
A19A1 CR15
NOT USED
NOT USED
POS
0.1 KC COM.
1 KC COM.
10 KC COM.
100 KC COM.
1 MC COM.
10 MC COM
6WIP28
3J2
F6 COM (UNIT 1)
F5 COM (UNIT 2)
F4 COM (UNIT 2)
F3 COM (UNIT 2)
F2 COM (UNIT 2)
F1 COM (UNIT 2)
F6 NH COM (UNIT 1)
F5 NH COM (UNIT 2)
F4 NH COM (UNIT 2)
F3 NH COM (UNIT 2)
F2 NH COM (UNIT 2)
F1 NH COM (UNIT 2)
0.1 KC NH COM
1 KC NH COM
10 KC NH COM
100 KC NH COM
1 MC NH COM
10 MC NH COM
* CONT FROM SH. NO. 1
FUNCTION POS 1
FUNCTION POS 2
FUNCTION POS 3
FUNCTION POS 4
FUNCTION POS 5
FUNCTION POS 6
FUNCTION POS 7
FUNCTION POS 8
FUNCTION POS 9
FUNCTION POS 10
- 30V



CONTROL POSITIONS FOR TEST

MODULAR UNIT	CONTROL	POSITION
TN-511/URR	RF GAIN KNOB	AGC
"	POWER SWITCH	ON
"	COUNTER MODE SWITCH	REC
"	BAND SWITCH	AUTO
TD-914/URR	SYM BFO	+3 KC
"	POWER SWITCH	ON
O-1510/URR	POWER SWITCH	ON
KY-661/URR	POWER SWITCH	ON
CV-2521(V)URC	POWER SWITCH	ON

NOTES: 1. SEE TIMING CHART (FIG. 4-14) FOR ALL TEST POINT READINGS.
2. NU = NOT USED IN AN/URR-63(V)2.
——— = CODE PATH

POWER SUPPLY VOLTAGES

VOLTS	SOURCE	TO:
-12	9A10-L	9A1-4, 9A2-4, 9A3-4, 9A4-4, 9A6-4, 9A7-4, 9A8-4, 9A9-4, 9K1-7
+12	9A10-X	9A2-20, 9A3-20, 9A4-20, 9A6-20, 9A7-20, 9A8-20, 9A9-20
-27	9A10-F	9A7-21, 9A8-21
DC RESET	9A10-12	9A2-L, 9A3-6, 9A4-11, 9A6-F, 9A9-Y
20 VAC	ACROSS 9TI-5 & -6	ACROSS 9A1-X & -W

Figure 4-10. Servicing Block Diagram, Remote Tuning Section (Sheet 5 of 6)

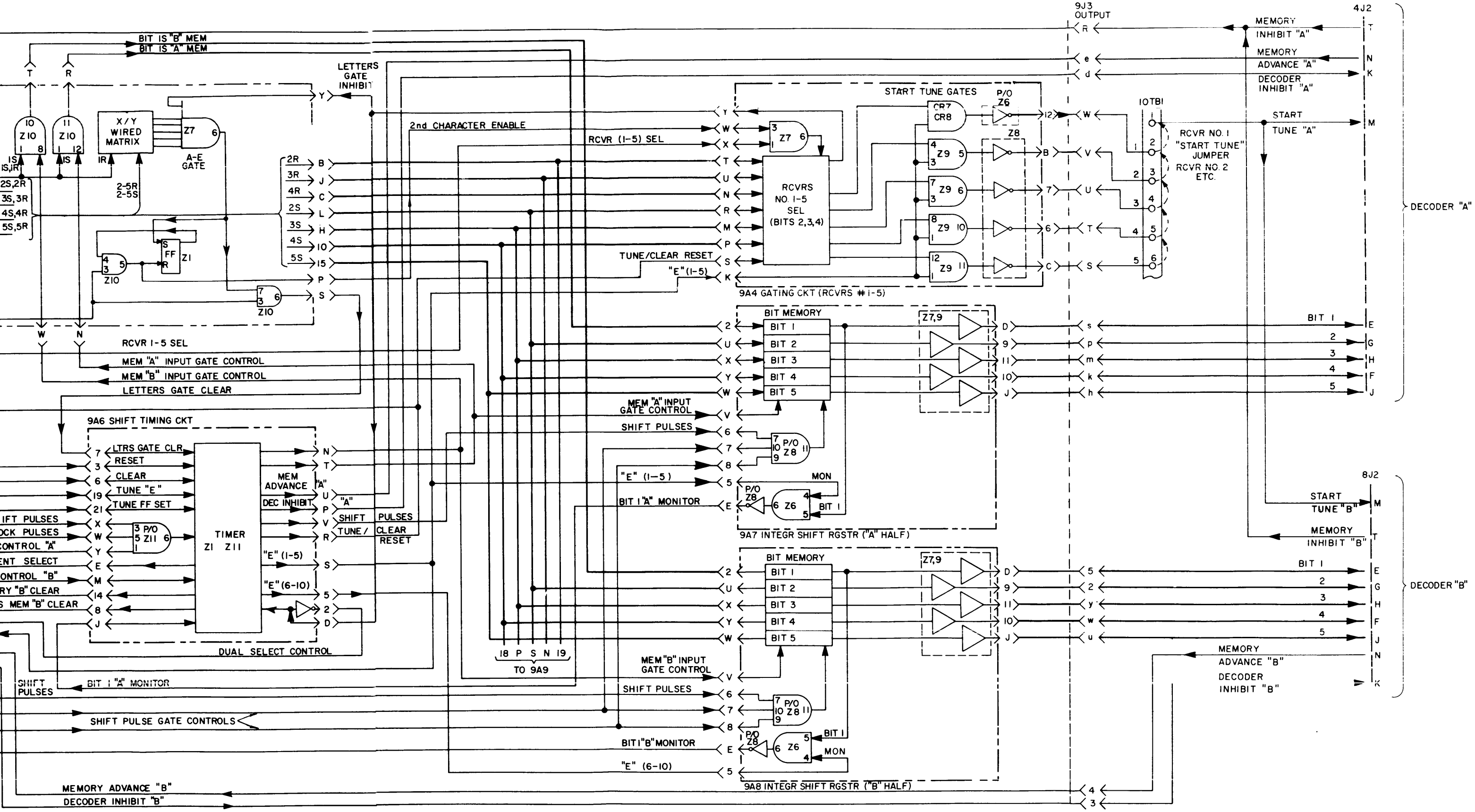
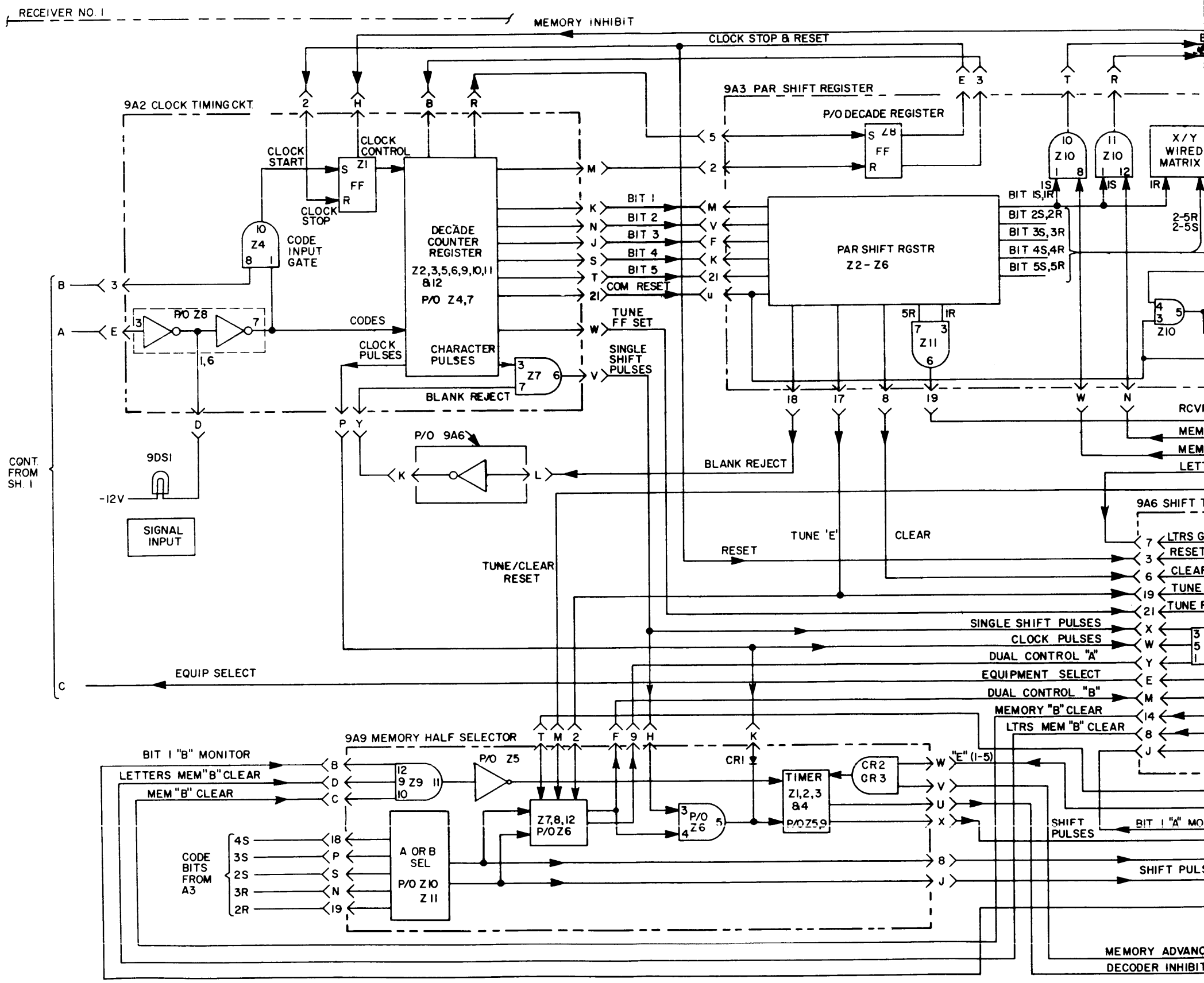
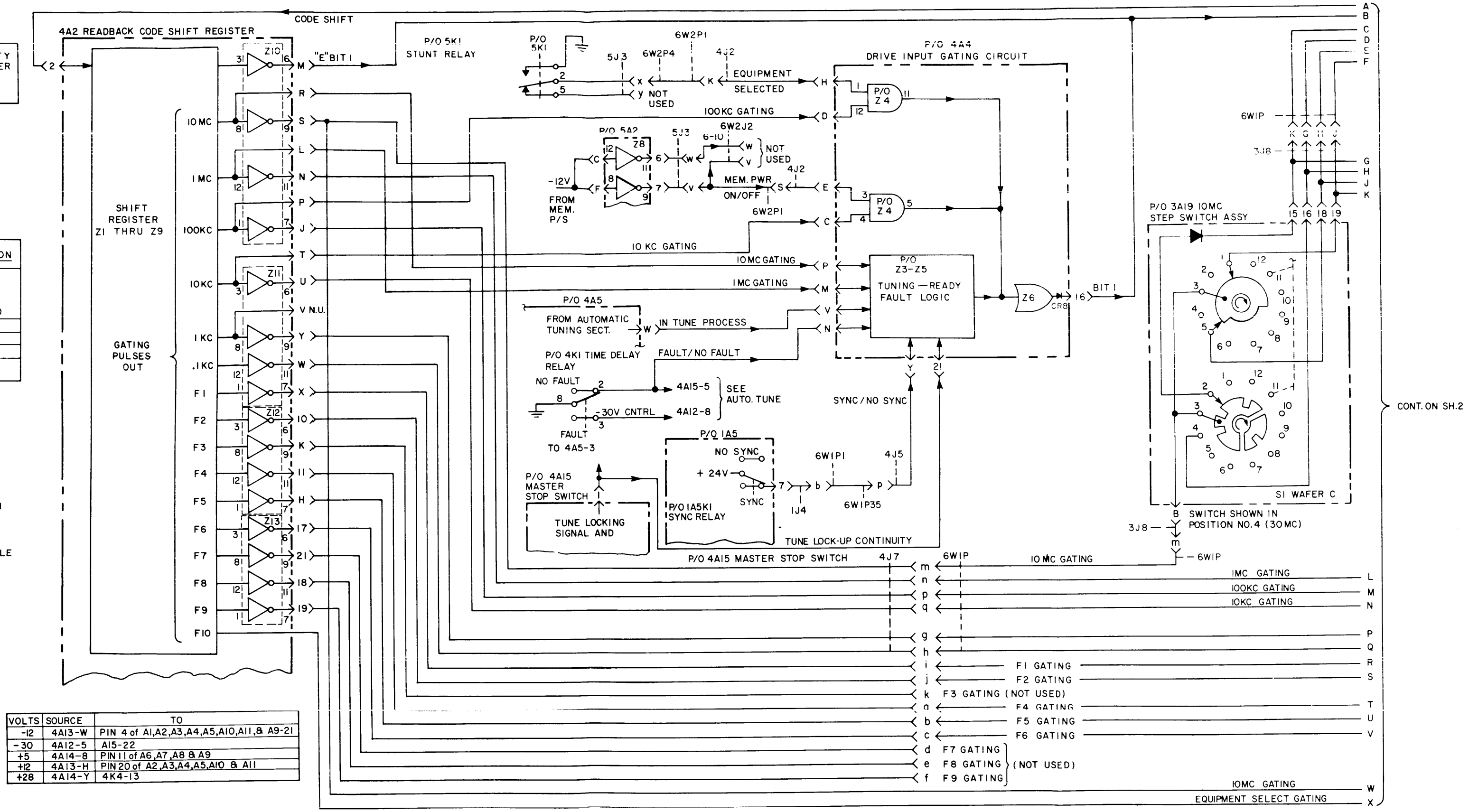


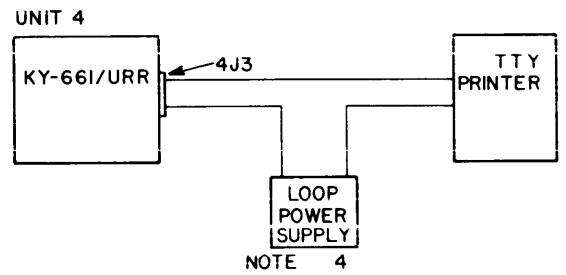
Figure 4-10. Servicing Block Diagram, Remote Tuning Section (Sheet 6 of 6)


RECEIVER NO. 1
MEMORY INHIBIT
CLOCK STOP & RESET
9A2 CLOCK TIMING CKT
9A3 PAR SHIFT REGISTER
P/O DECADE REGISTER
CLOCK START
CLOCK CONTROL
CLOCK STOP
Z1 FF
CODE INPUT GATE
Z4
DECADE COUNTER REGISTER
Z2,3,5,6,9,10,11 &12
P/O Z4,7
CHARACTER PULSES
CODES
CLOCK PULSES
TUNE FF SET
SINGLE SHIFT PULSES
BLANK REJECT
P/O Z8
1,6
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
COM RESET
PAR SHIFT RGSTR Z2 - Z6
BIT 1S,1R
BIT 2S,2R
BIT 3S,3R
BIT 4S,4R
BIT 5S,5R
X/Y WIRED MATRIX
2-5R
2-5S
Z10
Z11
5R
1R
P/O 9A6
9DS1
-12V
SIGNAL INPUT
CONT. FROM SH. 1
EQUIP SELECT
TUNE/CLEAR RESET
RESET
TUNE 'E'
CLEAR
BLANK REJECT
9A6 SHIFT
LTRS G
RESET
CLEAR
TUNE
TUNE F
SINGLE SHIFT PULSES
CLOCK PULSES
DUAL CONTROL "A"
EQUIPMENT SELECT
DUAL CONTROL "B"
MEMORY "B" CLEAR
LTRS MEM "B" CLEAR
RCVI
MEM
MEM
LET
9A9 MEMORY HALF SELECTOR
BIT 1 "B" MONITOR
LETTERS MEM "B" CLEAR
MEM "B" CLEAR
CODE BITS FROM A3
4S
3S
2S
3R
2R
A OR B SEL
P/O Z10 Z11
P/O Z5
Z7,8,12 P/OZ6
P/O Z6
CR1
CR2 CR3
TIMER Z1,2,3 &4
P/OZ5,9
"E" (1-5)
SHIFT PULSES
BIT 1 "A" MO
SHIFT PULS
MEMORY ADVANC
DECODER INHIBIT



VOLTS	SOURCE	TO
-12	4A13-W	PIN 4 of A1,A2,A3,A4,A5,A10,A11,& A9-21
-30	4A12-5	A15-22
+5	4A14-8	PIN 11 of A6,A7,A8 & A9
+12	4A13-H	PIN 20 of A2,A3,A4,A5,A10 & A11
+28	4A14-Y	4K4-13

Figure 4-11. Servicing Block Diagram, Remote Readback Section (Sheet 1 of 2)

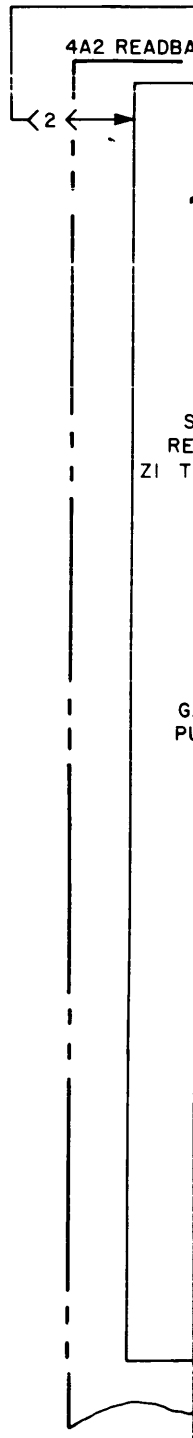


CONTROL POSITION FOR TEST

MODULAR UNIT	CONTROL	POSITION
TN-511/URR	RF GAIN KNOB	AGC
	POWER SWITCH	ON
	COUNTER MODE SWITCH	REC
	BAND SWITCH	AUTO
TD-914/URR	POWER SWITCH	ON
O-1510/URR	POWER SWITCH	ON
KY-661/URR	POWER SWITCH	ON
CV-2520(V) URC	POWER SWITCH	ON

NOTES

1. SEE TIMING CHARTS FOR ALL TEST POINT WAVEFORMS AND SWITCH POSITIONS AND OPERATING CONDITIONS.
2. NU = NOT USED IN CV-2520(V)URC
3. A DUAL TRACE SCOPE MUST BE USED TO COMPARE THE TIME OF ONE WAVEFORM WITH ANOTHER.
4. LOOP POWER SUPPLY WILL HAVE TO BE COMPATIBLE WITH TTY PRINTER AND CONNECTIONS AT 4J3 MADE TO BE COMPATIBLE WITH TTY MACHINE.



VOLTS	SOURCE	
-12	4A13-W	PIN
-30	4A12-5	A15-
+5	4A14-8	PIN 1
+12	4A13-H	PIN 2
+28	4A14-Y	4K4

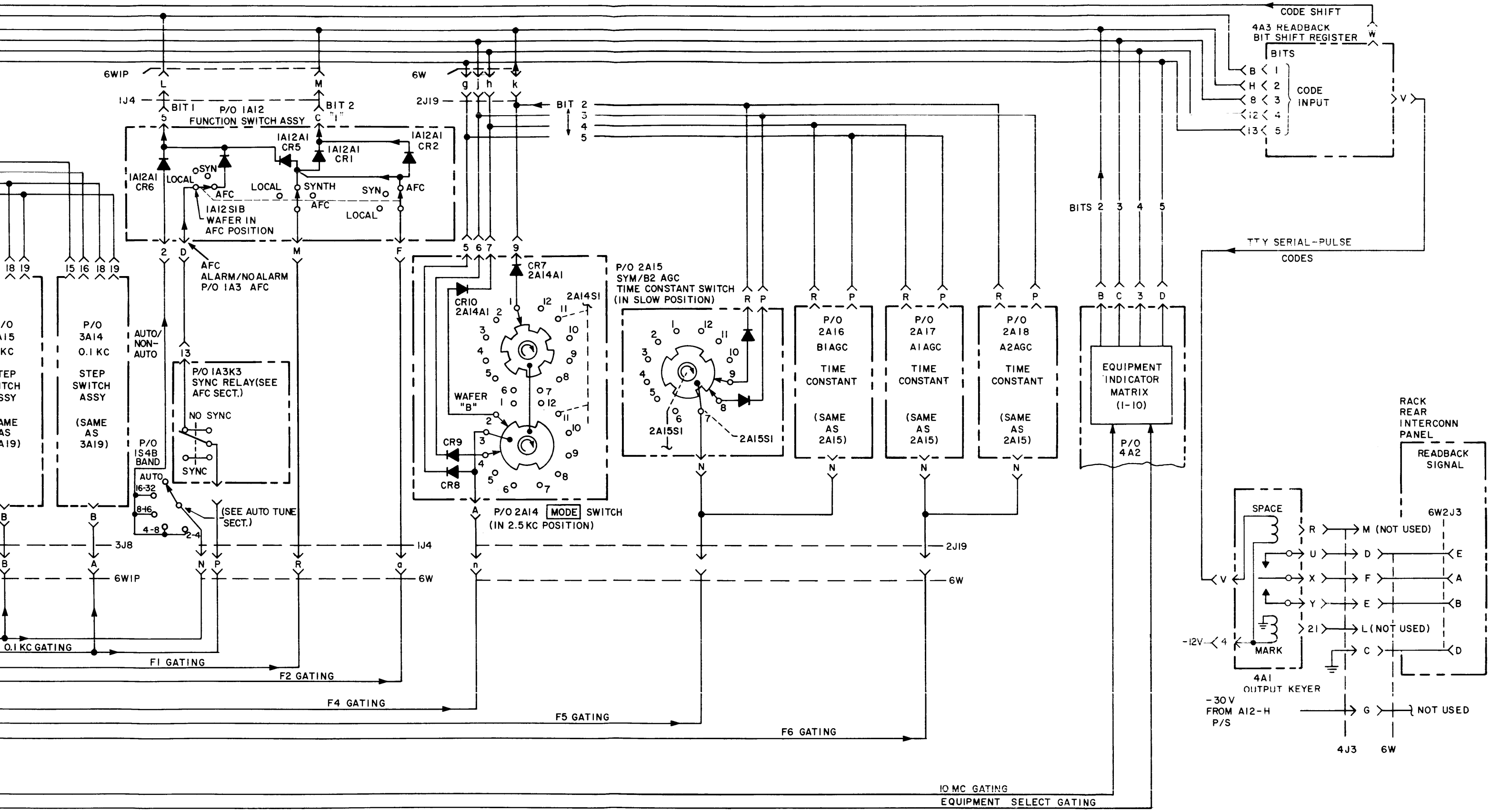


Figure 4-11. Servicing Block Diagram, Remote Readback Section (Sheet 2 of 2)

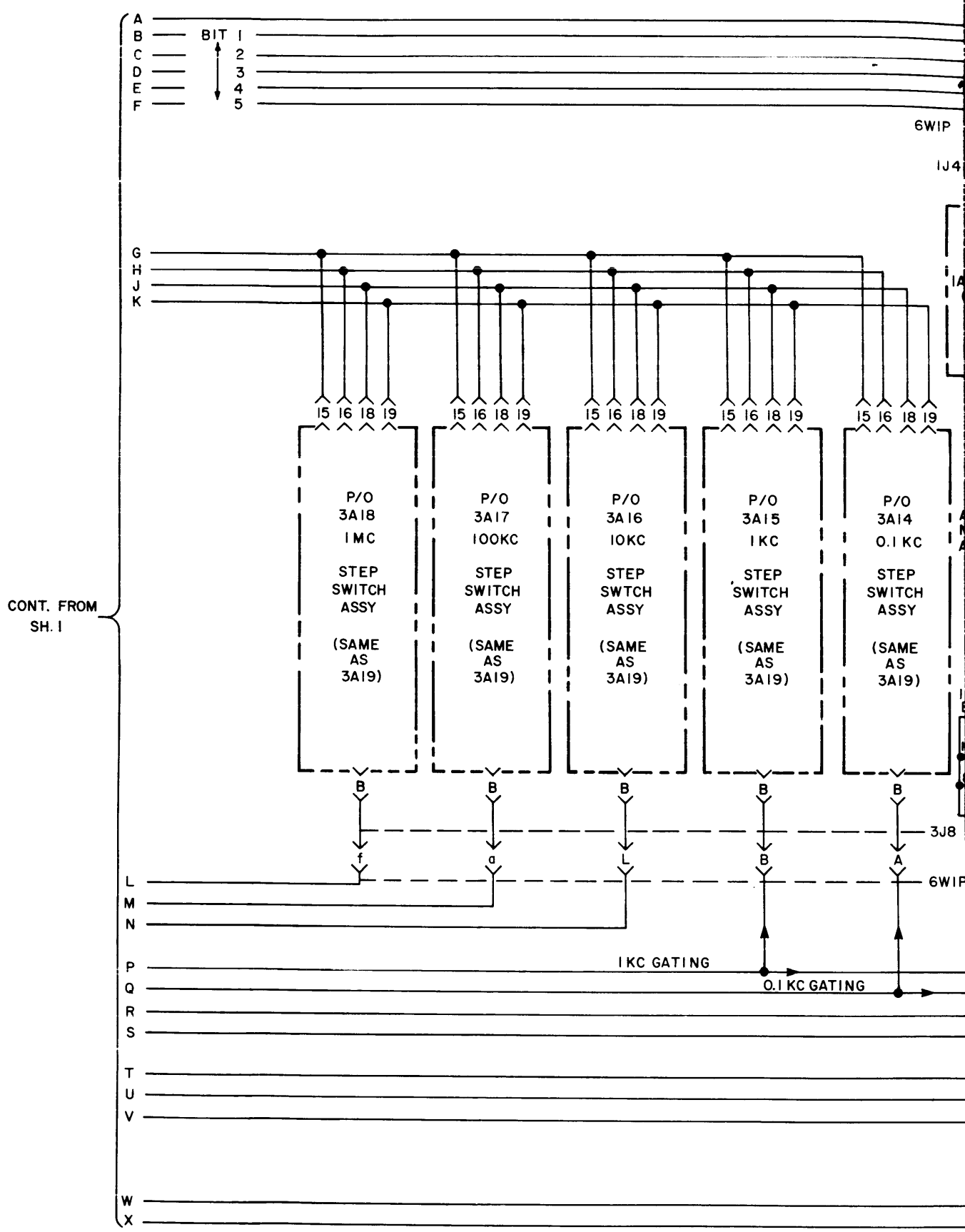
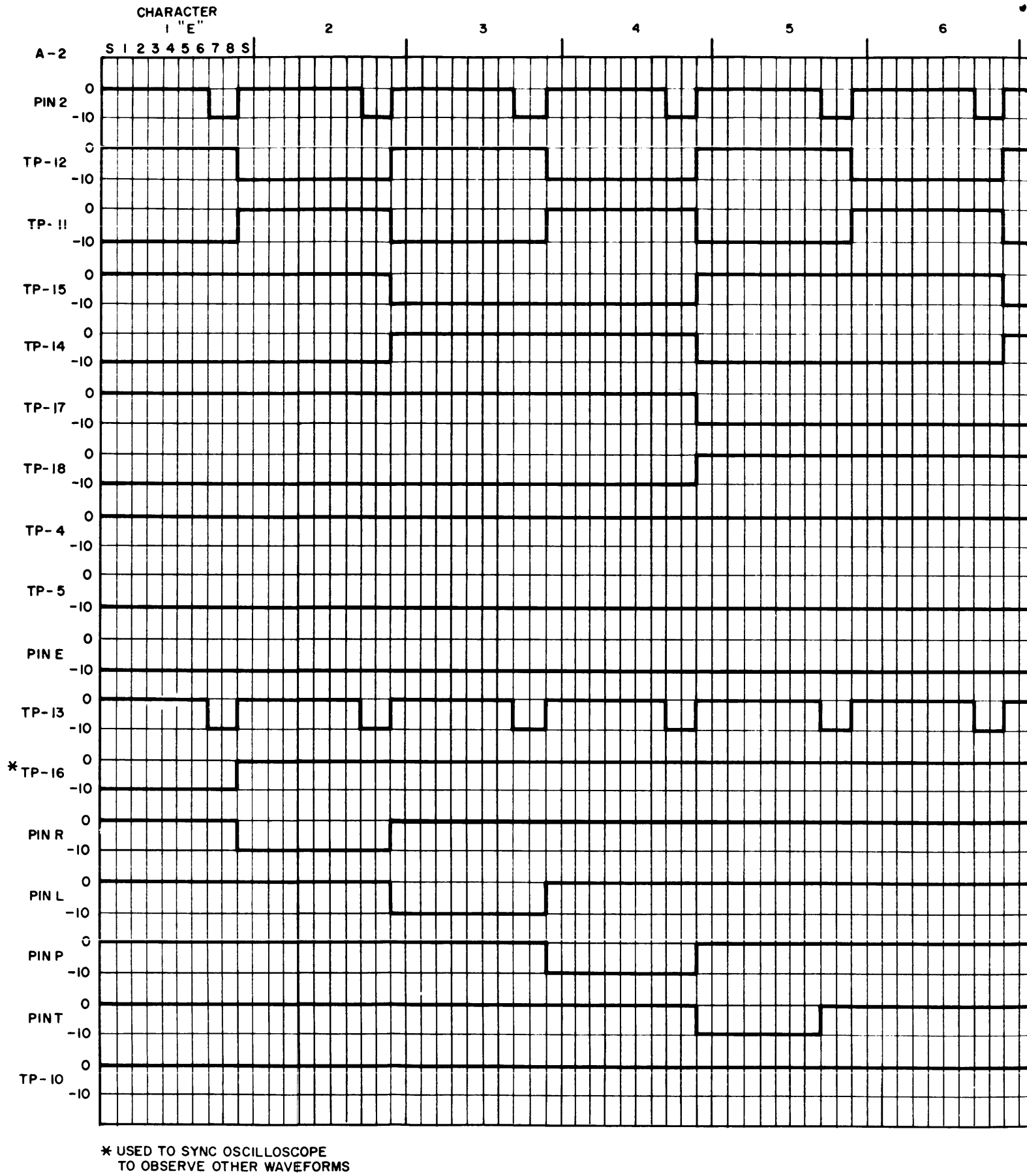

A
B
C
D
E
F
BIT 1
2
3
4
5
6WIP
1J4
G
H
J
K
15 16 18 19
P/O 3A18 1MC STEP SWITCH ASSY (SAME AS 3A19)
P/O 3A17 100KC STEP SWITCH ASSY (SAME AS 3A19)
P/O 3A16 10KC STEP SWTCH ASSY (SAME AS 3A19)
P/O 3A15 1KC STEP SWITCH ASSY (SAME AS 3A19)
P/O 3A14 0.1 KC STEP SWITCH ASSY (SAME AS 3A19)
CONT. FROM SH. 1
B
3J8
f
a
L
B
A
6WIP
L
M
N
P
Q
R
S
T
U
V
W
X
1KC GATING
0.1 KC GATING

Figure 4-12. Timing Chart, Command Signal Decoder KY-661/URR (Sheet 1 of 5) Card A2



* USED TO SYNC OSCILLOSCOPE
TO OBSERVE OTHER WAVEFORMS

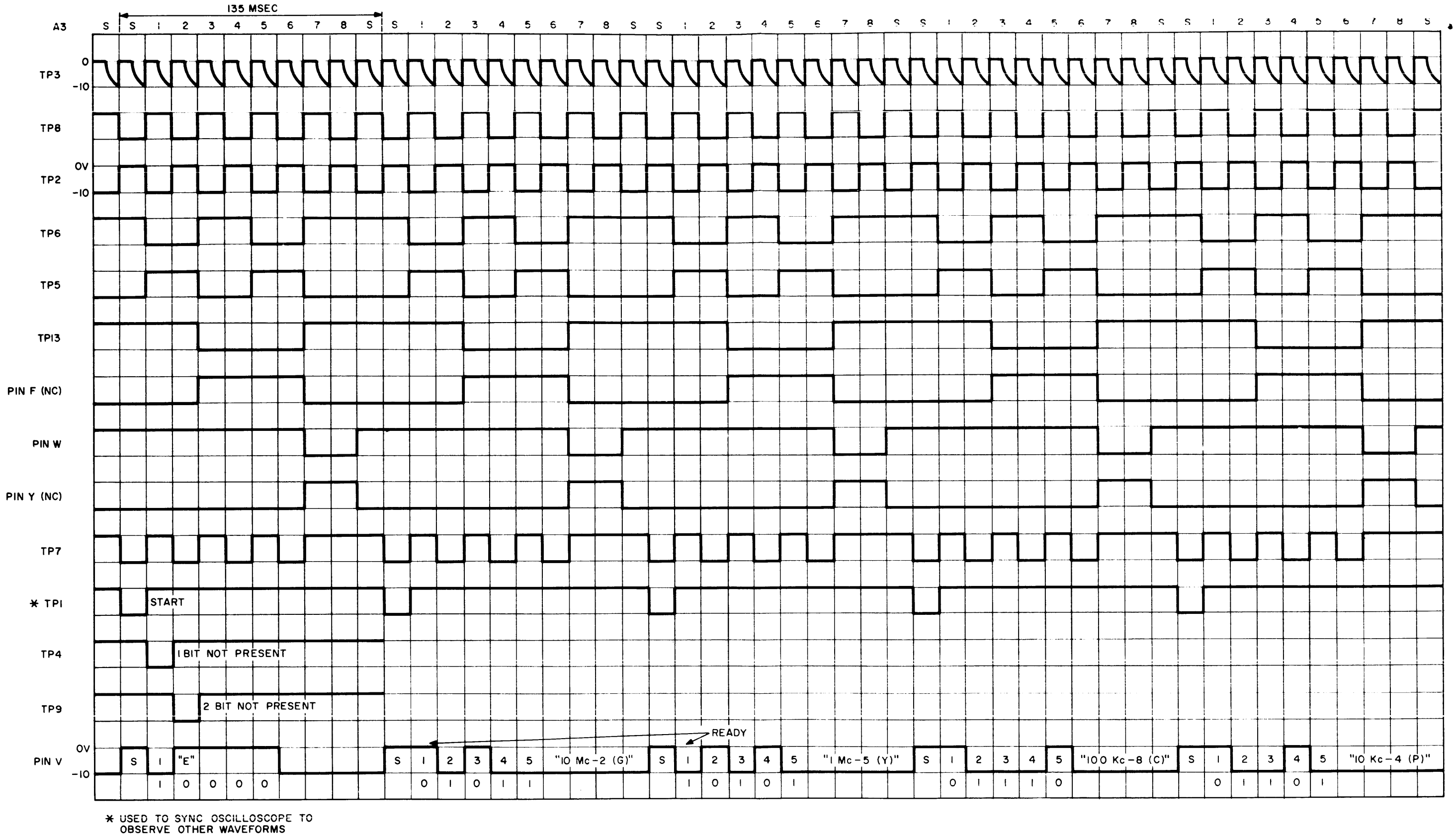
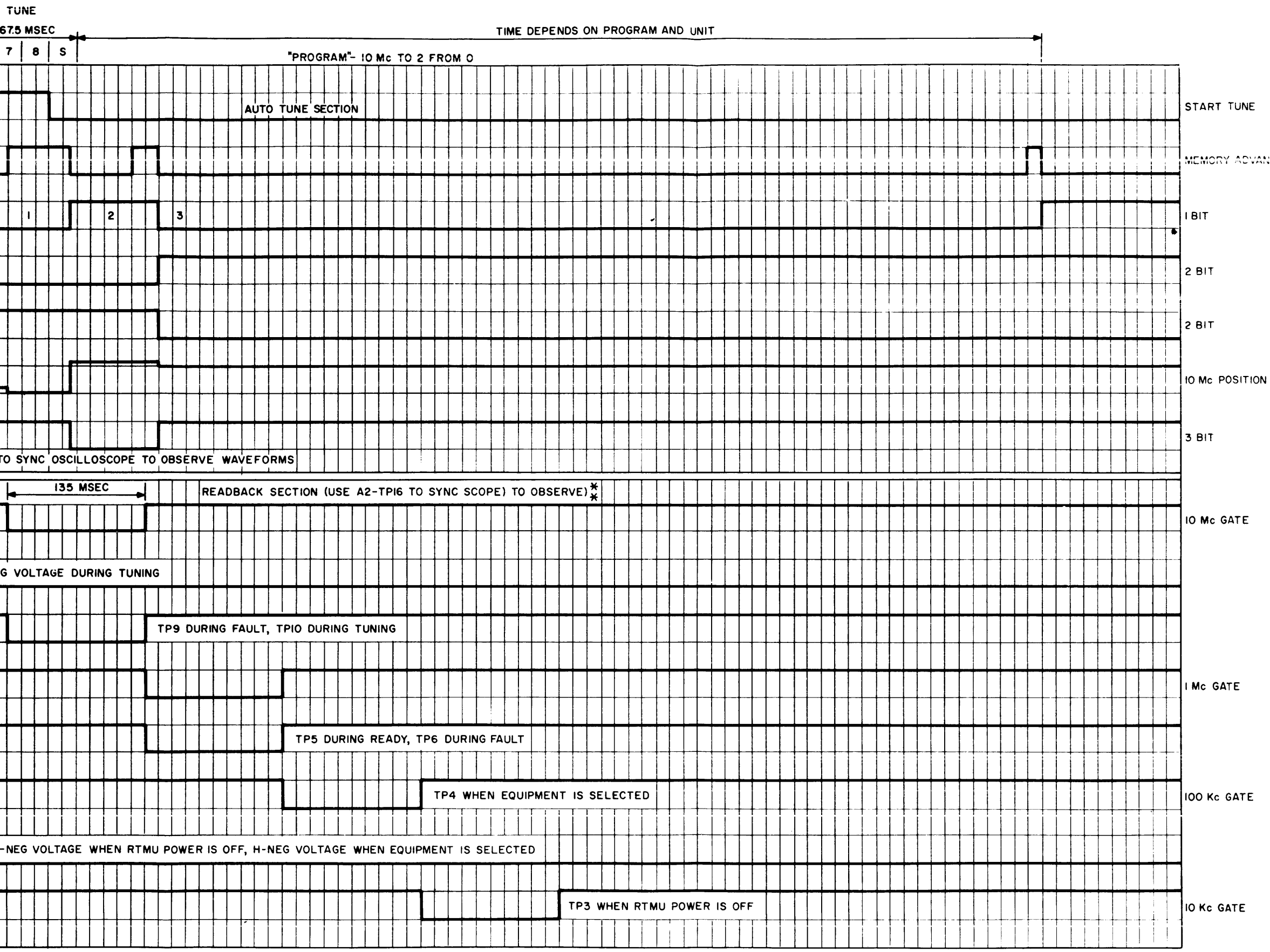
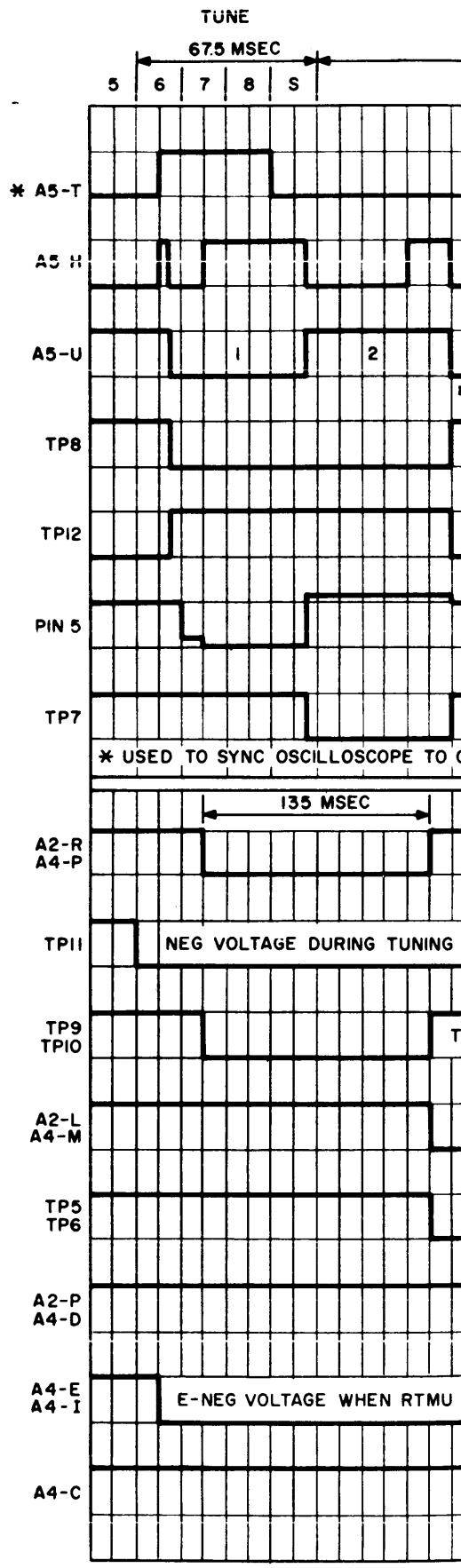


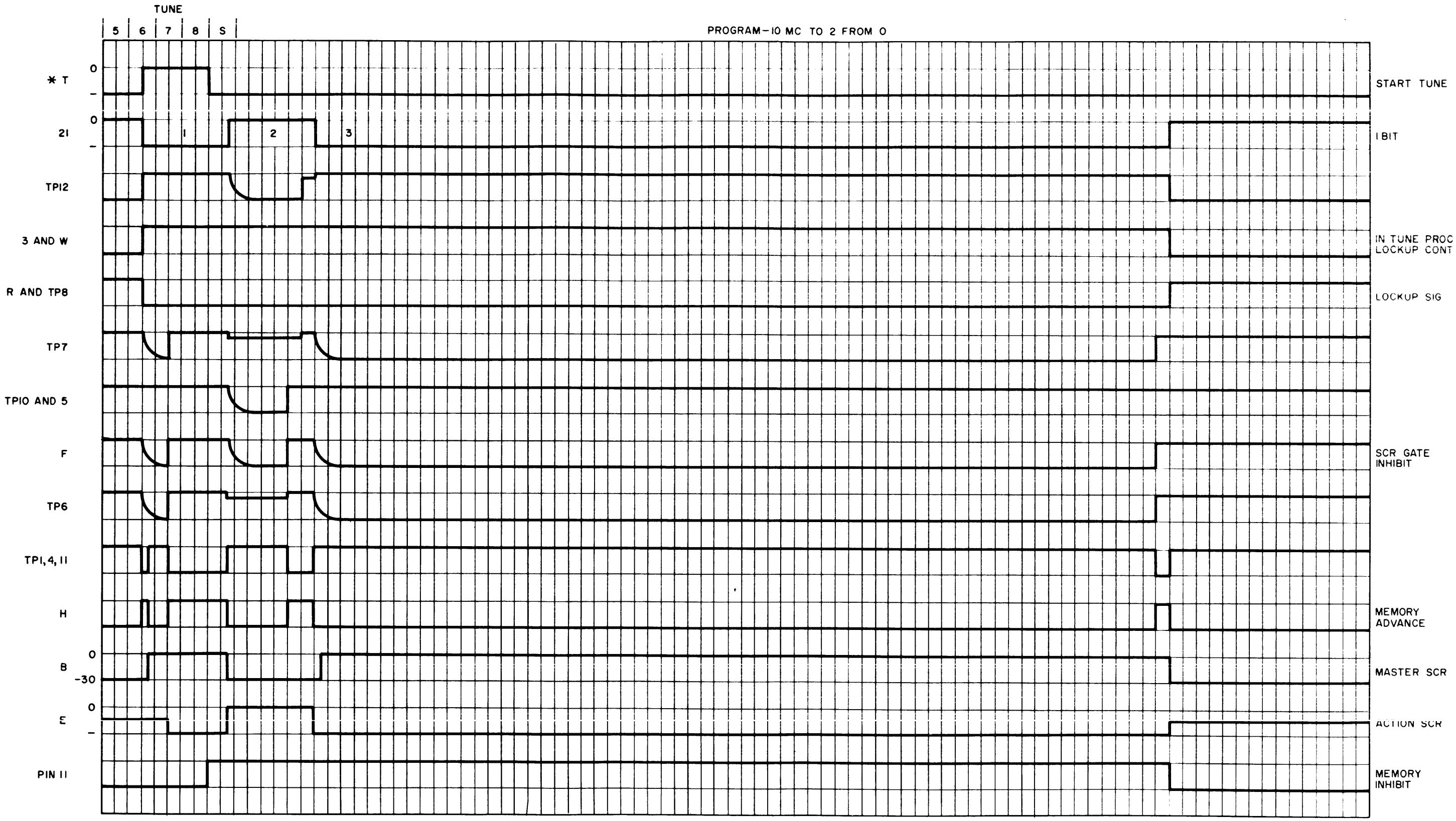
Figure 4-12. Timing Chart, Command Signal Decoder KY-661/URR (Sheet 2 of 5) Card A3



** NOTE: READBACK SECTION.
ABOVE WAVEFORMS WILL CONTINUE UNTIL THE NEXT READBACK CYCLE THEN THEY WILL BE REPEATED UNLESS THE RECEIVER FUNCTIONS HAVE CHANGED.

Figure 4-12. Timing Chart, Command Signal Decoder KY-661/URR (Sheet 3 of 5) Card A4


TUNE
67.5 MSEC
5
6
7
8
S
* A5-T
A5 H
A5-U
1
2
TP8
TP12
PIN 5
TP7
* USED TO SYNC OSCILLOSCOPE TO
135 MSEC
A2-R
A4-P
TP11
NEG VOLTAGE DURING TUNING
TP9
TP10
A2-L
A4-M
TP5
TP6
A2-P
A4-D
A4-E
A4-I
E-NEG VOLTAGE WHEN RTMU
A4-C



1. MASTER LEDEX TO 10 Mc
2. 10 Mc SWITCH FROM 0 TO 2
3. MASTER LEDEX TO HOME

* USED TO SYNC OSCILLOSCOPE TO OBSERVE WAVEFORMS

Figure 4-12. Timing Chart, Command Signal Decoder KY-661/URR (Sheet 4 of 5) Card A5

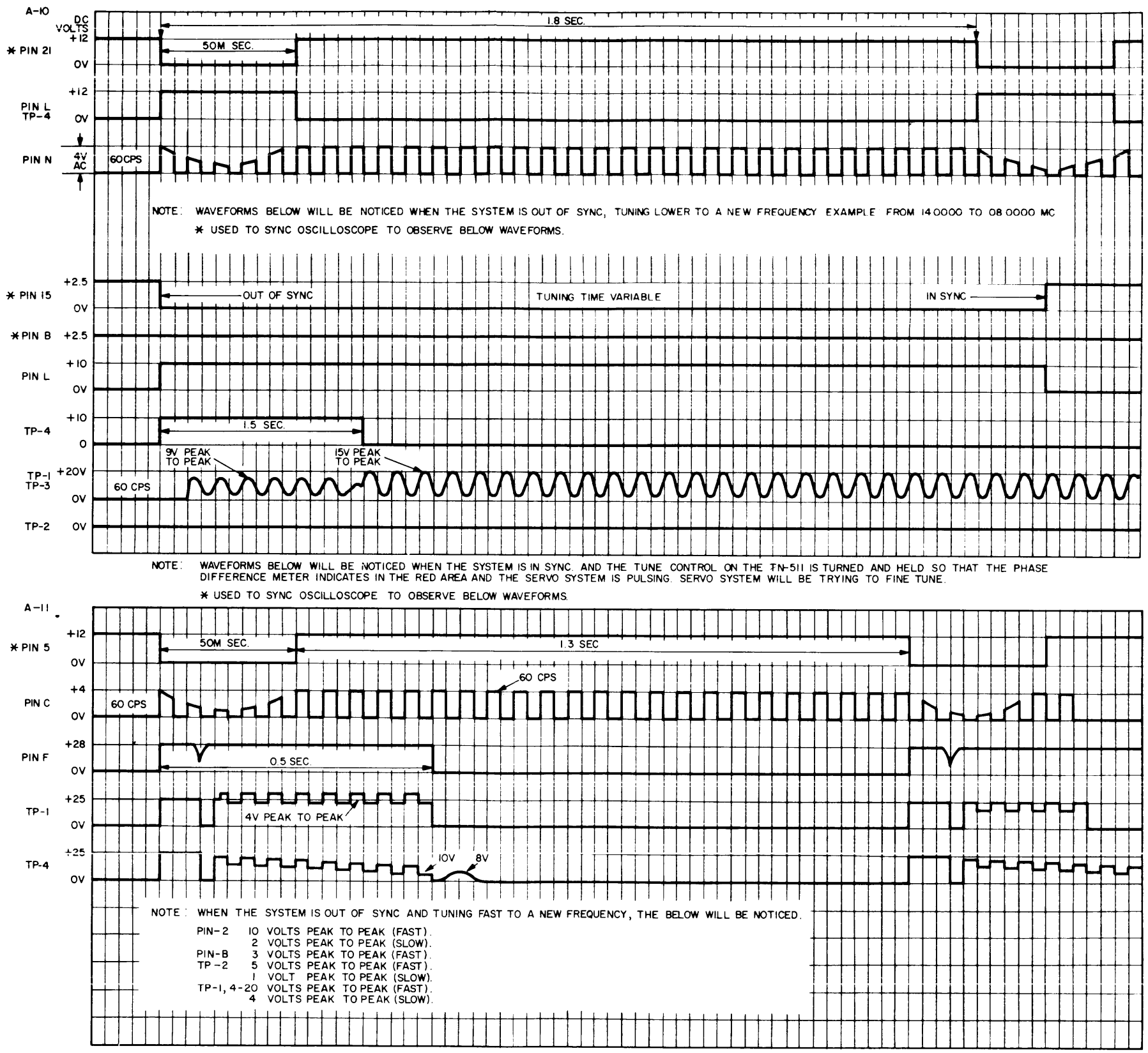
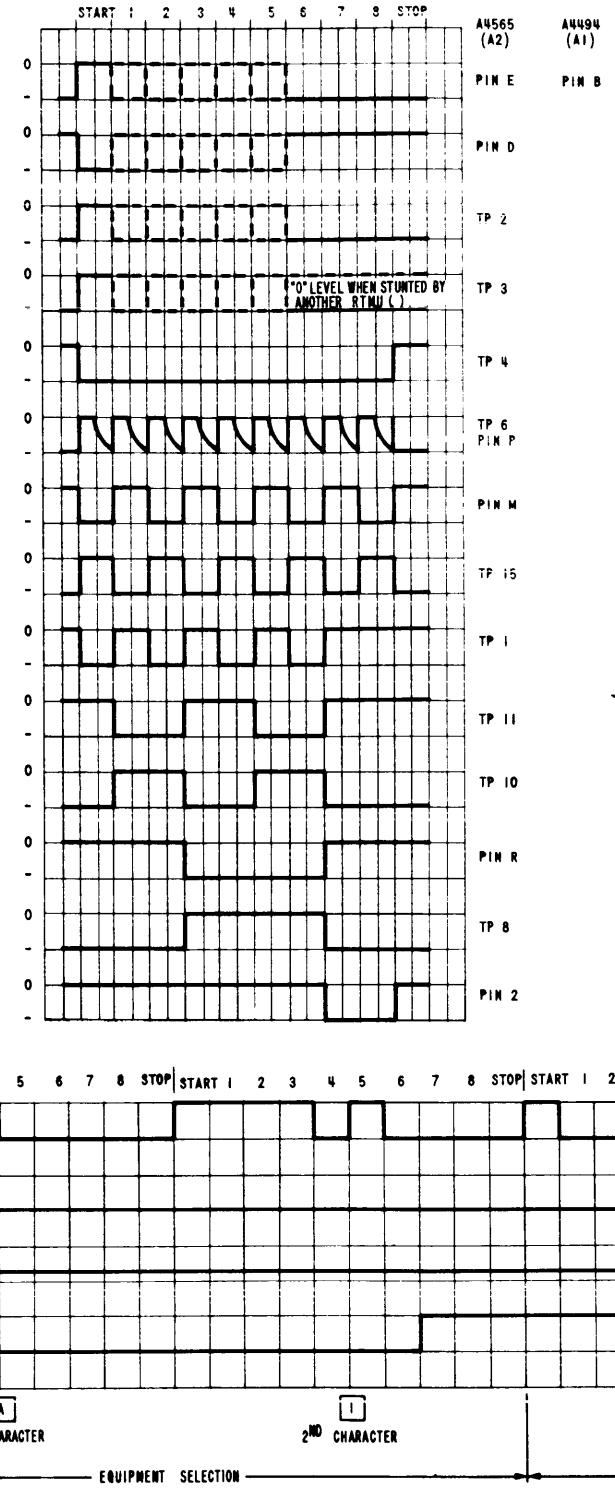
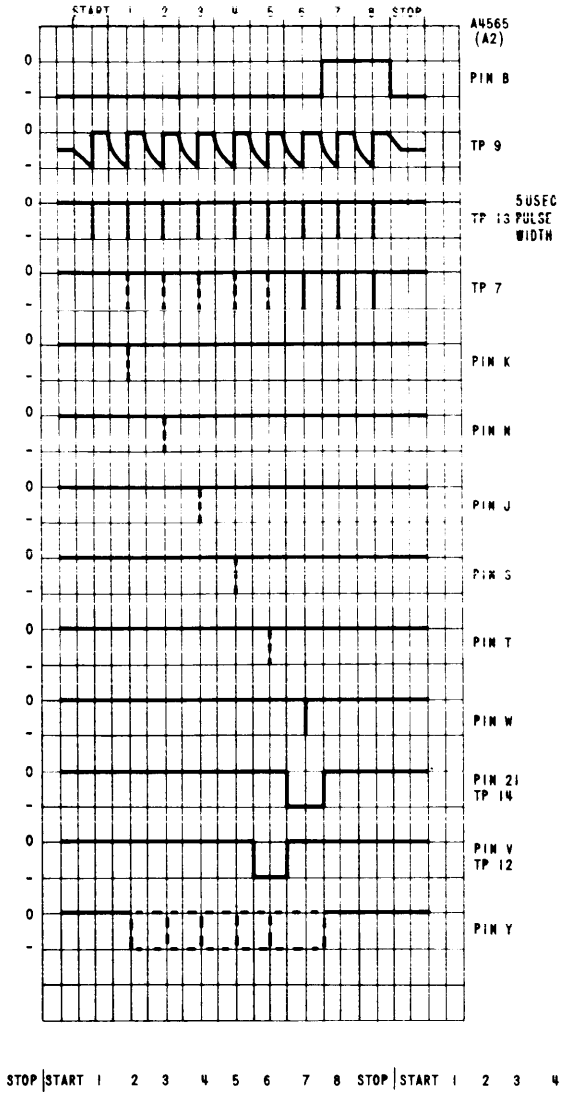
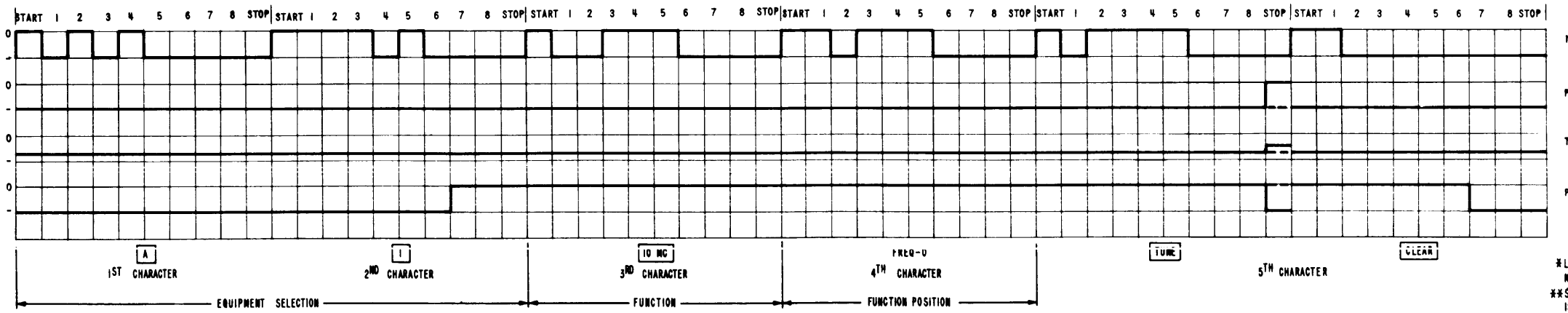


Figure 4-12. Timing Chart, Command Signal Decoder KY-661/URR (Sheet 5 of 5) Card A10 Card A11







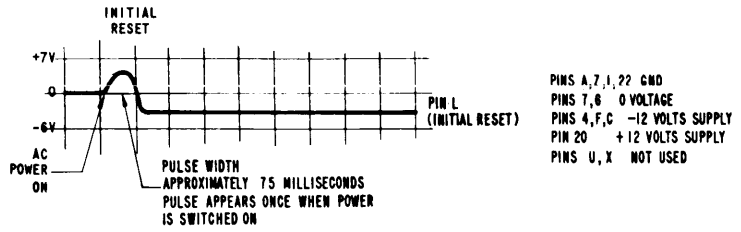
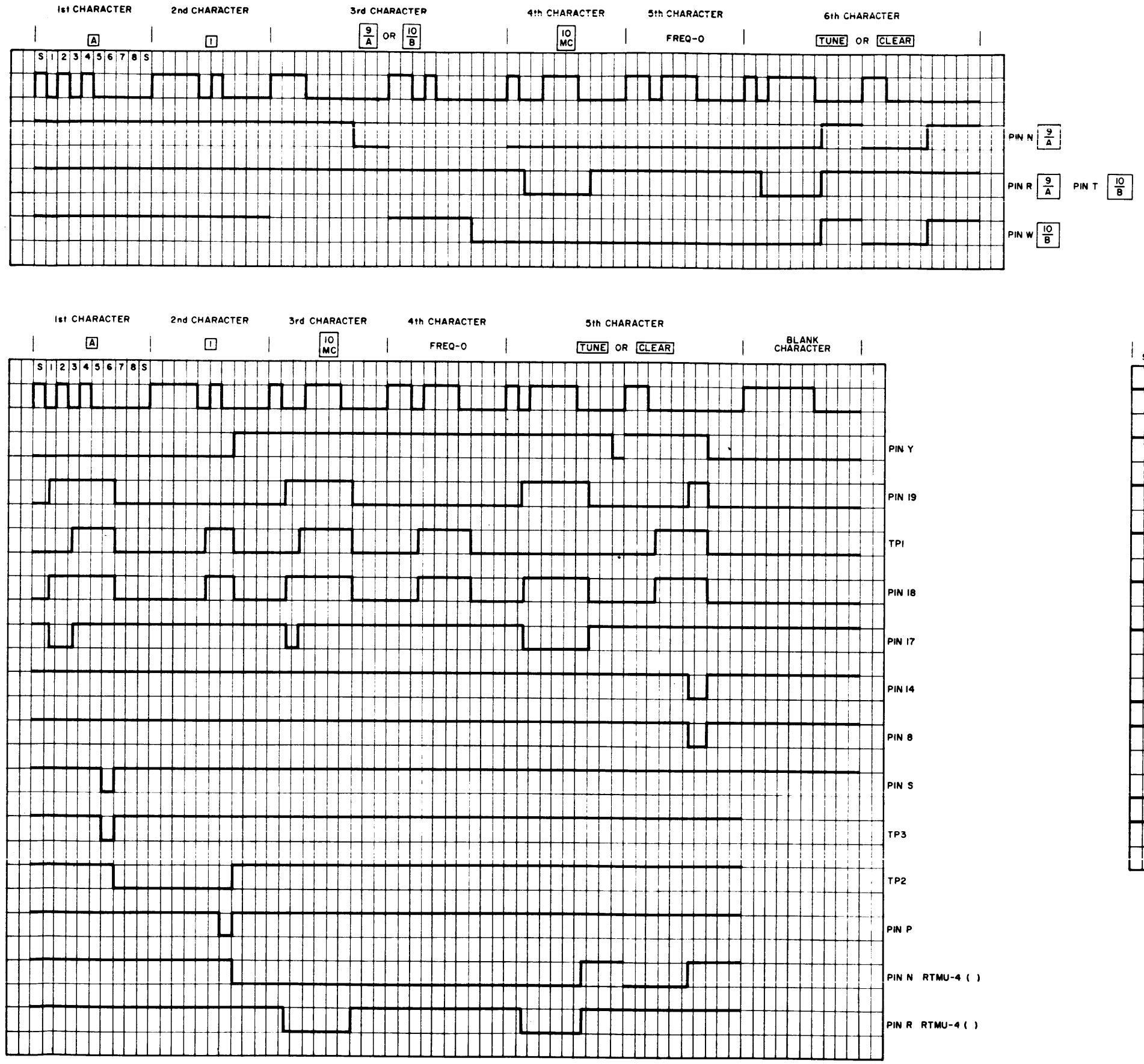
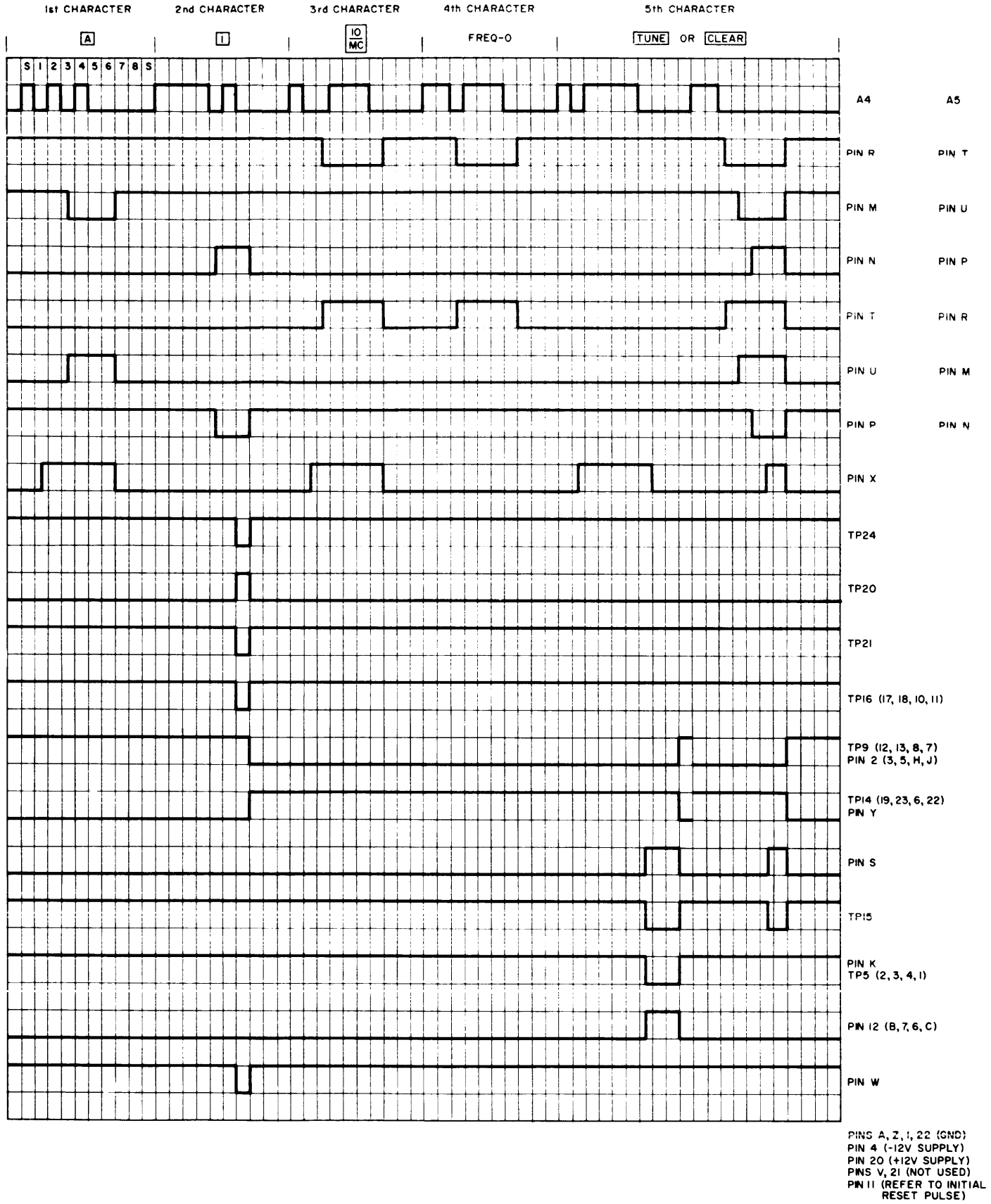


Figure 4-13. Timing Chart, Signal Data Converter-Storer CV-2520/URR (Sheet 1 of 10) Card A2



011690392

Figure 4-13. Timing Chart, Signal Data Converter-Storer CV-2520/URR (Sheet 2 of 10) Card A3



Card A4
Card A5

Figure 4-13. Timing Chart, Signal Data Converter-Storer CV-2520/URR (Sheet 3 of 10)

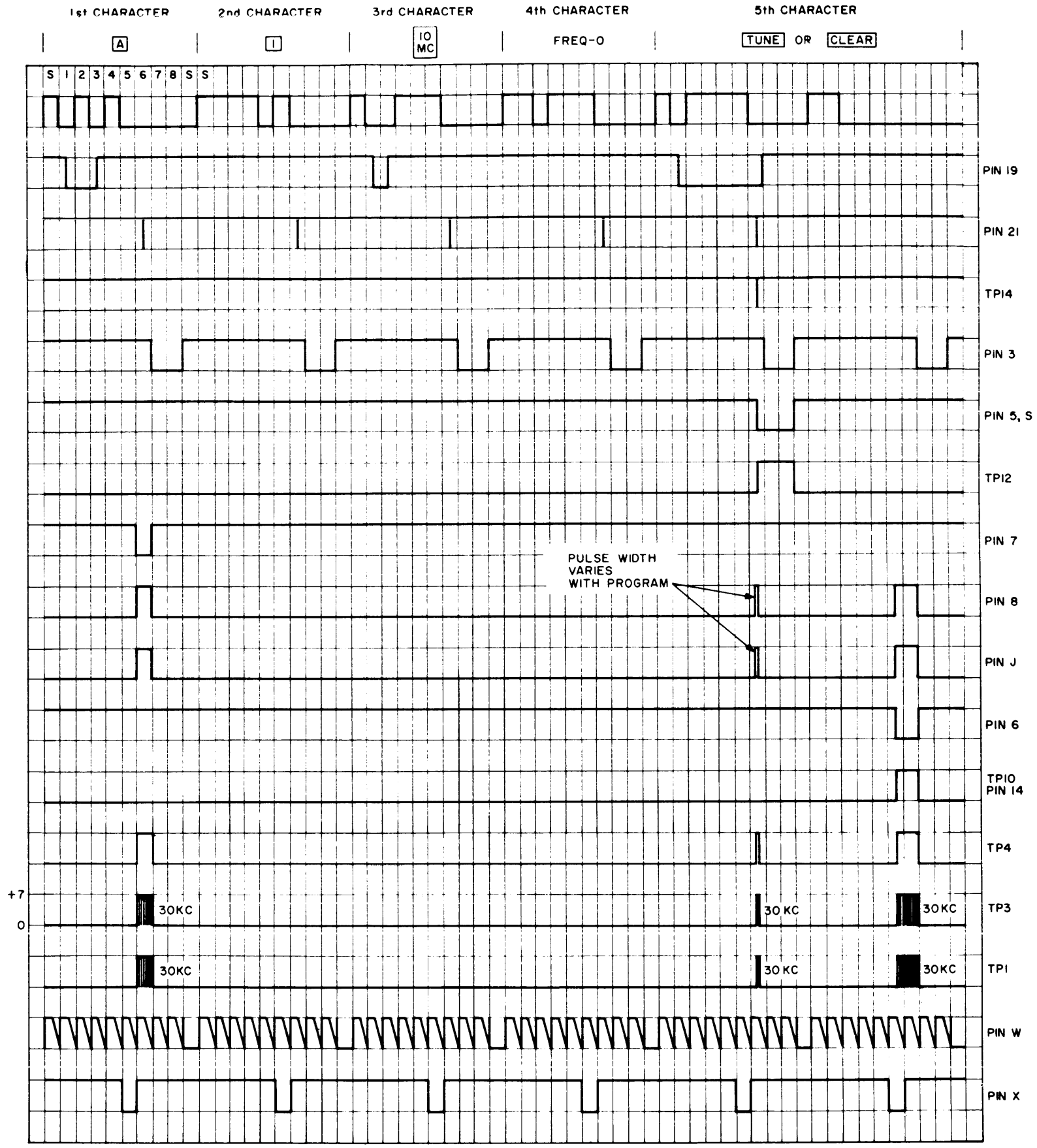


Figure 4-13. Timing Chart, Signal Data Converter-Storer CV-2520/URR (Sheet 4 of 10) Card A6

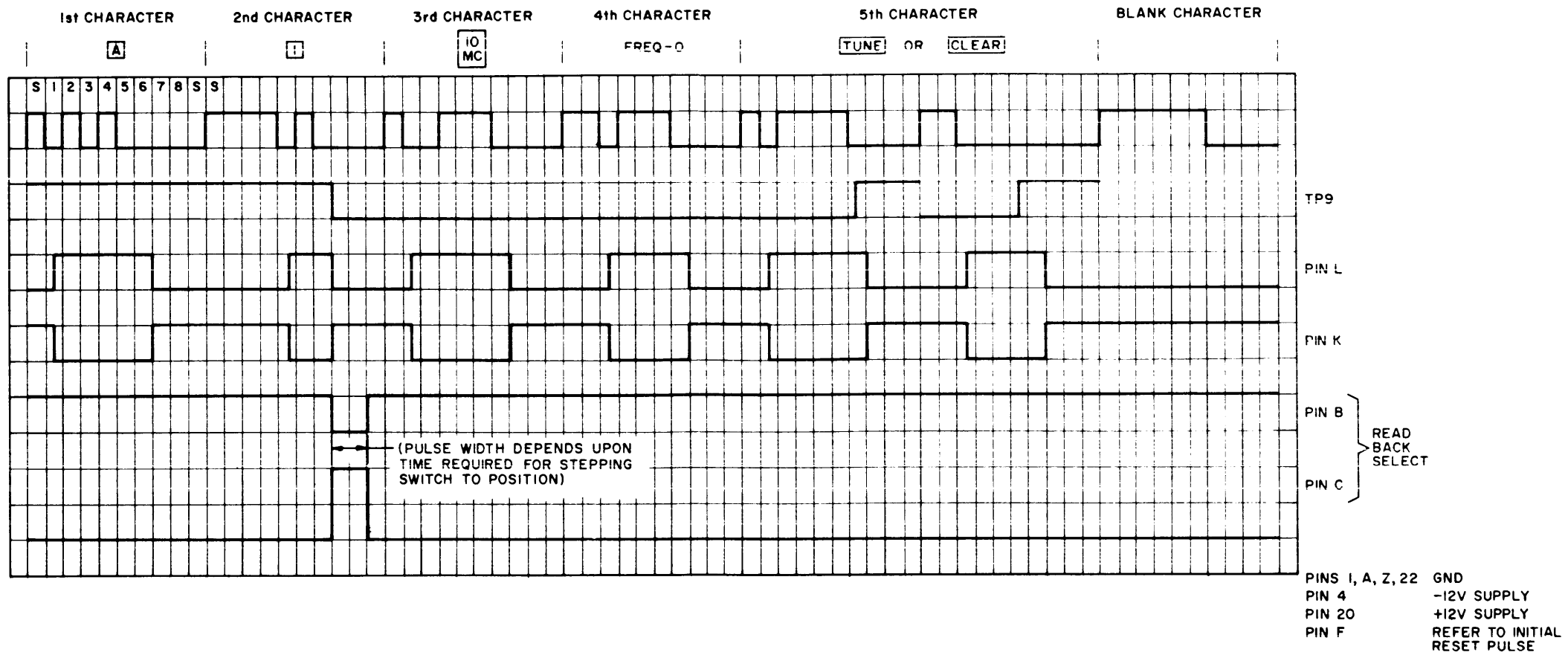
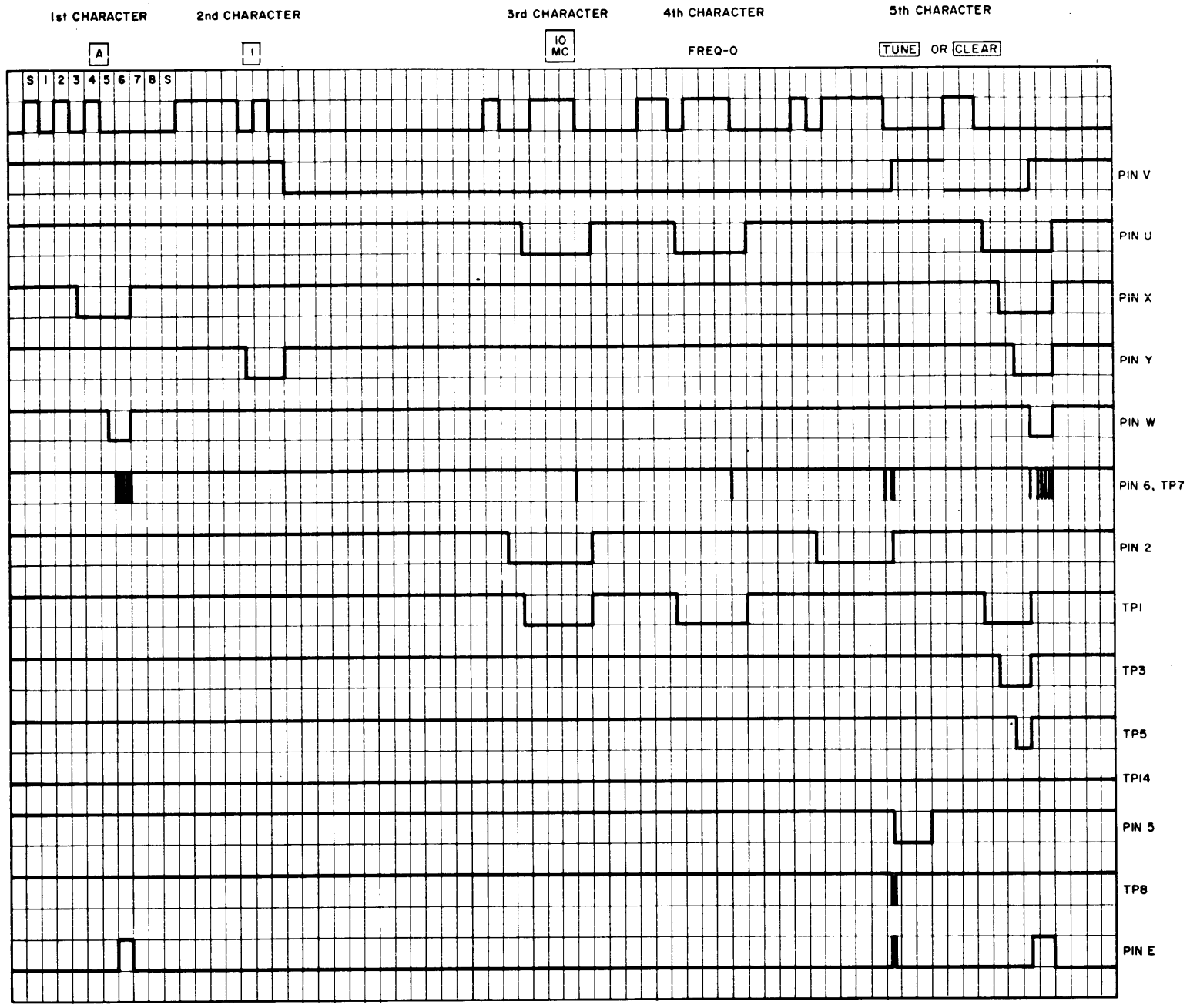


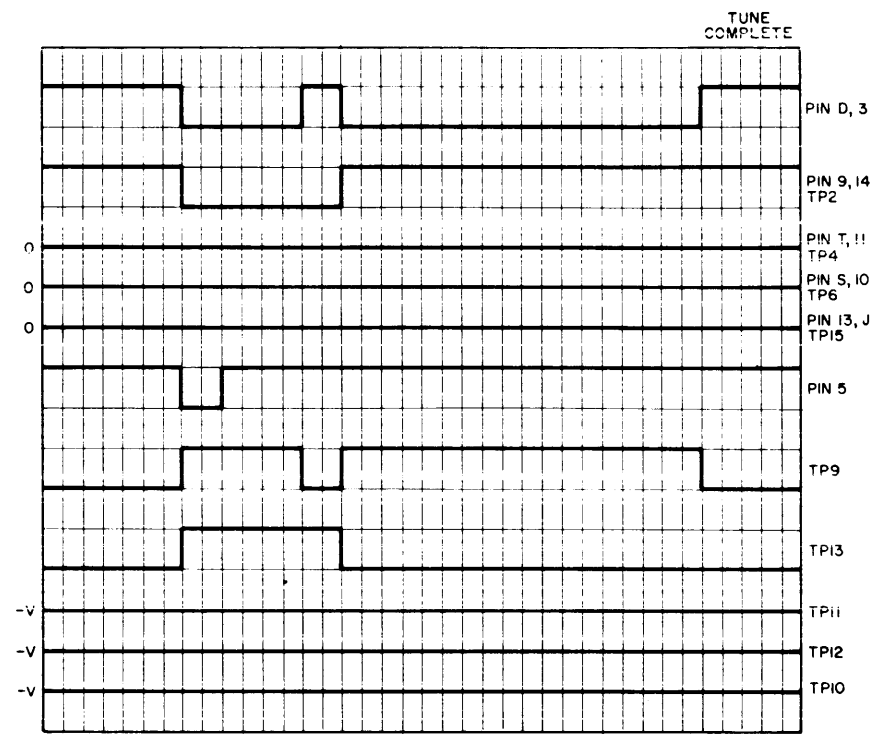
Figure 4-13. Timing Chart, Signal Data Converter-Storer CV-2520/URR (Sheet 5 of 10) Card A6

NOTE

WAVEFORMS ON PIN J, TP-5, TP-2, TP-15, TP-8, AND PIN P DURING TUNING CYCLE ONLY.

Figure 4-13. Timing Chart, Signal Data Converter-Storer CV-2520/URR (Sheet 6 of 10) Card A6





PINS 1, A, Z, 22, C -GND
PIN 4 -12V SUPPLY
PIN 20 +12V SUPPLY
PIN 21 -27V SUPPLY

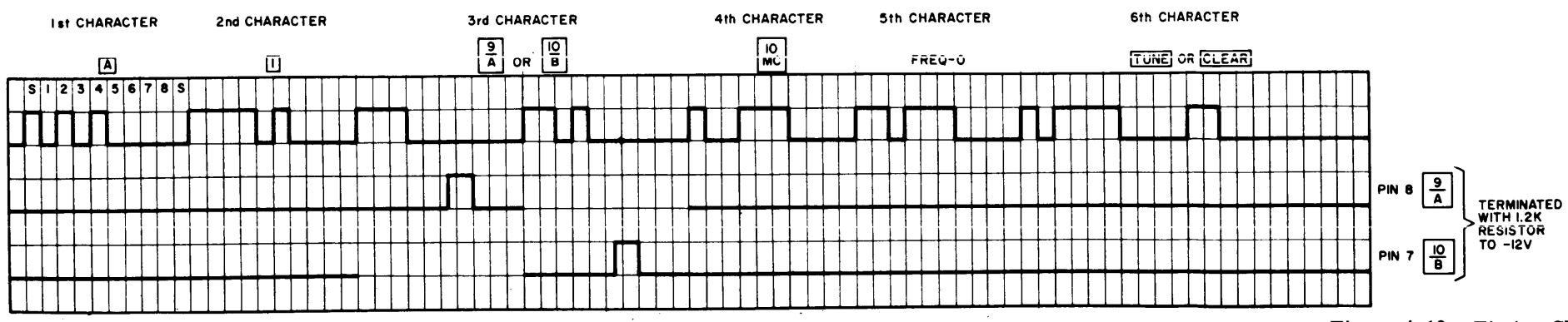


Figure 4-13. Timing Chart, Signal Data Converter-Storer CV-2520/URR (Sheet 7 of 10)

Card A7
Card A8

011690392

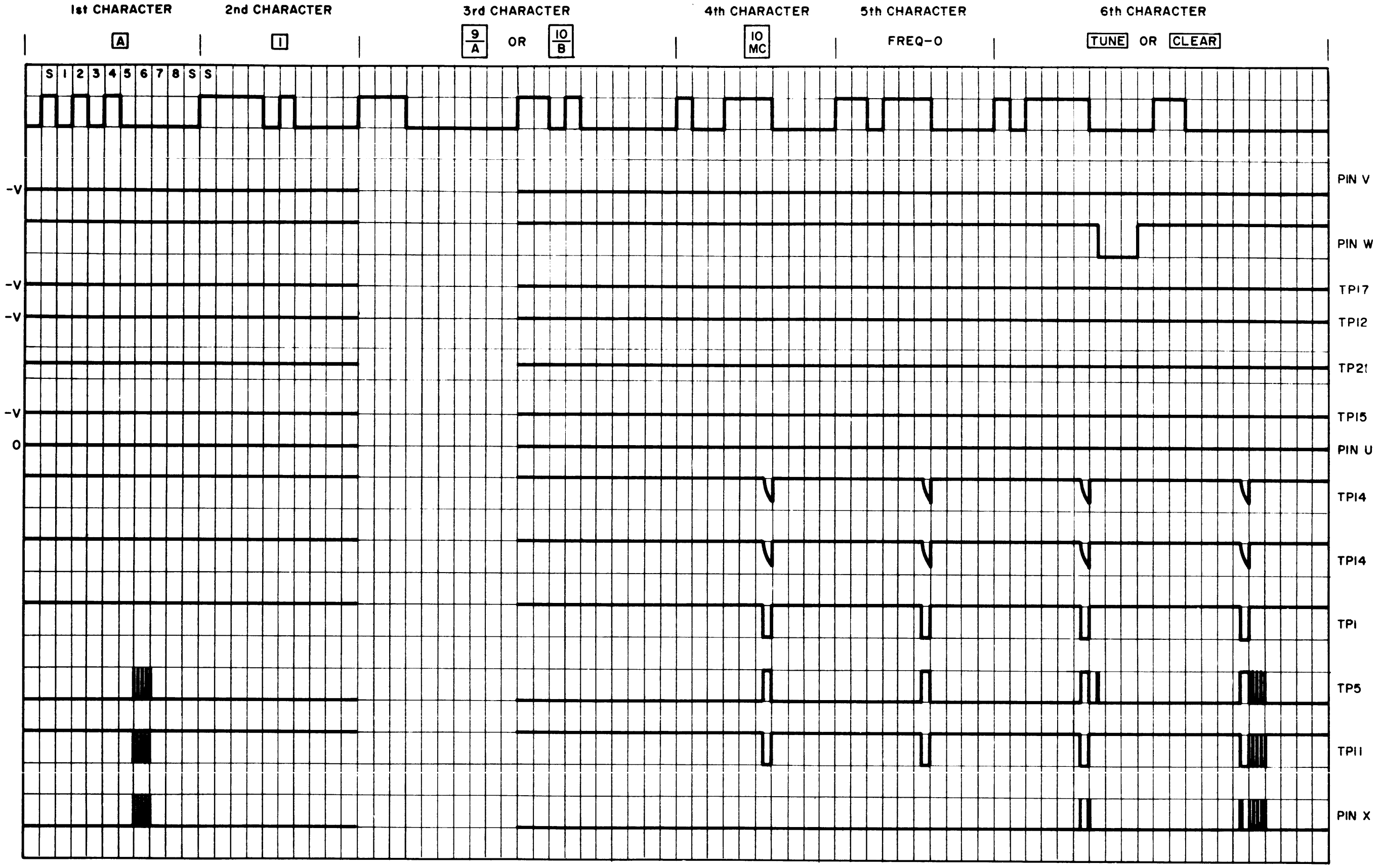


Figure 4-13. Timing Chart, Signal Data Converter-Storer CV-2520/URR (Sheet 8 of 10) Card A9

011690392

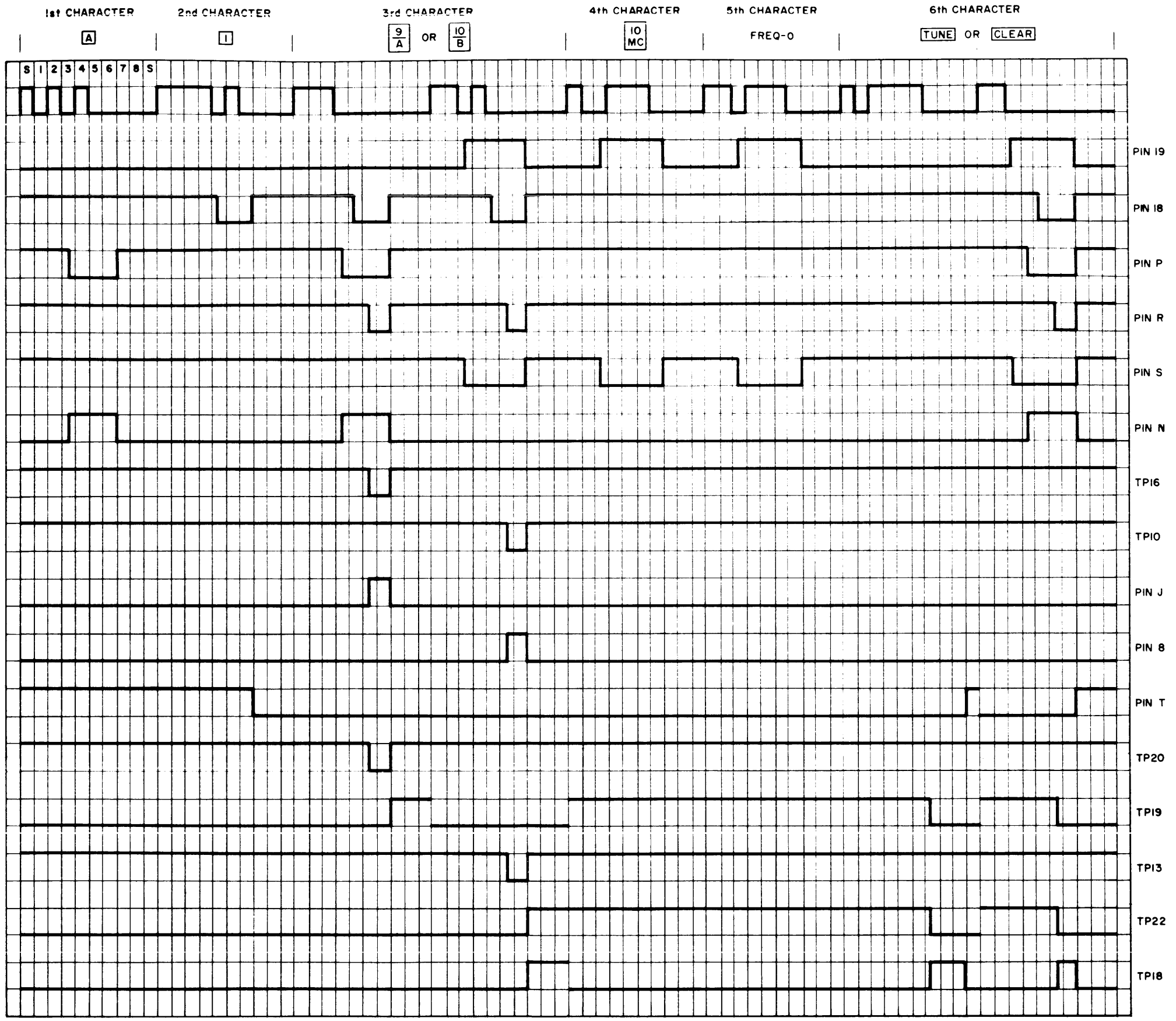


Figure 4-13. Timing Chart, Signal Data Converter-Storer CV-2520/URR (Sheet 9 of 10) Card A9

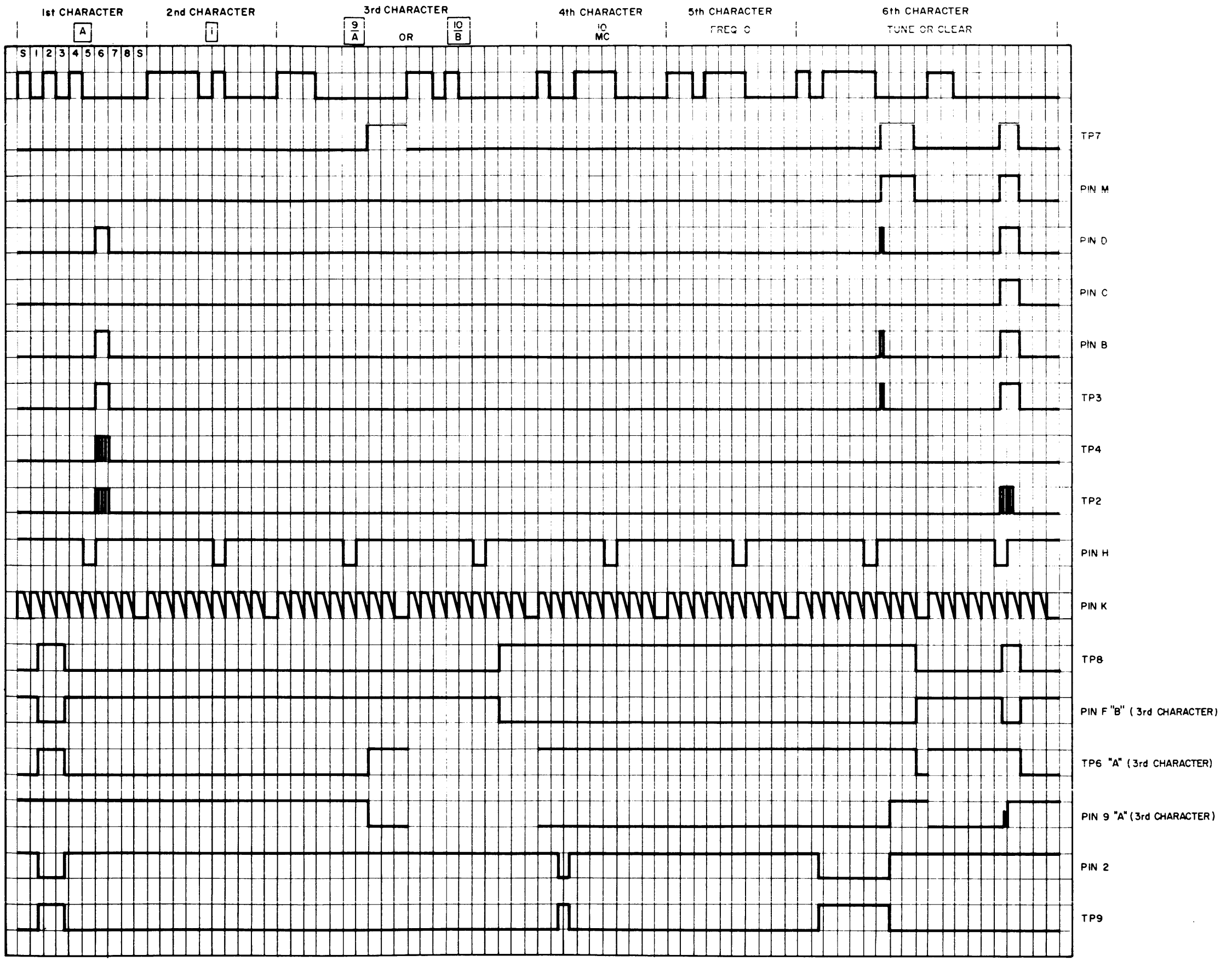


Figure 4-13. Timing Chart, Signal Data Converter-Storer CV-2520/URR (Sheet 10 of 10) Card A9

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