10382 DUAL EIA/NEUTRAL INTERFACE CIRCUIT CARD — TAU3

. Basic Function

'he 410382 circuit card assembly provides the SCCAT based Model 42 Terminal (4220) with a main inter- ıce consisting of either an EIA RS-232C interface or a neutral current loop interface. A secondary or AUX" EIA interface is provided to allow interfacing the Reperforator/Transmitter (R/T) unit to the erminal. The main EIA interface is intended for operation with a modem. Both EIA interfaces are termi- ated in standard EIA type connectors which are mounted to the noncomponent side of the circuit card. 'he neutral current loop interface, which functions in parallel with the main EIA interface, provides peration on all known neutral current loops such as those provided by the Telex network. Loop connec- ions are made via a terminal block located on the noncomponent side of the circuit card.

:. EIA Interfaces

'he EIA signals to and from the 410382 circuit card will be +3 V to +25 Vdc to represent an "ON" condi- ion for control signals and a "SPACE" for data signals. An "OFF" or "MARK" condition is represented ›y a voltage level of -3 V to -25 Vdc. Following is a list by pin numbers of the signals present at both EIA onnectors:

'he main EIA interface shifts the logic level signals from the controller (J103), to EIA level signals for pplication to a modem (J105). It also shifts the EIA level signals from the modem to logic level signal equired by the controller.

;D (Send Data) from the controller at J103 pin 19 (B3) is a mark when high and a space when low. The ignal is inverted at MLB10-12 and is applied to MLB9-4 (C3). MLB9-6 will be low when SD is spacing hereby illuminating LED 1. The inverted SD signal is inverted again at MLB11-2 (B4) and applied to EIA ıriver MLA8 on pin 2. MLA8-3, which is connected to the main EIA connector (J105 pin 2), will be pproximately +12 V for a space and -12 V for a mark. The DTR (Data Terminal Ready) signal at J103 ›in 5 (C3) functions identically as the SD signal. LED 2 will be illuminated when DTR is active. J105 pin :0 will be approximately +12 V when DTR is on and approximately -12 V when DTR is off. The remaining hree signals from the controller, SRTS (Secondary Request to Send), RTS (Request to Send) and AL Analog Loop) are applied directly to their respective EIA drivers.

'he CTS (Clear to Send), DSR (Data Set Ready), DCD (Data Carrier Detect) and RD (Receive Data) from he modem are applied via J105 to MLB8 (D5) which shifts the EIA levels to logic levels. The outputs of ILB8 at pins 11, 3 and 6 will be low when the CTS, DSR and DCD signals are active (approximately -12 V) and high when inactive (approximately -12 V). The output at MLB8-8 (D5) will be high when RD s a mark and low when a space. The output of the CTS receiver (MLB8-11) is applied to the controller ia J103 pin 12. The outputs of the DSR and DCD receivers (MLB8-3 and 6) are applied to MLB12-4 and ;. When these two inputs are low, the output at MLB12-6 will go low forcing MLB13-3 high.

f ST1 (D4) (Normal/Private Line) is in the "Normal" position, MLB12-8 will be high, placing a low on 103 pin 15 via MLB10-4. Additionally MLB10-6 will go low illuminating LED 3. Should ST1 be in the 'Private Line" position, MLB12-8 will be high regardless of the state of the signal at MLB12-10. The DR Data Ready) signal at MLB13-2 is generated by the receive side of the neutral current loop circuitry and s used to control the DSR output to the controller when the neutral current loop circuitry is selected as he main interface. The output of the RD receiver at MLB8-8 drives MLB12-1. MLB12-3 (D4) will follow he condition of pin 1 since the RD input at MLB12-2 is low until driven by the receive side of the neutral oop interface. MLB12-3 drives the RD output to the controller via J103 pin 17 and will be low for a pace and high for a mark. In addition, this signal is double inverted by MLB10-10 and 8 (E4) and will lluminate LED 4 when RD to the controller is spacing.

The auxiliary EIA interface which terminates at J106 (C3) provides a means of interfacing the Reperforator/ Transmitter (R/T) unit to the terminal controller. This interface operates independently and provides ›nly level shifting. Signal polarities are the same as those on the main EIA interface.

B. CIRCUIT DESCRIPTIONS (Contd)

410382 DUAL EIA/NEUTRAL INTERFACE CIRCUIT CARD — TAU 3 (Contd)

3. Neutral Current Loop Interface Circuitry

The neutral current loop interface maintains 2500 V dc isolation from the EIA and logic circuitry, and frame ground. The send side of the interface will operate within an open circuit voltage range of 10 to 276 V dc and a closed circuit current of 16 to 72 mA in either a half or full duplex configuration. In addition, it will limit loop current to approximately 5 mA when in the idle condition. The receive side of this interface will detect both the idle (5 mA) condition and the full loop current (15 mA or greater) condition. The receive loop current must be externally limited to 72 mA.

The neutral current loop interface is the alternate main interface for the 410382 circuit card. The function of the receive circuitry is to detect idle and data loop current in both the forward and reverse direction. The function of the send circuitry is to open and close the loop in response to a mark/space command and to set the loop current to 5 mA in the idle condition.

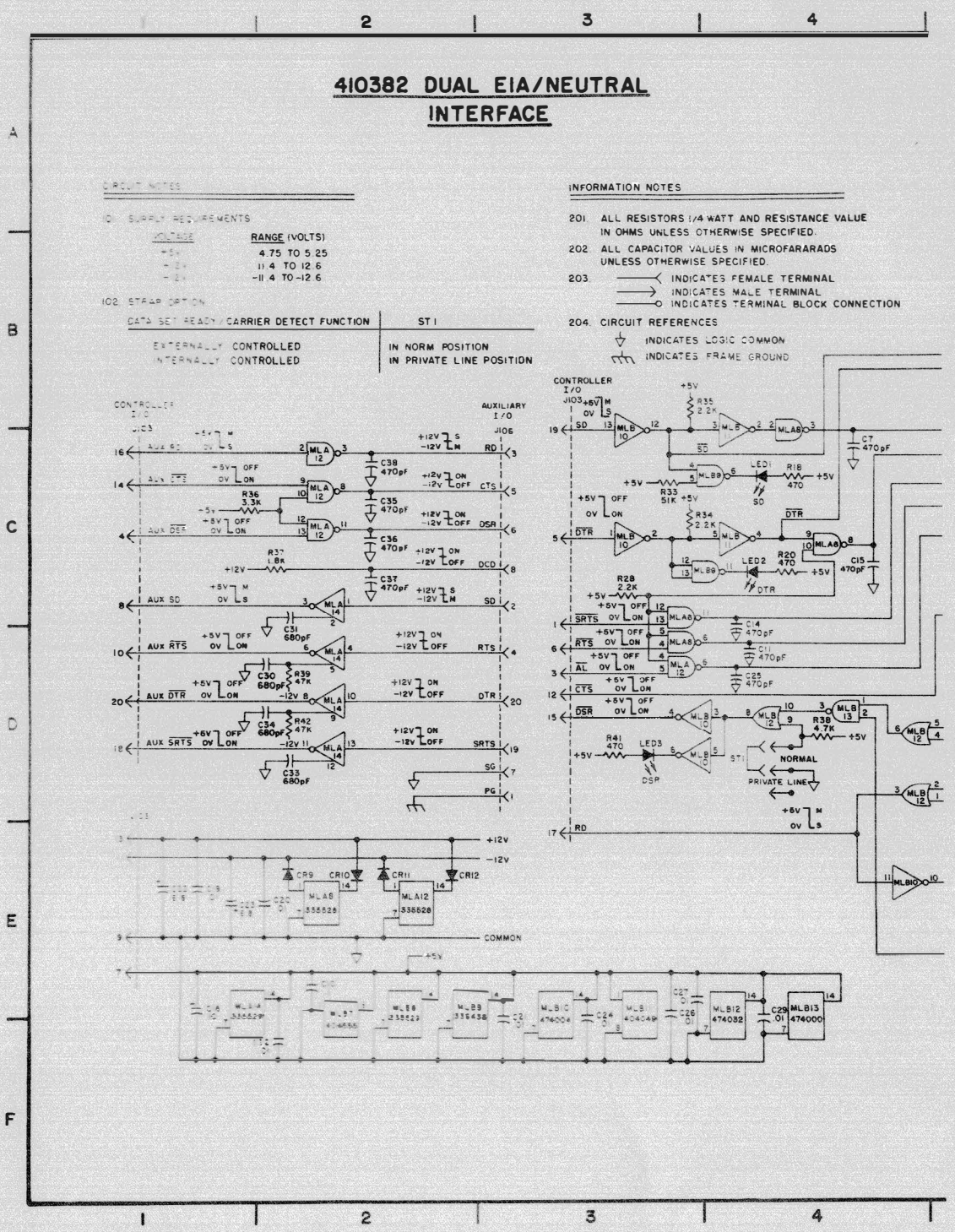
Optical isolator MLB1 (E7) detects idle loop current in the forward direction whereas MLB3 (F7) detects idle loop current in the reverse direction. When reverse idle current is detected, MLB3-5 will go low thereby setting the Data Ready Latch at MLB13-13 (E6). The latch output at MLB13-8 will go low which is the alternate source for the main $\overline{\text{DSR}}$ signal to the controller. When forward idle current is detected, MLB1-5 will go low causing the Data Ready Latch to reset. Optical isolator MLB2 (E7) detects forward data current and isolator MLB4 detects reverse data current in the loop. Resistors R1 and R3 shunt approximately 9 mA of loop current from the optical isolators.

Resistors R2 and R4 limit the forward and reverse loop current through the optical isolators to approximately 20 mA. The remaining loop current is passed by Q1 and Q2. When a forward loop current of 15 mA or greater is flowing, MLB2-5 will go low. MLB4-5 will be low when a reverse loop current of 15 mA or greater is flowing. These outputs are double inverted by MLB11 and gated at MLB13. The output at MLB13-6 is the alternate source for the RD signal to the controller.

Timer MLB7 (C6) with its associated components is set to free run at approximately 20 kHz with a duty cycle of about 70%. This timer in conjunction with Q6, T1 and associated components form a dc to dc converter with 2500 Vdc isolation from primary to secondary. The voltage at the secondary of T1 is rectified by CR 8 and filtered by C4 and C5. The output is approximately 12 Vdc and is used as an isolated bias power supply for the neutral loop send circuitry. The SD signal from the logic circuitry is connected to MLB9-2. When SD is a mark, MLB9-3 will be high turning off the LED in optical isolator MLB5. The 5 mA idle current limit circuit consisting of Q4, Q5 and R6 is enabled via R7. When SD is spacing, this circuitry is disabled since the transistor in MLB5 is turned on. The $\overline{\text{DTR}}$ signal from the logic circuitry is connected to MLB12-13 and is gated with the SD signal on MLB12-12. MLB12-11 will go low when both $\overline{\text{DTR}}$ and SD are low. This low causes MLB9-8 to go high turning off the LED in optical isolator MLB6. The send switch (Q3) is turned on via R9 thereby allowing full loop current to flow. When either $\overline{\text{DTR}}$ or SD go high, the transistor in MLB6 is turned on thereby turning Q3 off preventing the flow of loop current. A full wave bridge consisting of CR3 through CR6 allows the send circuitry to operate with reverse polarity applied at TB1. RV1 protects the send circuitry from transient voltage surges.

C. CIRCUIT DIAGRAMS (Contd)

8. 410382 Dual EIA Neutral Interface Circuit Card — TAU3

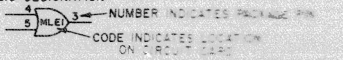


ISSUES 1B THROUGH 3A

205. CONNECTOR INFORMATION

J103 – INTERFACE TO
J105 – MAIN EIA INTERFACE
J106 – AUX EIA INTERFACE
TB1 – NEUTRAL CURRENT LOOP INTERFACE

206. LOGIC DESIGNATION:



207. NOT PRESENT ON ISSUES 1B AND 2A.