INSTRUCTION MANUAL

MODEL 1306

MESSAGE GENERATOR

NOTICE

One diode type used in this equipment is identified in the parts lists and schematic diagrams as General Electric Type 1N4009. In actuality, however, this diode type may have been replaced with Fairchild Types FD100 or FDH600. Both the FD100 and the FDH600 are directly interchangeable with the 1N4009. The Type FDH600 is physically smaller than the Type FD100 and is used on matrix boards where vertically mounted diodes are required.

November 1967
Reprinted May 1968

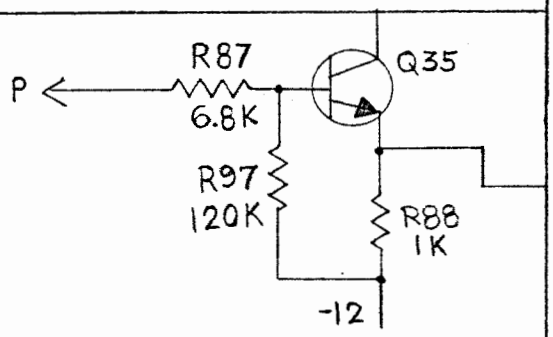
CHANGE NOTICE

1306

CHANGE	SECTION	PAGE	FIG.	REFERENCE	CORRECTION
1	V VI		5-2 6-3	C36	Changed value of capacitor from 820 PF to .002 MF. 7 December 67
2	VI		6-1	Parts list	Changed part number of item 9 to C1303-4 and of item 10 to C1301-5. 22 January 68
3	VI		6-12	L1 and L2	Replaced L1 and L2 with two No. 5250, 100 MH Miller chokes (now item 16 on parts list). Added item 17, am't required of 22 gauge, Alpha, natural tubing. 28 February 68
4	VI		6-7	Parts list	Item 1 changed to N0464B. Item 22 removed. Item 21 changed to two, number 2059 Stimpson eyelets. 22 February 68
5	VI		6-4	Parts list	Item 1 changed to N0454B. 23 February 68
6	VI		6-1	Parts list	Item 31 changed to number 267031-7, Amp connectors. Added item 36 : Six polarizing keys, Amp, number 67611-2. 13 May 68
7	V		5-7	R11	R11 should be 27K. 6 June 68

CHANGE NOTICE

1306

CHANGE	SECTION	PAGE	FIG.	REFERENCE	CORRECTION
8	V VI		5-3 6-4	Q35	 Added 120K resistor R97 from base of Q35 to -12 volt supply. Changed R87 to 6.8K.
	V		5-9	J2 and J6	Wire 49 changed to go from J2-4 to J6-7. Wire 50 changed to go from J2-X to J4-P. 12 June 68

CONTENTS

ILLUSTRATIONS

ILLUSTRATIONS (cont.)

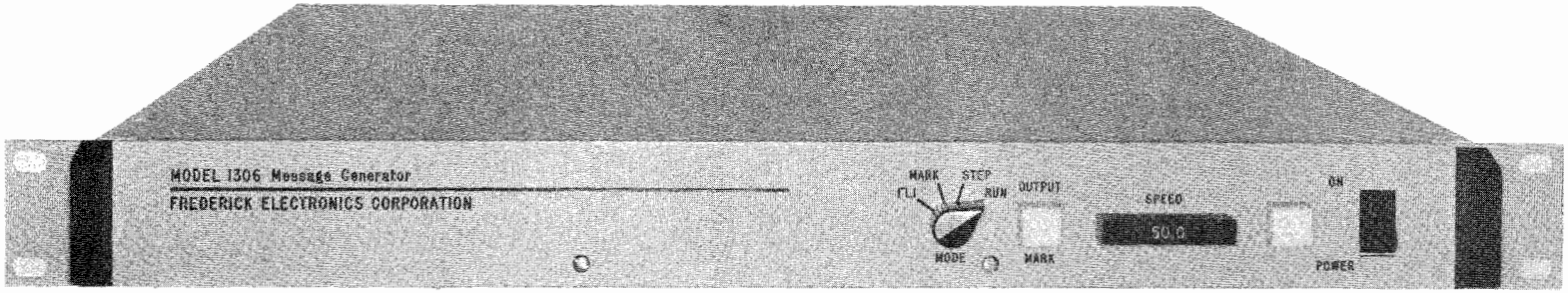


Figure 1-1. Model 1306 Message Generator

SECTION I

INTRODUCTION

1.1 PURPOSE OF EQUIPMENT

The Model 1306 Message Generator is designed to serve as a continuous source of standard 5-level teleprinter code for testing the operation and quality of telegraph terminal systems. The character sequence can be wired to provide a message length of 1 to 80 characters with individual characters tailored to customer requirements.

1.2 PHYSICAL DESCRIPTION

The Model 1306 is an all solid-state device containing five plug-in printed circuit boards housed in an aluminum cabinet 19 inches wide, 18 inches deep, and 1-3/4 inches high. The top cover of the cabinet is removable for maintenance and troubleshooting. Front panel items include two indicator lamps, a mode switch, a power switch, and a slot for accepting miniature plug-in printed circuit boards called "speed chips." The speed chip is the means by which the output baud rate is selected. A separate speed chip is required for each baud rate.

1.3 SPECIFICATIONS

A list of specifications for the Model 1306 Message Generator is contained in table 1-1.

Table 1-1. Specifications, Model 1306

Output Code	Standard 5-level teleprinter code, 7.0 or 7.5 units in length
Output Speed	50 to 1600 wpm, selectable by front panel speed chip
Message Format	Customer option
Message Length	Up to 80 characters
Output Circuit	Provides polar logic level signal with a minimum of ±6 volts into 1000 ohms
Optional Output Circuits	Dry contacts of: 1. A non-isolated 60 ma neutral keyer 2. An isolated 60 ma neutral keyer 3. An isolated 60 ma polar keyer

Table 1-1. Specifications, Model 1306 (cont.)

Step Circuit	Requires a neutral or polar positive logic level with a minimum duration of 1 millisecond. (Circuit reads a single character from unit for each step pulse.)
Burst Circuit	Requires a neutral or polar positive logic level with a minimum duration of 1 millisecond. (Circuit reads a complete message from unit for each burst pulse.)
Power Requirements	115 vac, 50/60 Hz, at approximately 15 watts (can be switched internally for 230 vac operation).
Dimensions	Height: 1-3/4 inches Width: 19 inches Depth: 18 inches
Weight	Approximately 10 pounds

SECTION II

INSTALLATION

2.1 UNPACKING AND INSPECTION

Carefully unpack and remove the Model 1306 Message Generator from its shipping container. Inspect the unit for damage. If any damage is found, file a written claim with the shipping agency. Send a copy of this claim to Frederick Electronics Corporation, P.O. Box 502, Frederick, Maryland 21701.

2.2 POWER REQUIREMENTS

The Model 1306 is normally shipped ready to operate on 105-125 vac, 47-63 Hz. The unit will also operate on 210-250 vac, 47-63 Hz by repositioning an internal 115/230-volt slide switch. This switch is mounted inside the unit on a bracket which also mounts transformer T1. The switch is locked in the 115-volt position. To change to the 230-volt position, proceed as follows:

1. Remove power plug from a-c outlet.
2. Remove top cover of Model 1306.
3. Locate switch and loosen screw holding locking plate.
4. Slide switch to 230-volt position and tighten screw. The unit will now operate on 230-volts a-c.
5. Replace cover and insert power plug into 230 vac outlet.

2.3 MOUNTING

The Model 1306 is designed to mount in a standard 19-inch equipment rack. A vertical rack space of 1-3/4 inches is required. If slide mounting is desired, use Chassis Trak part C-300-S-20.

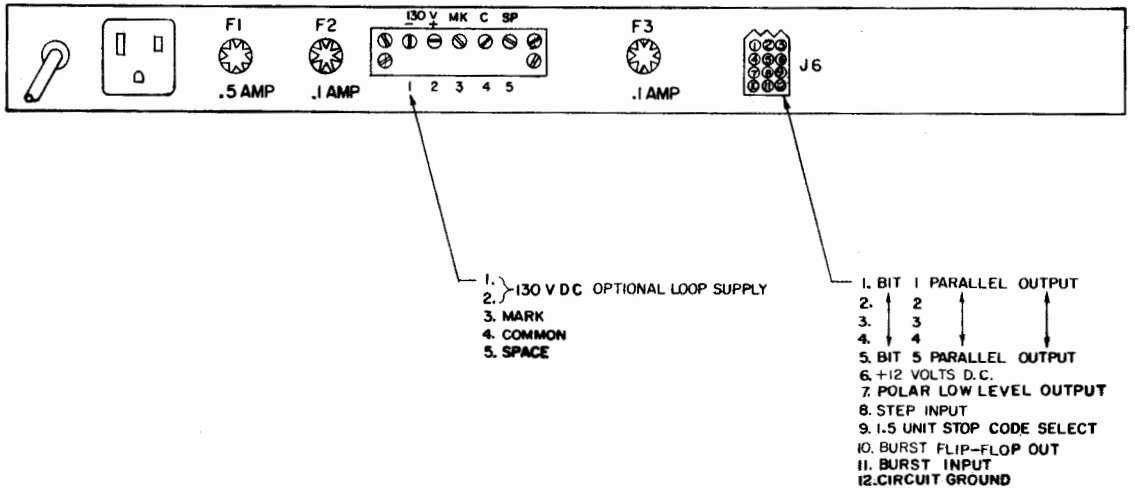
2.4 OUTPUT SIGNAL CONNECTIONS

Figure 2-1 shows the output signal connections for the Message Generator Make those connections that apply to particular operating requirements and ignore those that do not apply.

Refer to details 1 and 2 for instruction in the methods of assembling cable plugs Allow sufficient slack in the cabling to avoid strain on leads or connectors and to allow the unit to be fully withdrawn when slide mounted.

2 4 1 HIGH LEVEL CONNECTIONS TB1

When an optional High Level Keyer is plugged in, the contacts of the keyer's electronic relay will appear at TB1. Under this condition, pin 4 is the common or swinger contact, pin 3 is closed to pin 4 for mark, and pin 5 is closed to pin 4 for space. Neutral



MODEL 1306
REAR PANEL

Figure 2-1. Output Signal Connections
(C1345)

Step 1. Strip about 1/8-inch of insulation from end of lead wire. Wire gauge range: #20 through #24 stranded conductor.

Step 2. Select appropriate pin type and lay lead wire in connector pin valley so that end of insulation is centered at notch between tabs.

Step 3. Using long nose or chain nose pliers, fold down one tab over exposed conductor wires.

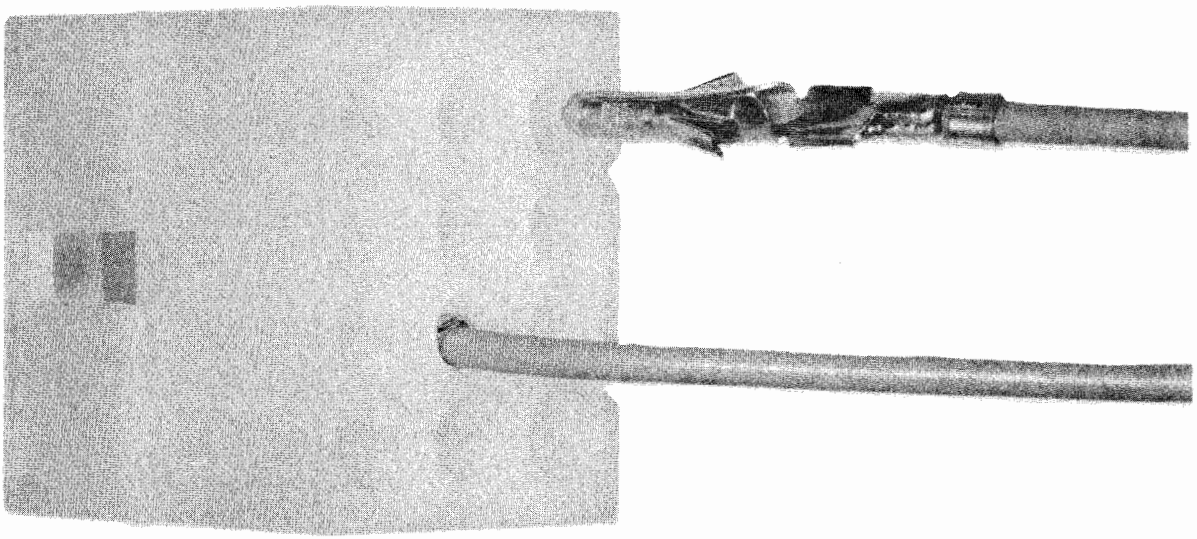
Step 4. Fold down opposite tab over conductor wires.

Step 5. Solder crimped conductor to pin. Do not let solder flow towards pin tip. Avoid melting wire insulation.

Step 6. After pin has cooled, fold down a clamp tab over wire insulation.

Step 7. Fold down the remaining tab over wire insulation to complete pin assembly.

Detail 1. Connector Pin Assembly



As shown above, the complete cable plug is formed by inserting the lead wire and pin assemblies into the proper holes in the rear of the nylon connector body. A small screwdriver blade or similar tool may be used to assure full pin seating by placing the tool along the wire and pressing end-wise on the shoulder formed by tabs wrapped around the wire insulation. Proper seating obtains when the barbs on the pin sides have expanded beyond the hole diameter as viewed from the mating side of the connector plug.

Removal of pins from the connector body for replacement or wiring alterations may be facilitated by the tool listed below. The tool works by collapsing the retaining barbs on a pin so that it may be pulled out.

A hand operated crimping tool is available and may be desirable whenever large numbers of connections are required.

The following items are manufactured by:

Molex Products Company
5224 Katrine Ave.
Downers Grove, Ill. 60515

Removal tool	Part Numbers:	HT-1010-2B
Hand crimping tool		HT-1031-C
Plug connector body		1360-P
Male connector pin		1380
Female connector pin		1381

Detail 2. Connector Assembly

keyers use only pins 3 and 4. The keyer outputs are not polarity sensitive, but an EXTERNAL CURRENT LIMITING RESISTOR MUST BE USED to set loop current to a value below 100 ma. The output keyer is protected with a 1/10 ampere fuse in both the mark and space leads. When driving an inductive load, an additional appropriate resistor-capacitor arc suppressor should be used across the electronic relay contacts.

The optional telegraph Loop Power supply output appears at pins 1 and 2, with pin 2 as the positive terminal. The power supply is capable of continuously supplying a maximum of 100 ma. The voltage may range from 120 volts (full load) to 150 volts (open circuit).

CAUTION

The optional telegraph Loop Power Supply is not protected by internal current limiting or fusing. As a result, a continuous short circuit or current overload may cause equipment damage before the primary power fuse functions. Therefore, check all connections before applying primary power.

When both high level and low level connections are made, it is desirable to keep the cabling separate to avoid introducing noise into the low level circuits. Either physical separation or shielding would be satisfactory.

2.4.2 LOW LEVEL CONNECTIONS - J6

The logic level output at pin 7 is a polar signal which alternates between ±10 volts (open circuit), and which provides at least a ±6 volt level when loaded with 1000 ohms to ground (pin 12). Mark is normally the negative level.

2.5 SELECTING OPERATING MODES

2.5.1 STEP AND BURST MODES

The step and burst circuits are controlled by an external signal applied between pin 8 or pin 11 and ground (pin 12) of connector J6. The required voltage for either circuit is +6 volts minimum. This voltage may be supplied externally from a neutral or polar logic level source, or, if desired, the positive Model 1306 power supply level may be switched by remote switch or relay contacts. The positive power supply level is available at pin 6 of J6. The step or burst pulse duration must be at least one millisecond.

If the step mode is selected, the burst circuit must be clamped on by connecting a jumper from pin 6 to pin 11 of J6. If the burst mode is selected, pins 6 and 8 must be jumpered. The

front panel MODE switch remains in the STEP position for both burst and step operation. Refer to details 1 and 2 for connector fabrication data.

2.5.2 POSITIVE OR NEGATIVE MARK LOW LEVEL OUTPUT

1. Remove Output Register board N0375A from Model 1306.
2. Locate - MARK + eyelets (adjacent to TP1).

NOTE

For a negative mark, perform step 3; for a positive mark, perform step 4.

3. Bend and insert a U-shaped jumper between center eyelet and - eyelet for negative mark (EIA) output.
4. Bend and insert a U-shaped jumper between center eyelet and + eyelet for positive mark output.
5. Solder eyelets selected in step 3 or 4 above and clip excess lead length.
6. Replace board N0375A in Model 1306.

2.5.3 1.5-UNIT STOP BIT

There are two methods of obtaining a 1.5-unit output stop bit: The first method requires wiring of low level connector J6; the second method requires wiring of Output Register board N0375A.

a. J6 Connector Wiring

1. Refer to details 1 and 2 for connector fabrication data.
2. Connect a jumper from pin 9 to pin 12.

b. Output Register Board Wiring

1. Remove register board N0375A from Model 1306.
2. Locate ½-UNIT STOP eyelets. Bend and insert a U-shaped jumper between eyelets.
3. Solder both eyelets and clip excess lead length.
4. Replace board N0375A in Model 1306.

2.6 OUTPUT RATE SELECTION

The Model 1306 is capable of operating at speeds up to 1300 baud. The different baud rates are obtained by means of miniature printed circuit boards (called speed chips) which plug into the time base board through the front panel of the unit. Each unit is shipped from the factory with two speed chips, one of which is prewired for a user-specified baud rate, and one which is left unwired for user's selection and completion. The unwired or universal speed chips may

be wired for any baud rate desired. When inserting a speed chip, make sure that the side marked TOP is facing upward.

The time base circuit consists of a 38.4 kHz crystal oscillator and a 10-stage binary counter. The binary counter divides the oscillator output. Thus, by sampling individual or combined counter stage outputs, any integral division from the basic oscillator frequency to 1/1024 of the frequency may be obtained.

The speed chips provide the means of setting a particular binary division rate. Factory-wired speed chips are available for all standard telegraph rates. (See table 2-1.) In the absence of a speed chip, the unit operates at 37.5 baud. With data rates for which there is no standard chip, a universal speed chip can be wired to provide any baud rate within the range of the equipment.

2.6.1 UNIVERSAL SPEED CHIP

An illustration of the universal speed chip is shown in figure 2-2. The speed chip has a system of hole-pairs numbered so that each represents a different binary division factor in the time base circuit. Hole-pair 1 and hole-pair 16 are identified in figure 2-2. Notice that the common track connects to one hole of each hole-pair. A particular binary division factor is selected by soldering a small U-shaped wire between the two holes of a numbered pair. For example, if a division factor of 86 is required, jumper wires are connected at hole-pairs 2, 4, 16, and 64.

The division factor related to a specific rate is found from the formula:

$$\text{Division Factor} = \frac{\text{Crystal Frequency in Hz}}{\text{Desired Baud Rate}} \times 1/2$$

Once the division factor is found, the proper hole-pairs to be wired can be determined. An example of this process is given for a baud rate of 200.

1. Determine division factor.

$$\text{Division Factor} = \frac{38{,}400 \text{ Hz}}{200 \text{ Baud}} \times 1/2 = 96$$

NOTE

Since the time base circuitry overall division ratio is necessarily even, any fractional result obtained from the formula must be reduced or increased slightly to produce a valid division factor.

Table 2-2. Factory Wired Speed Chips

Baud Rate	Part Number C1194-
45.5	1
50.0	2
56.9	3
74.2	4
75.0	5
110.0	6
135.0	7
150.0	8
300.0	9

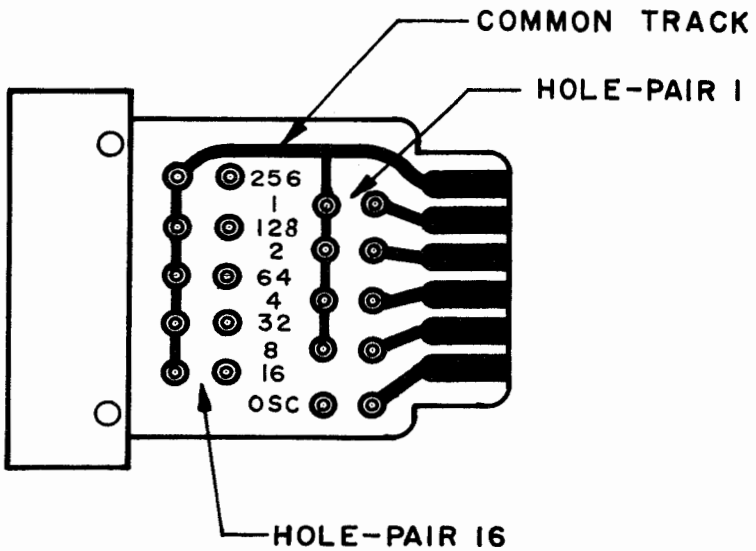


Figure 2-2. Universal Speed Chip Board (Bottom View)

2. Determine which binary counter stages to use.

   a. Select the next binary division factor which is less than 96. This factor (64) is part of the answer.
   b. Subtract 64 from 96. The result (32) is the remaining part of the answer. Therefore, the binary counter divide-by-64 and divide-by-32 outputs require speed chip jumpers for 200 baud operations.

2.7 MATRIX BOARD WIRING

Matrix characters are assigned to the board by inserting a type 1N4009 diode at the proper location for each mark bit of a character. A sufficient quantity of these diodes is supplied with each unit to allow the user to change characters. Consult the code chart in table 2-2 for the mark and space bits comprising a character. The matrix board has five character-bit diode positions and one reset jumper position for each character. (Refer to figure 2-3.) The reset jumper is inserted only at the end of the message, and care must be used to insure that only one jumper is installed per board. All wiring changes are confined to matrix board N0453.

2.7.1 INSERTING A NEW CHARACTER

1. Remove matrix board N0453 from Model 1306.
2. Determine position of new character in message sequence. Locate proper scan line. (Lines 1 through 80 correspond to characters 1 through 80.)
3. Unsolder and remove any existing diodes connected to scan line.
4. Refer to selected character in table 2-2 and determine which output bits are mark. The mark bit lines must have diodes inserted. For example, character C must have diodes inserted between selected scan line and bit lines 2, 3, and 4. (Refer to figure 2-3.)
5. Bend and insert diodes where indicated. Cathode end of diode (marked with black band) must be toward bit line eyelets.
6. Solder both ends of diodes and clip excess lead length.
7. This procedure completes the wiring of one new character. Repeat procedure for each additional new message character.
8. Replace matrix board N0453 in Model 1306.

2.7.2 INSERTING A RESET JUMPER

1. Remove matrix board N0453 from Model 1306.
2. Unsolder and remove existing reset jumper wire.
3. Determine position of last character in message sequence. (Lines 1 through 80 correspond to characters 1 through 80.)
4. Bend and insert an appropriate wire jumper between last character scan line and reset line.
5. Solder both ends of jumper and clip excess lead length.
6. Replace matrix board N0453 in Model 1306.

FIGURES	-	?	:	$	3	!	&	STOP	8	'	(	)	.	,	9	0	1	4	BELL	5	7	;	2	/	6	=	BLANK	LTRS	FIGS	SP	CR	LF
LETTERS	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z						
1	0	0		0	0	0				0	0						0		0		0		0	0	0	0		0	0			
2	0		0				0		0	0	0	0				0	0	0			0	0	0					0	0			0
3			0			0		0	0		0		0	0		0	0		0		0	0		0	0			0		0		
4		0	0	0		0	0			0	0		0	0	0			0				0		0				0	0		0	
5		0					0	0				0	0		0	0	0			0		0	0	0	0	0		0	0			

DOT INDICATES MARK BIT

Table 2-2. 5-Level Communications Code Chart

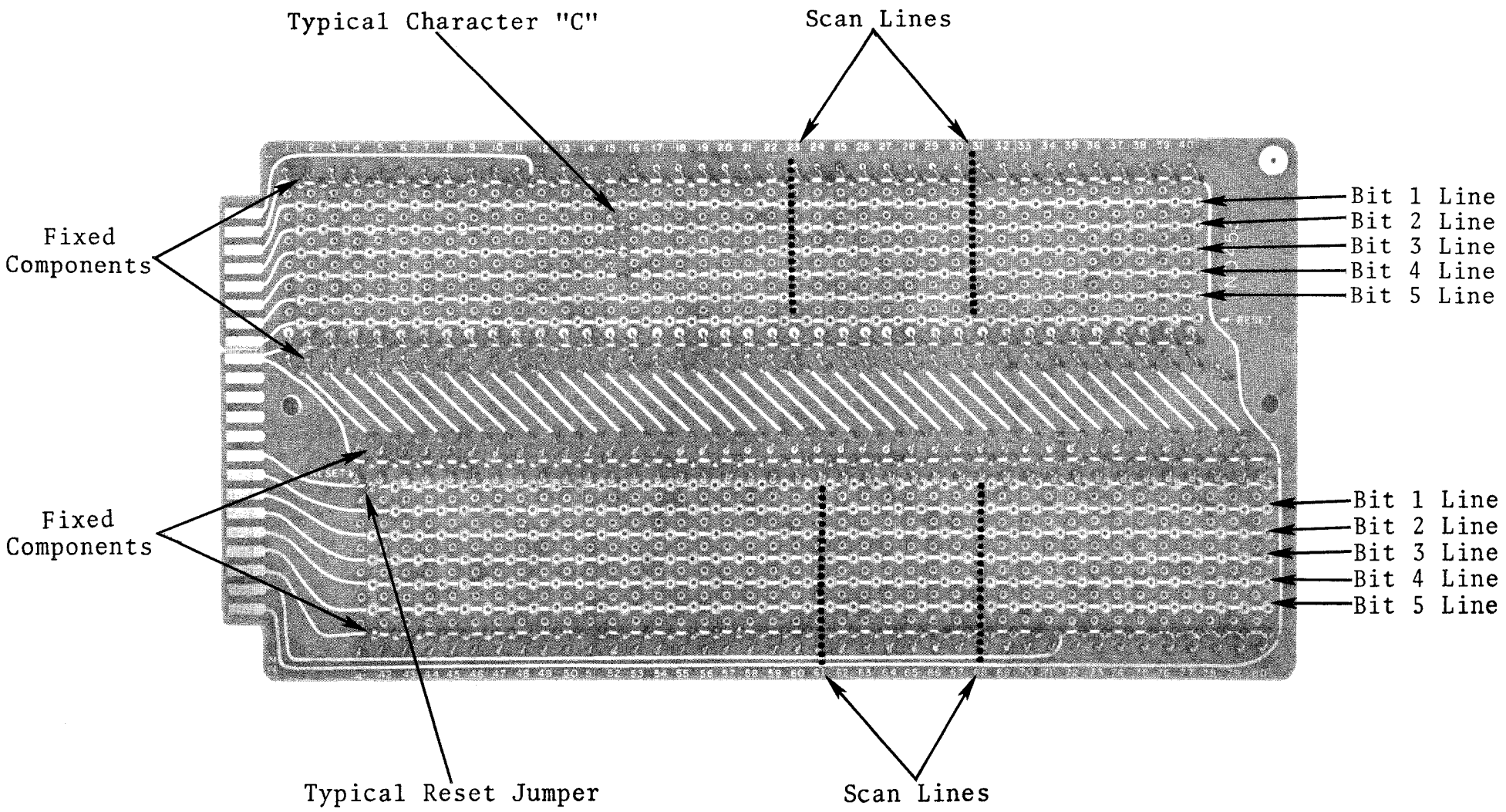


Figure 2-3. Component Side View of Matrix Board N0453

SECTION III

OPERATION

3.1 GENERAL

The Message Generator is ready for operation after installation is completed as described in section II of this manual. Table 3-1 lists the functions of all controls and indicators.

Table 3-1. Controls And Indicators, Model 1306

NAME	REFERENCE NUMBER	FUNCTION
POWER ON switch	S1	Controls a-c power to Message Generator
POWER ON lamp	DS2	Lights to indicate that a-c power is applied to equipment
SPEED slot		Accepts plug-in speed chips for desired output baud rates
OUTPUT MARK lamp	DS1	Indicates a mark output
MODE switch	S2	1) ⊓⊔: Provides reversals output, i.e., alternate mark and space 2) MARK: Provides steady mark output 3) STEP: Allows user to control character readout of Message Generator 4) RUN: Provides continuous programmed message output

3.2 OPERATION

1. Insert proper speed chip. (See paragraph 2.6 for chip wiring information.)
2. Set MODE switch to desired position.
3. Set POWER switch to ON position.

SECTION IV

THEORY OF OPERATION

4.1 FUNCTIONAL DESCRIPTION

A functional block diagram of the Model 1306 is shown in figure 4-1. For the purpose of discussion, assume that the MODE switch is in the STEP position and a step level is applied to the start-stop flip-flop via the step gate. In the set state, the start-stop flip-flop sets the parallel-to-serial register START flip-flop to space, sets the transfer flip-flop, and removes reset from the time base divider circuits. The latter action allows the time base to generate clock pulses at a baud rate determined by a front panel plug-in speed chip. The output clock pulses are applied to various circuits including the transfer flip-flop and the parallel-to-serial register.

The first clock transition resets the transfer flip-flop and thereby reads the first matrix character into the register. One-half bit time later the clock pulses begin shifting data out of the register. As the register releases the data to the output circuits, each flip-flop is successively set to the space state by a gate attached to the INDEX 2 flip-flop. When the index 1 level (stop bit) has advanced to the START flip-flop, the all space condition of the register is recognized by a sense empty gate and used to set a register empty flip-flop.

The register empty flip-flop enables the start-stop flip-flop reset gate, enables one input of the index AND gate, and disables the step gate. One-half bit time later the clock signal resets the start-stop flip-flop. This action advances the scanning circuits, enables the second input to the index AND gate, and clamps the register START flip-flop to the mark state. Notice that the time base continues operation due to the effect of the register empty flip-flop on the enable clamp. The index AND gate sets a mark into the INDEX 1 flip-flop and resets the stop flip-flop. The former action disables the sense empty gate which, in turn, opens both register empty flip-flop reset gates.

The 1-unit reset gate is normally used to reset the empty flip-flop one-half bit time after the start-stop flip-flop is reset. The 1-unit gate is disabled by inserting a jumper between the gate and ground. In this manner, the 1.5-unit gate and the stop flip-flop reset the empty flip-flop In operation, one bit time after reset of the start-stop flip-flop, the stop flip-flop is set by the clock signal. The resultant output from the stop flip-flop is coupled through the 1.5-unit gate and used to reset the empty flip-flop. The empty flip-flop then releases the time base enable clamp and allows the time base divider to reset The next step pulse input initiates a new sequence and reads the second matrix character from the unit.

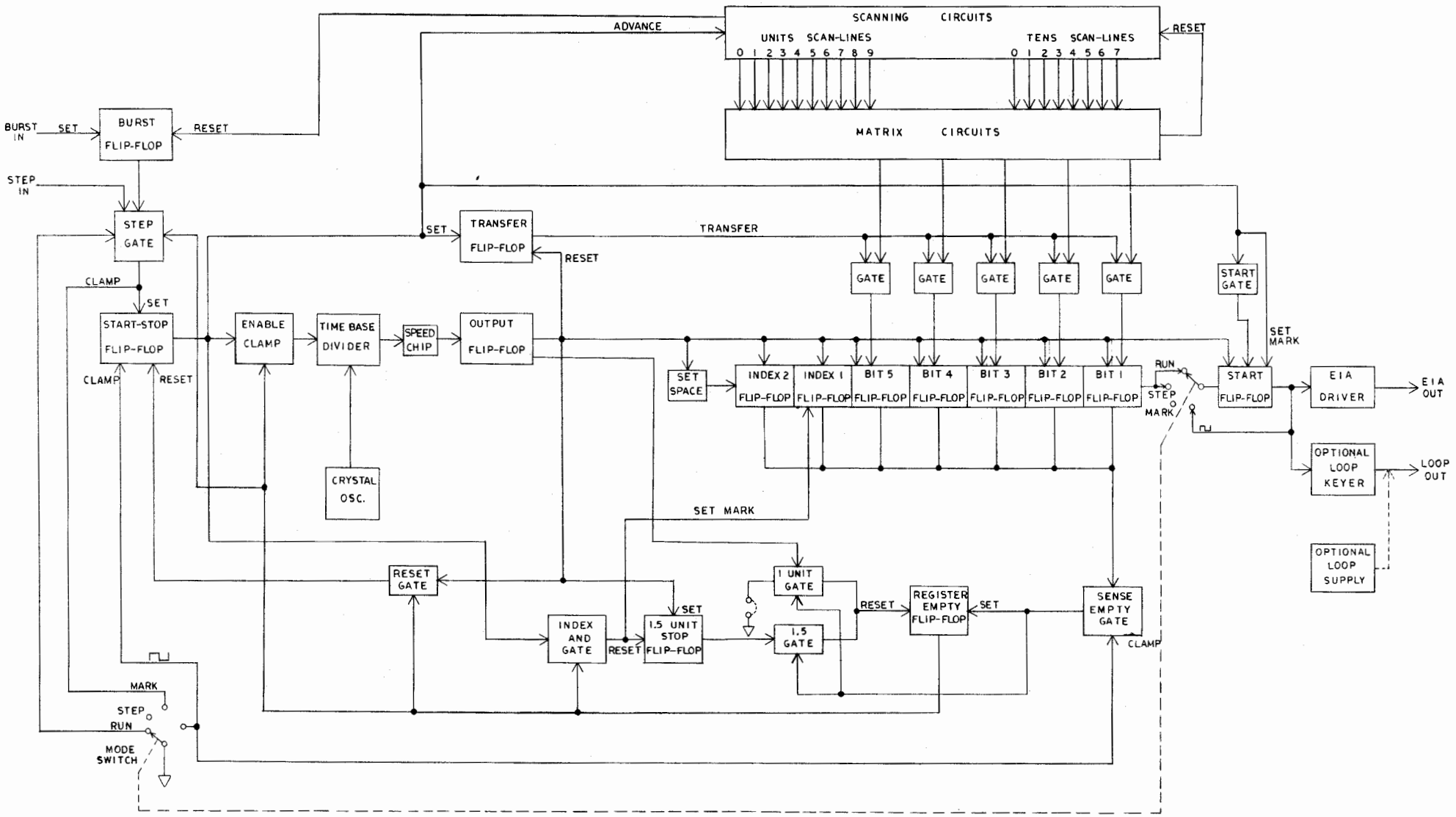


Figure 4-1. Block Diagram, Model 1306
(D1211)

In the RUN MODE a continuous level is supplied to the step gate and the matrix characters are continuously read from the unit. Burst mode operation is similar to the RUN mode operation with the exception that readout stops after one complete message sequence.

4.2 INTEGRATED CIRCUIT DISCUSSION

The Model 1306 character scan line decade counter circuits incorporate Motorola SN7490N Decade Counter and Texas Instruments SN7441N BCD-to-Decimal Decoder integrated circuit packages. Both packages are discussed in the following paragraphs.

4.2.1 SN7490N DECADE COUNTERS

The SN7490N Decade Counter (figure 4-2) consists of four, dual-rank, master-slave flip-flops connected together internally to provide a divide-by-two counter and a divide-by-five counter. Output 1 (pin 12) is from the divide-by-two counter; outputs 2,4, and 8 (pins 9, 8, and 11) are from the divide-by-five counter. Since the divide-by-two section is not internally connected to the divide-by-five section, the decade counter may be utilized in several different modes. For purposes of this discussion, however, only the BCD arrangement is applicable.

In order to connect the two sections for BCD counter operation, the BD (pin 1) input must be externally connected to the 1 output. The input count is then applied to the T input (pin 14), and the countdown sequence is as shown in the truth table of figure 4-2. Gated direct reset inputs are available for resetting all outputs to the logical zero state (R_0 at pins 2 and 3), or to the BCD count of 9 (R_9 at pins 6 and 7). These direct reset inputs override any count inputs applied to the counter.

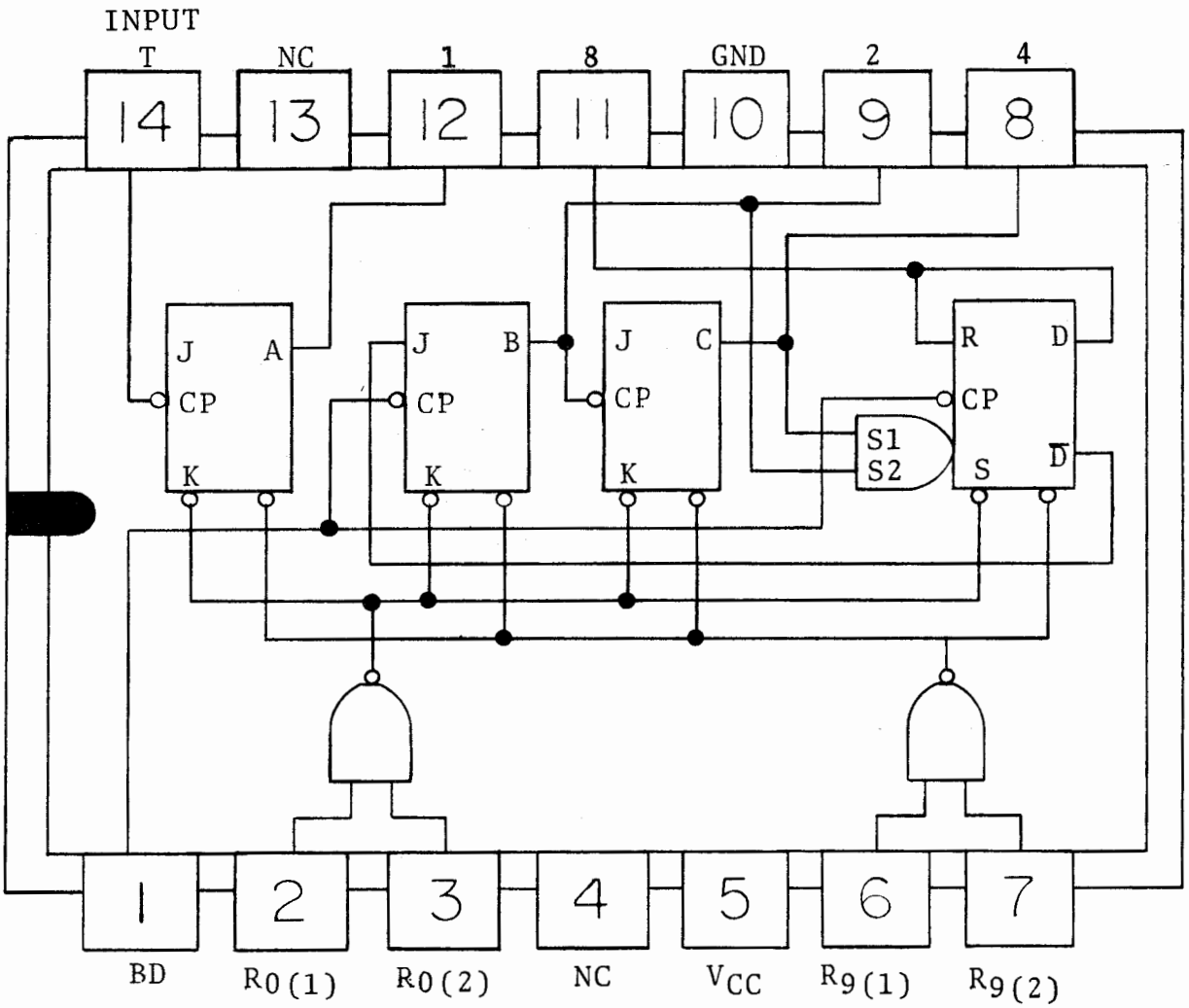
4.2.2 SN7441N BCD-TO-DECIMAL DECODER

The SN7441N Decoder consists of ten standard TTL (Transistor-Transistor Logic) gate circuits and ten output driver circuits. The BCD input connections are compatible with the SN7490N Decade Counter outputs. A truth table and logic symbol for the decoder are shown in figure 4-3.

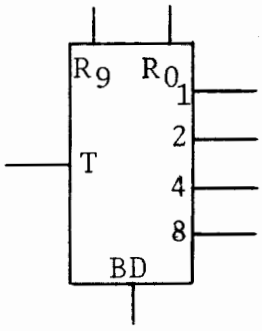
4.3 CIRCUIT DESCRIPTION

4.3.1 TIME BASE CIRCUITS

Refer to figure 5-1. The time base circuits consist of a crystal oscillator, a start-stop flip-flop, start-stop control circuits, and a divider and associated speed chip. Time base oscillator stages Q1 and Q2 form a series-resonant crystal oscillator which operates continuously at a 38.4 kHz rate. The oscillator signal at the emitter of Q2 is coupled to the base of Q3. The collector of Q3 drives amplifier Q7 which, in turn, drives the first stage



Logic Symbol

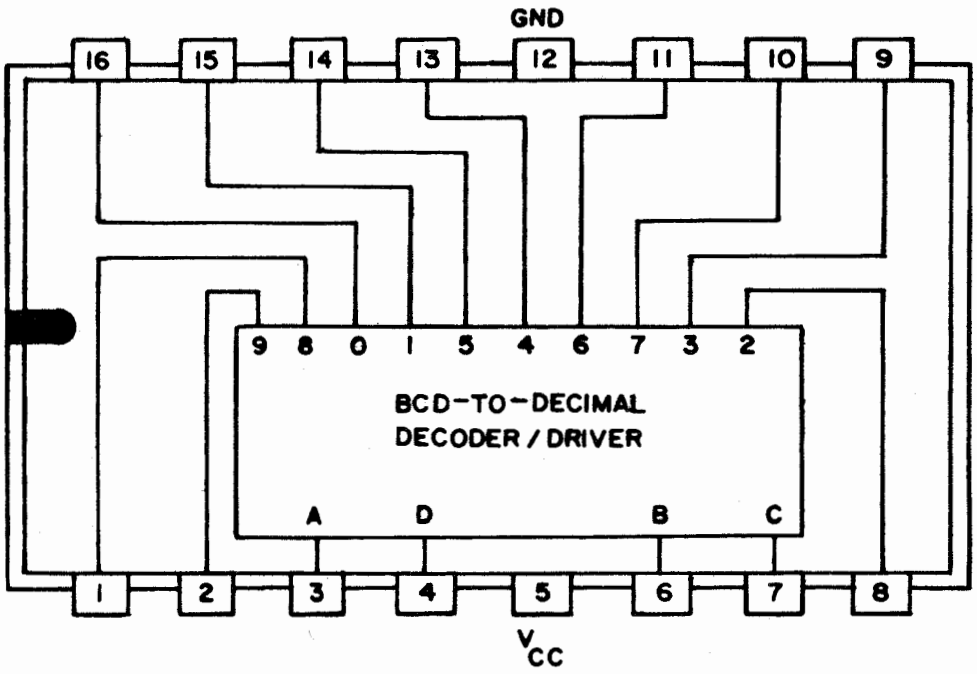


Logic Level 1 = +5V
Logic Level 0 = ground

Truth Table

INPUT	OUTPUT			
T	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Figure 4-2. SN7490N Decade Counter Logic



TRUTH TABLE

INPUT				OUTPUT ON ‡
D 8	C 4	B 2	A 1	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

‡ ALL OTHER OUTPUTS ARE OFF

Figure 4-3. SN7441N BCD-To-Decimal Decoder Logic

of the divider. Start-stop flip-flop Q33-Q34 controls operation of the divider circuits. The flip-flop is set in the STEP (includes step and burst operation) and RUN modes to the Q33 on-Q34 off state by a positive level at pin 6. In the reversals (⊓⊔) mode the flip-flop is clamped to the set state by a ground connected to the collector of Q33.

The collector of stage Q34 keeps the divider stages reset by controlling enable clamp Q29. (Q29 may also be controlled by a register empty level.) When the flip-flop is reset, Q29 is turned off and thus holds output flip-flop stage Q31 off. At the same time, Q29 holds on both trigger amplifier Q30 and reset clamp Q28. Turn-on of Q28 forces one-shot stage Q9 to turn off by grounding the junction of R59-R61. The resultant positive collector level of Q9 is connected to one emitter of each divider stage, thus forcing that stage to be turned off.

The divider stages consist of transistors Q10 through Q27. Collector levels of stages Q10, Q12, Q14, Q16, Q18, Q20, Q22, Q24 and Q26 can be sampled individually by a plug-in "speed chip." In this manner, a specific division factor can be obtained. In operation, when a given division factor is recognized, the plug-in speed-chip sets the one-shot through diodes CR30-CR31. The one-shot then resets the divider and drives the output flip-flop.

For purposes of discussion, assume that the speed chip selects a division factor of 128, and that the start-stop flip-flop has just been set. Each divider stage has been previously reset to the even-transistor-on and odd-transistor off state (Q10 on-Q11 off, etc.). Setting the start-stop flip-flop releases the reset level and allows the divider to count the oscillator frequency. When the speed chip is wired for a division factor of 128, the collector output of Q22 is connected to the input of reset one-shot Q8-Q9. When a count of 64 is reached, Q22 is turned off, CR23 is back-biased, and the base of Q8 is driven positive through R56, CR30, and CR31. This action sets the one-shot to the Q8 on-Q9 off state, and the positive collector level of Q9 resets the divider and turns on trigger amplifier Q30.

The zero-going output of Q30 drives output flip-flop Q31-Q32. This flip-flop divides the one-shot pulses by two, thereby producing a total crystal oscillator division factor of 128. Resetting the divider returns Q22 to the conducting state and thus removes the positive level from the base of Q8. One-shot Q8-Q9 relaxes after approximately one-half an oscillator cycle.

After six consecutive divider output flip-flop cycles, the parallel-to-serial register circuits remove the static set level from pin 6 and simultaneously enable (ground) the reset gate at pin 7 of the start-stop flip-flop. The reset gate clock input connects to pin E of the output flip-flop and the next zero-going transition (one-half clock time later) resets the start-stop flip-flip. Reset of

the start-stop flip-flop cannot immediately reset the divider circuits because clamp Q29 is held on by a register empty level. One-half clock time later (one clock time if 1.5-unit stop bit option is selected), the register empty flip-flop and divider circuits are reset. During the run mode, the divider circuits operate continuously because the start-stop flip-flop is set (by step level at pin 6) coincident with reset of the register empty flip-flop.

4.3.2 PARALLEL-TO-SERIAL SHIFT REGISTER

Refer to figure 5-2. The parallel-to-serial shift register consists of an eleven-stage register (only eight stages are used), a sense empty gate and associated register empty flip-flop, a transfer flip-flop, a stop bit flip-flop, an index AND gate, and a step circuit. Transistor circuits Q9 through Q18 form the 5 register stages which accept parallel data bits from the matrix circuits. Data is set into the register each time the transfer flip-flop is reset by the incoming clock signal.

Two index flip-flops (Q19-Q20 and Q21-Q22) are provided: index 1 (Q19-Q20) inserts the character stop bit and index 2 fills the register with spaces following readout. Start stage Q1-Q2, which is set by the start-stop flip-flop, inserts the character start pulse.

When the register is at rest, the transfer and register empty flip-flops are in the reset state and the stop bit flip-flop is in the set state. In addition, the shift register is set as follows: INDEX 2 is space, INDEX 1 is mark, the five data bit stages are space, and START is mark. In operation, when a positive step level is applied to pin 6 it is inverted by Q31 and used as one input to step gate Q36. The other gate input comes from the register empty flip-flop which is reset at this time. Thus, the gate applies a positive set level to the time base start-stop flip-flop.

In the set state, the start-stop flip-flop applies a ground level to the register at pin 9. This level sets the transfer flip-flop and inserts a space into the register start flip-flop. Normal operation of the time base also begins at this point. As a result, when the first clock transition appears at pin 13 (phase two), the transfer flip-flop is reset and matrix data is read into the register. One-half bit later, the clock signal reverses to a positive polarity and provides the first register shift pulse via shift gate Q24. This action shifts the first data bit into the START stage. Successive shift pulses move the data out of the register serially.

When the INDEX 1 bit (mark) has advanced to the START stage, the previous stages have been shifted to the space state. Sense empty gate Q23 recognizes this condition by turning off. The positive output of the sense empty gate sets register empty flip-flop Q27-Q28 to the Q27 on and Q28 off state. The empty flip-flop then performs the following functions: (1) disables step gate Q36 via emitter-follower Q26; (2) enables the start-stop flip-flop reset gate (through pin C), (3) enables one input of the index AND gate

(CR38); (4) disables the shift gate (Q24); (5) clamps time base clamp Q29 to the on state (through pin 8). One-half bit later, the start-stop flip-flop is reset. (Notice that enable clamp Q29 allows the time base divider to continue running even though the start-stop flip-flop is reset.)

Reset of the start-stop flip-flop clamps the START stage of the register to mark and enables the second index AND gate input (CR31). The index AND gate then sets INDEX 1 (stage Q19-Q20) to the mark state (Q19 off-Q20 on) and sets the stop bit flip-flop to the Q32 off-Q33 on state. Setting a mark into INDEX 1 causes the sense empty gate output to return to ground and thus enable the register empty flip-flop reset gates.

The register empty flip-flop is reset by one of two gates to provide either a 1 or a 1.5-unit stop level. Normal operation uses gate CR36-CR37, R123-R124-R125, and C34 to provide a 1-unit stop level. Since the 1-unit reset gate is connected to phase two of the clock signal, the empty flip-flop is reset one-half bit after reset of the start-stop flip-flop or 1 bit after recognition of an empty register. The 1-unit gate can be disabled to allow operation of the 1.5-unit gate by inserting a jumper from the junction of R124-R125 to ground. (See paragraph 2.5.3.)

The 1.5-unit reset gate involves the use of stop flip-flop Q32-Q33. The gate consists of C33-R116-CR35 and operates on set of the stop flip-flop. The latter flip-flop which is reset when the index AND gate is enabled, is set by the next zero-going clock transition at pin 13. At the end of a character readout, the register empty flip-flop is set. This action allows reset of the start-stop flip-flop following a one-half bit delay (clock at pin 13 is zero at this time). The two flip-flops enable the index AND gate and thus provide reset of the stop flip-flop. The latter flip-flop is then set on the next zero-going clock transition (1 bit later). Thus, the total stop bit time of the register is 1.5-units.

At this point, the register has completed a character readout sequence and rests in the conditions described initially. If the front panel MODE switch is in the RUN position, the register will begin a new cycle following reset of the register empty flip-flop. In the reversals mode (⌐¬), the input to the START stage of the register is disconnected from the preceding stage (pin 10) by the MODE switch. This input is then connected through the switch to its Q1 collector output (pin 21). Connected in this manner, the start flip-flop will alternately toggle between mark and space when driven by the clock signal. In order to provide a continuous clock signal, the MODE switch also clamps the start-stop flip-flop to start by grounding the collector of Q33. Sense empty gate Q23 is also grounded at pin W during this time to prevent the register empty flip-flop from blocking shift gate Q24. Placing the MODE switch in the MARK position disables the start-stop flip-flop set input and thereby disables all register operations.

The register serial output is connected through either a + MARK or a - MARK jumper and pin 22 to low level keyer input pin 3. In addition, pin 21 of the START flip-flop is connected directly to the optional high level keyer input.

The low level keyer consists of inverter Q37, driver Q40, and complementary emitter-follower Q38-Q39. A zero-level applied at pin 3 turns off Q37 and thereby removes forward bias from Q40. As Q40 turns off, the center of voltage divider R138-R139 swings negative. The negative level is conveyed to output pin 4 by emitter-follower Q39. A positive level at pin 3 turns on Q37 providing forward bias for Q40. This action drives the voltage divider positive and emitter-follower Q38 supplies the level to pin 4. The keyer output is connected to pin 7 of rear panel low level connector J6 and to the front panel OUTPUT MARK lamp driver circuit.

4.3.3 MATRIX SCANNING CIRCUITS

Refer to figure 5-3. The matrix scanning circuits consist of a units section and a tens section. Since both sections are basically similar in operation; only the units section is discussed. The units section consists of an SN7490N decade counter I.C. package, an SN7441N BCD-to-Decimal decoder I.C. package, and ten matrix driver stages. In operation, a drive level is applied to the decade counter T input each time the start-stop flip-flop is reset. Thus, each time a character is read from the register, the counter is advanced and a new matrix character is available to the register.

The decade counter output levels are applied to the BCD-to-Decimal decoder for subsequent conversion to decimal outputs. Each decimal (0 through 9) output level is inverted by an individual transistor stage (Q1 through Q10) before being connected to the matrix circuits. After each character is read from the register, the decade counter is advanced and the next decimal line is activated. This action reads the next consecutive character from the matrix. In addition, decimal line number 9 drives the tens decade counter input. As a result, the tens counter is advanced once every ten characters and each advancement activates a new section of the matrix.

The matrix has a reset line which can be wired to provide reset of the decade counters at any point from 1 through 80 characters. For example, the matrix reset could be wired to scan line 58, in which case the output message would be 58 characters in length. This reset line connects to pin 13 of the scanning circuit board; when activated, the line turns off Q36. The positive pulse from Q36 is applied to the zero reset inputs of both the units and tens decade counters. In addition, a reset output at pin 11 provides reset of the burst flip-flop. Reset stage Q36 has an additional input from startup preset clamp Q37 to provide reset of the two counters when a-c power is first applied to the unit.

4.3.4 MATRIX CIRCUITS

Refer to figure 5-4. The matrix circuits consist of a number of diode-resistor networks arranged in eight scan line groups. Each group consists of ten gates made up of two diodes and a resistor. One input of each gate is connected to a single tens decimal line. For example, diodes CR11 through CR20 all connect to decimal line 1 of the tens counter. The second input of each gate is connected to successive decimal line outputs of the units decade counter, i.e., 0 line to CR51, line 1 to CR52, line 2 to CR53, and so on through 9. The tens decade counter is advanced on the trailing edge of the ninth units decimal line. Wired in this manner, the first matrix group will read out characters 1 through 10 sequentially. The trailing edge of the ninth units decimal line advances the tens counter and the next gate group is activated. The units decimal lines now read out characters 11 through 20, and so on to a maximum of 80 characters.

Readout of a given character by a scan line gate is accomplished by connecting diodes between the gate output and any one of 5 bit lines. A diode connected between the gate and a bit line provides a mark output: no diode provides a space output.

The matrix bit line outputs are connected to a set of output driver circuits (located on board N0454, figure 5-3). The driver circuits consist of transistors Q11 through Q25. Each driver consists of three transistor stages. The first transistor stage is an emitter-follower which simultaneously drives two output stages. One output stage connects to rear panel output connector J6 while the other stage connects to the parallel-to-serial register input. For example, Q15 is the emitter-follower, Q14 drives the register, and Q16 drives J6.

4.3.5 STEP AND BURST CIRCUITS

Refer to figure 5-7. The step and burst circuits consist of a step inverter, a step gate, and a burst flip-flop. The step gate receives an input from both the step inverter and the burst flip-flop. Step inverter Q2 turns on when a positive step level is applied to rear panel connector J6-6. The resultant zero collector level allows step gate Q1 to turn off and thereby provide a step level to the output register step control circuits. The burst flip-flop set input (Q3) is clamped at this time and thus has no control over the step gate. A single character is read from the matrix each time a new step pulse is applied to the circuit.

During burst operation the step inverter is clamped on and thus permits the burst flip-flop (Q3-Q4) to control the gate. The burst flip-flop is set by a positive level from J6-11 and is reset by the scanning circuit decade counter reset level. In the set state, flip-flop stage Q3 is on and step gate Q1 is off, providing a step level to the shift register step control circuits. Each burst input reads a complete message sequence from the matrix circuits.

4.3.6 OPTIONAL HIGH LEVEL KEYERS

4.3.6.1 Isolated Polar Keyer. Refer to figure 5-5. The isolated polar keyer consists of a threshold detector, a gated RC oscillator, a space keyer, a mark keyer, and an isolated power supply.

A positive mark logic level input switches threshold detector circuit Q1 through Q4 to the Q1 off and Q4 on state. This action gates on RC oscillator Q5 through Q8. The oscillator output is approximately 50 kHz to coupling transformer T1. The T1 output to the mark channel causes Q9 and Q10 to switch on and off alternately at the 50 kHz rate. Capacitor C6 filters the output of Q9 and Q10 to provide a continuous zero level at the input to Q11. The space channel (Q13-Q14) functions the same as the mark with the exception that the output is driven positive rather than zero. Transistors Q11 and Q15 invert the two levels and respectively provide a positive signal to Q12 and a zero signal to Q16.

In the mark circuit, the positive output of Q11 turns on loop keyer Q12, thus allowing loop current to flow through the bridge circuit and Q12 to the common side of the loop. In the space circuit the opposite action occurs: Q16 is turned off, thereby preventing loop current flow.

The above conditions are reversed when the input is a space logic level. The space circuit will then pass loop current and the mark circuit output will be off.

The isolated power supply, consisting of T2, CR11 through CR16, and C1 through C3, operates from a 16-vac source and provides the keyer circuit with the proper operating voltages.

4.3.6.2 Isolated Neutral Keyer. Refer to figure 5-6. The isolated neutral keyer consists of gated RC oscillator Q1-Q2, coupling transformer T1, mark keyer circuit Q8 through Q11, and an isolated power supply. The oscillator is gated on when a positive mark level is applied to pin C of the keyer. The oscillator free-run frequency of approximately 65 kHz is coupled by transformer T1 to the mark keyer circuit.

The transformer-coupled oscillator signal is applied to the base of Q8, and Q8 follows this signal, turning on and off at the 65 kHz rate. The resultant collector output of Q8 is filtered by C10 and used as a static turn-off level for Q9. Turn-off of Q9 forward biases emitter-follower Q10, and Q10, in turn, forward biases loop keyer Q11. This latter stage then allows loop current to flow between the output terminals. When the input signal is a space, loop keyer stage Q11 turns off and thus inhibits current flow between the two terminals. Keyer Q11 is connected to the output terminals through diode bridge network CR13 through CR16. This arrangement insures that the proper polarity is always connected across Q11, regardless of the connected input polarity.

The isolated power supply consists of power transformer T2, diode rectifier CR11, and an RC filter circuit. The primary voltage of 16 vac is supplied to T2 by secondary windings of the Model 1306 power supply transformer.

4.3.7 POWER SUPPLIES

4.3.7.1 Low Level Power Supply. Refer to figure 5-7. The low level power supply components are mounted on power supply board N0489A. The supply consists of the following: 115/230 vac switch S3; transformer T1; full-wave diode bridge rectifier CR1 through CR4; positive and negative 12 vdc filter sections R1-C1 and R2-C2; full-wave rectifier CR5-CR6; and positive 5 vdc filter section R3-L8-C3.

4.3.7.2 Optional Loop Power Supply. Refer to figure 5-8. The optional loop power supply is constructed as a plug-in assembly that mounts on the Model 1306 main chassis. The supply consists of transformer T1, full-wave bridge rectifier CR1 through CR4, and filter network R1, C1, and R2. The supply will provide up to 100 ma at 130 vdc.

SECTION V

SCHEMATIC DIAGRAMS

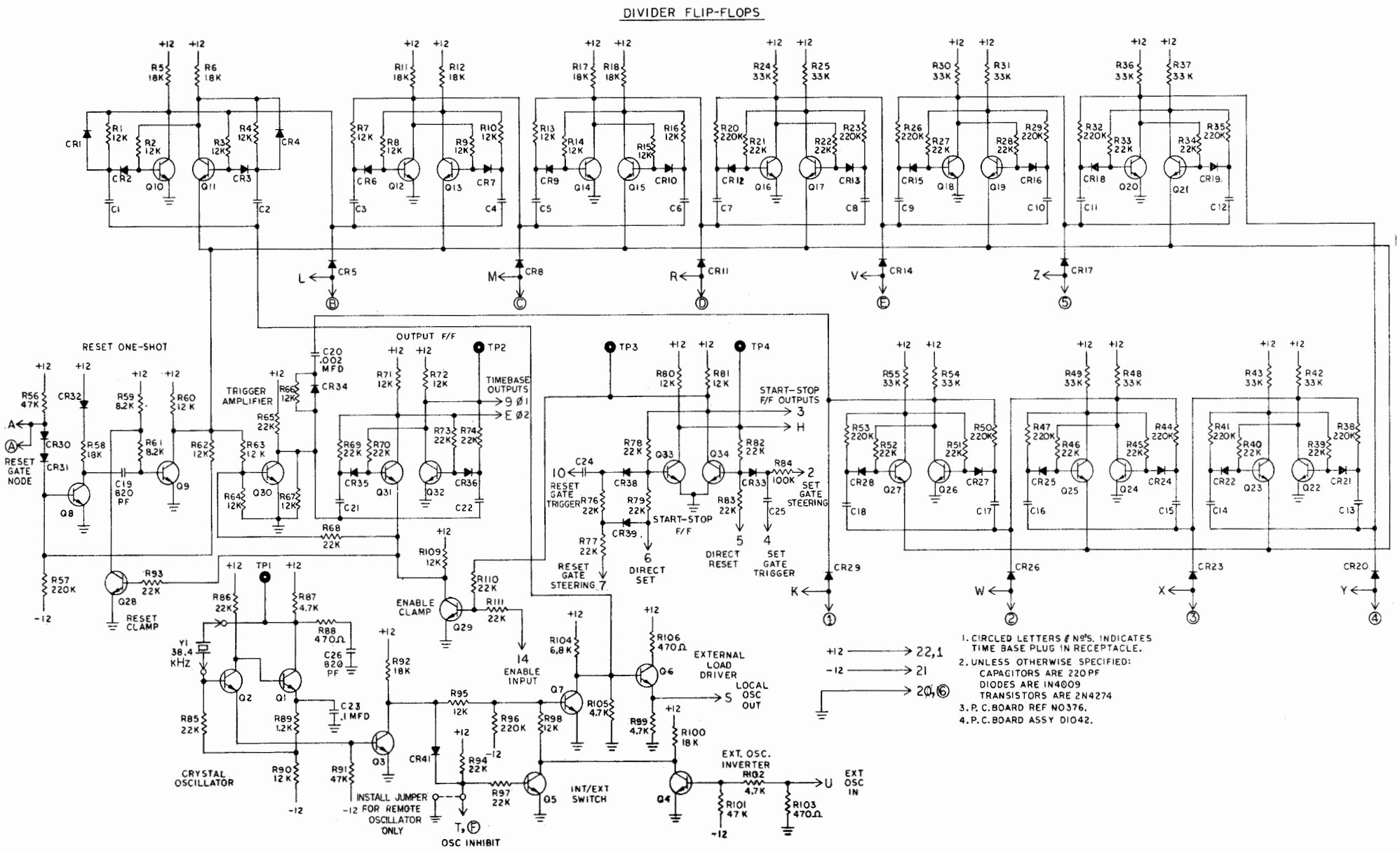


Figure 5-1. Schematic, Time Base Circuits (D1043A)

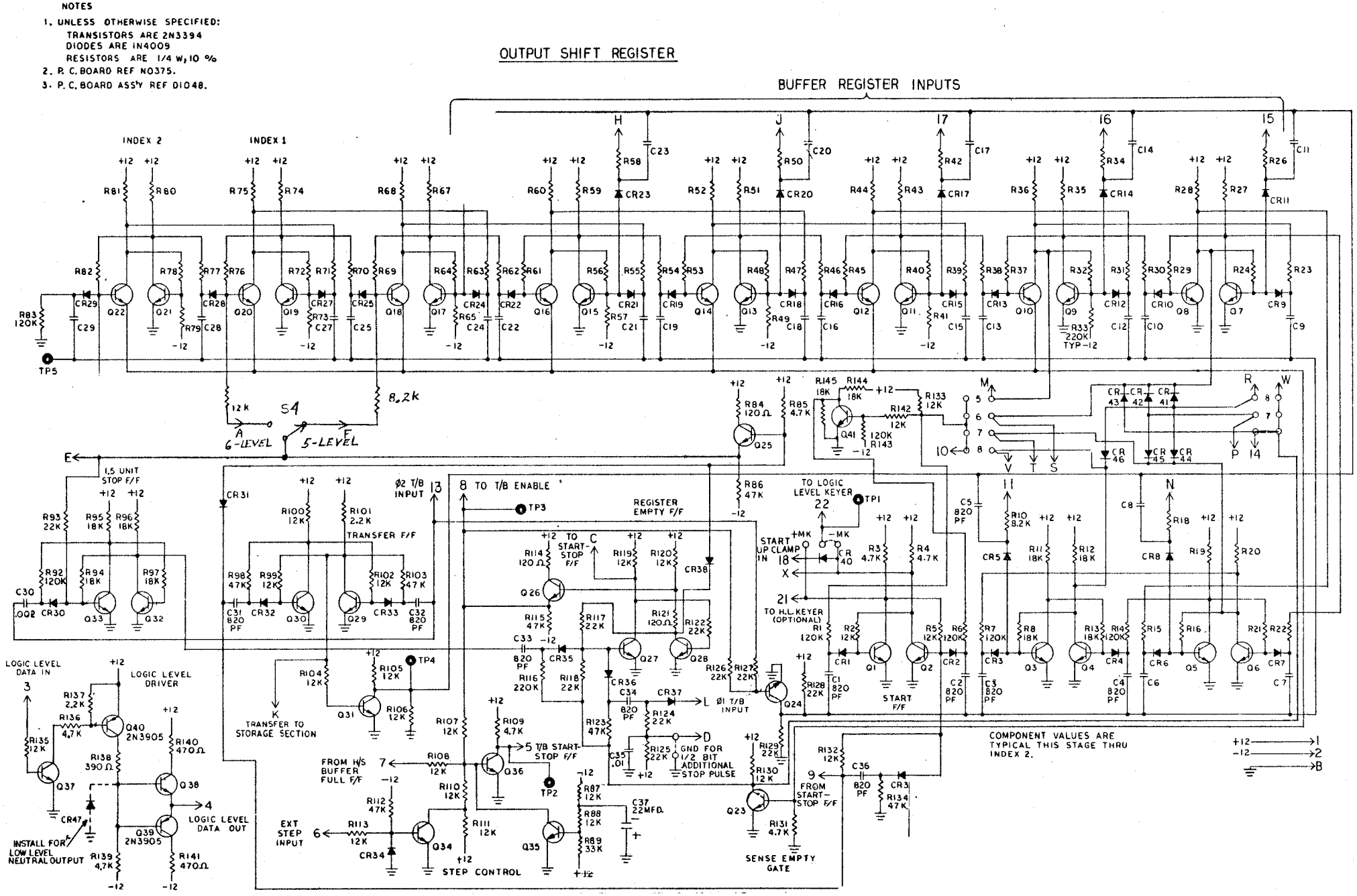


Figure 5-2. Schematic, Parallel-To-Serial Shift Register (JOB 3182)
(D1049A)

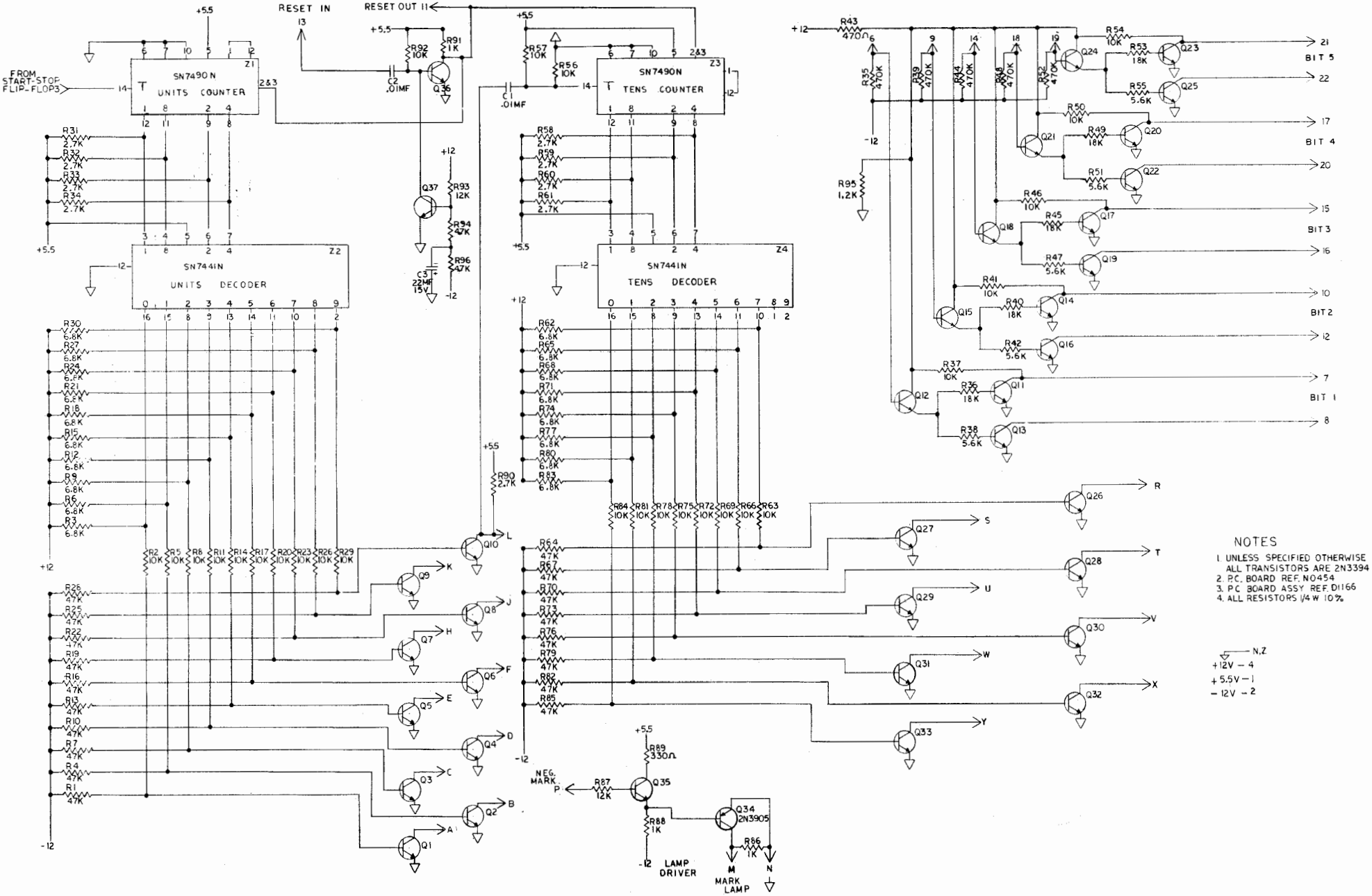


Figure 5-3. Schematic, Matrix Scanning Circuits (D1167B)

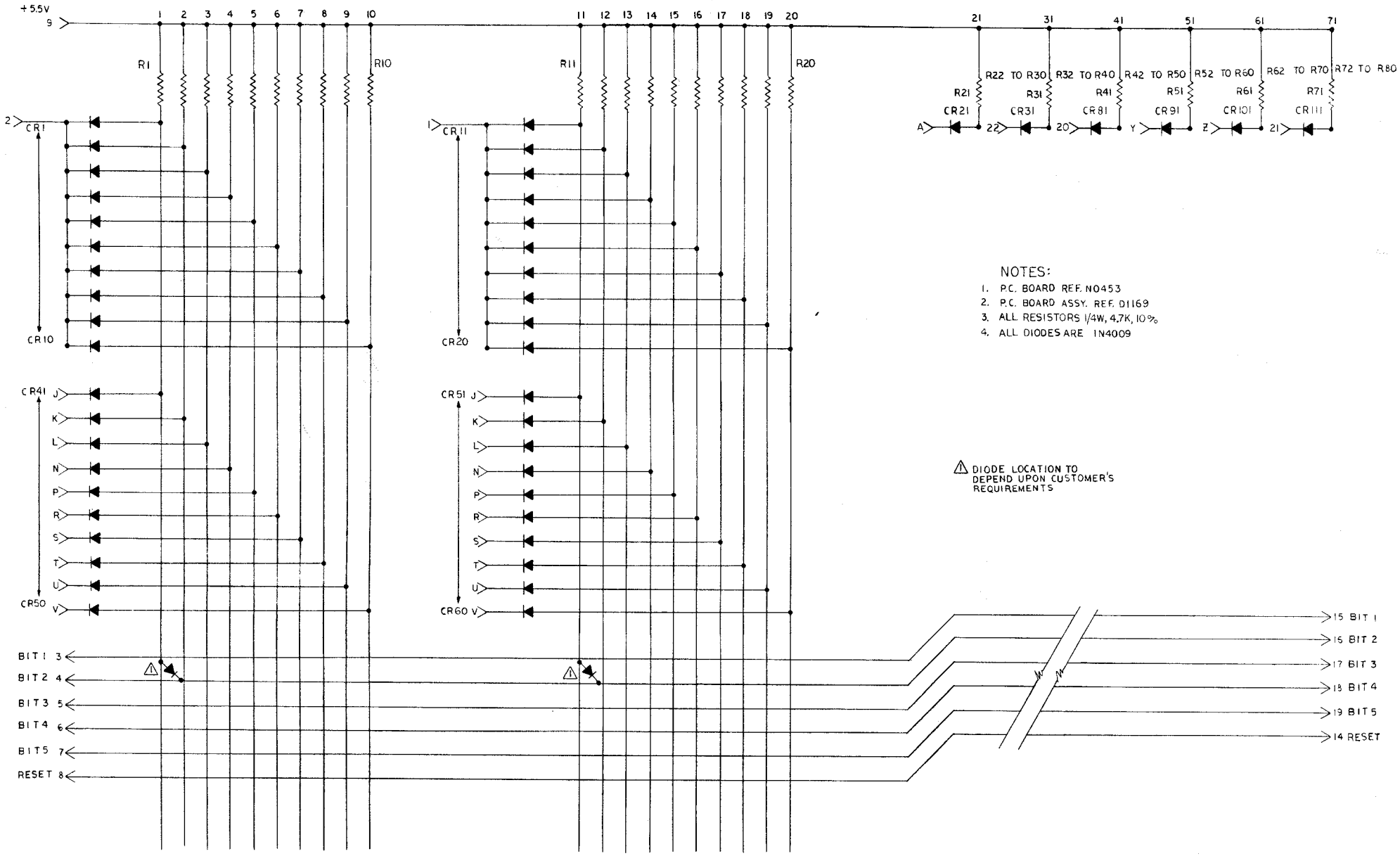
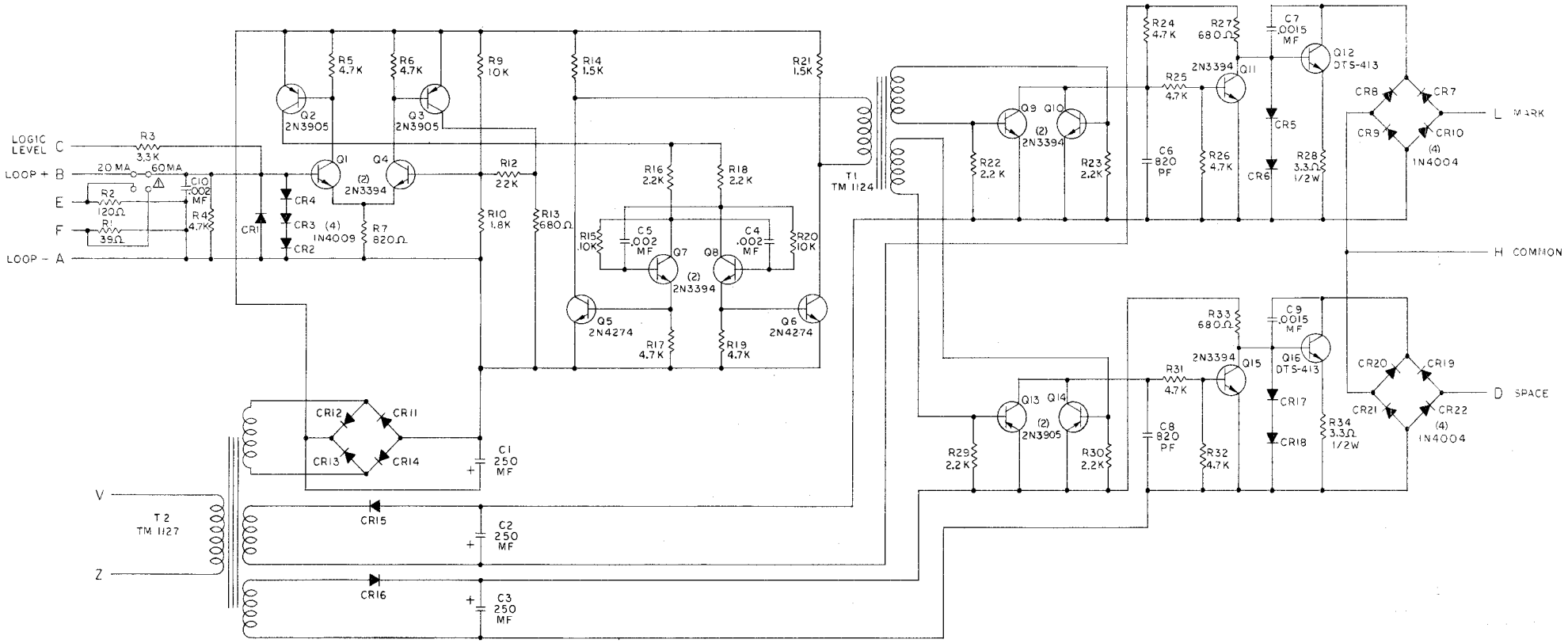
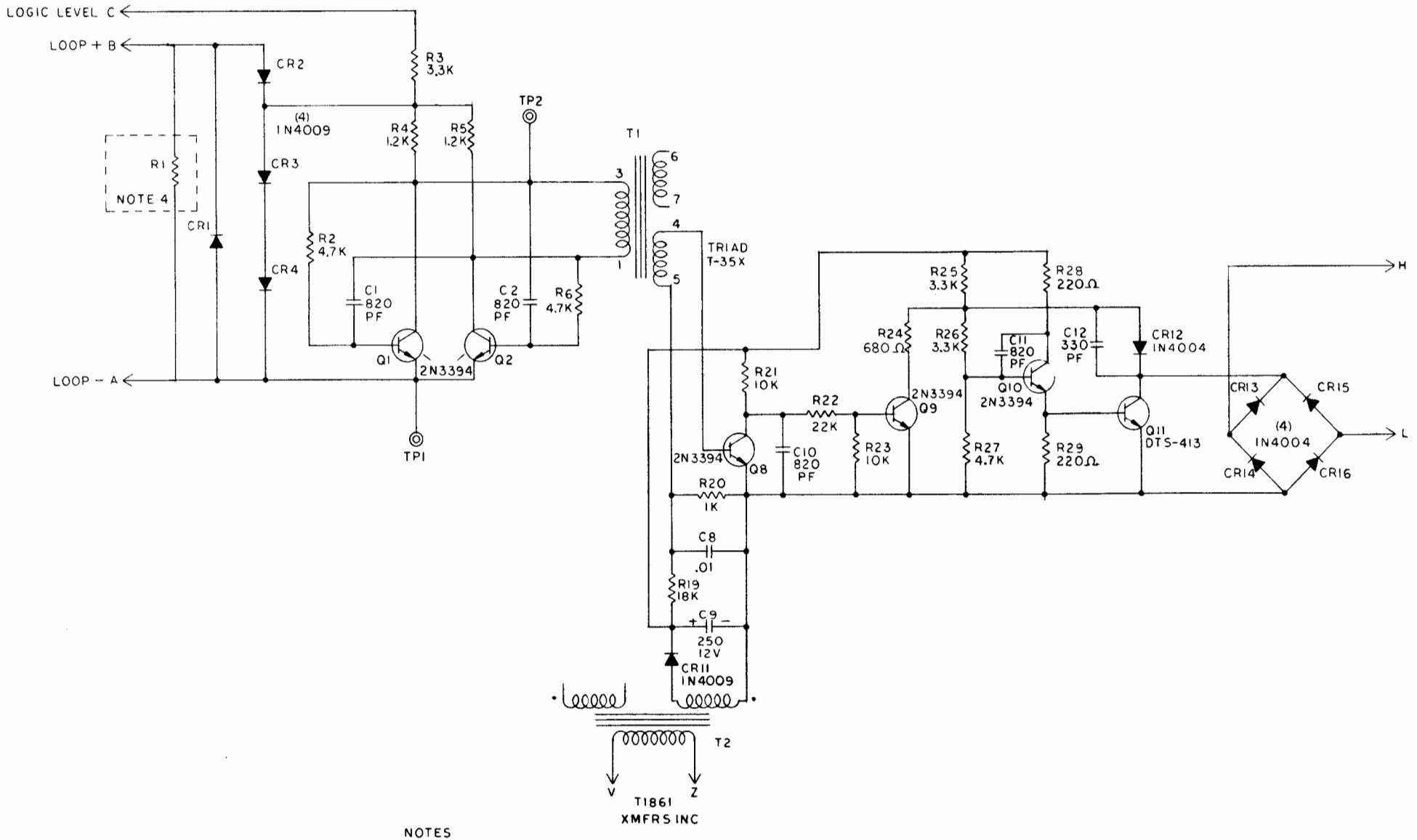


Figure 5-4. Schematic, Matrix Circuits (D1170A)



1. ADD JUMPER FOR 20MA OR 60MA OPERATION, ONLY WHEN NOT PROVIDED EXTERNALLY.
2. P. C. BOARD REF. NO327
3. P. C. BOARD ASS'Y D0822, SHEET 3
4. UNLESS OTHERWISE SPECIFIED
   DIODES ARE IN4002
   RESISTORS ARE 1/4W, 10 %

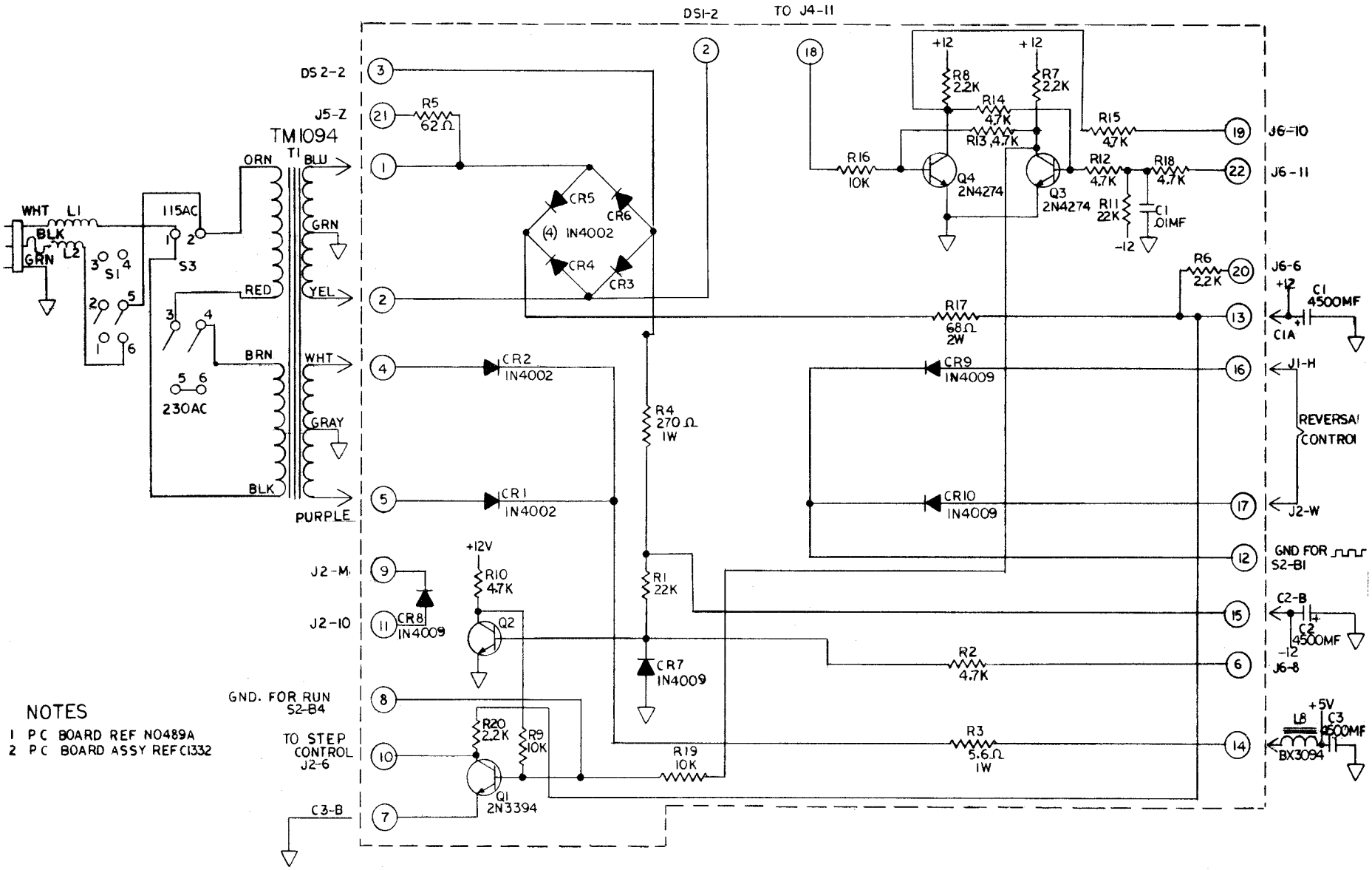
Figure 5-5. Schematic, Optional Isolated Polar Keyer (D0823I)



NOTES

1. CAPACITOR VALUES ARE MFD UNLESS OTHERWISE SPECIFIED.
2. P. C. BOARD REF NO464. JOB 2627 USED PC BOARD NO327A
3. P. C. BOARD ASS'Y REF D1110.
4. THIS RESISTOR IS A BIAS ADJUSTMENT AND IS INSTALLED ONLY WHEN THE LOOP HAS NO PROVISION FOR EXTERNAL ADJUSTMENT.

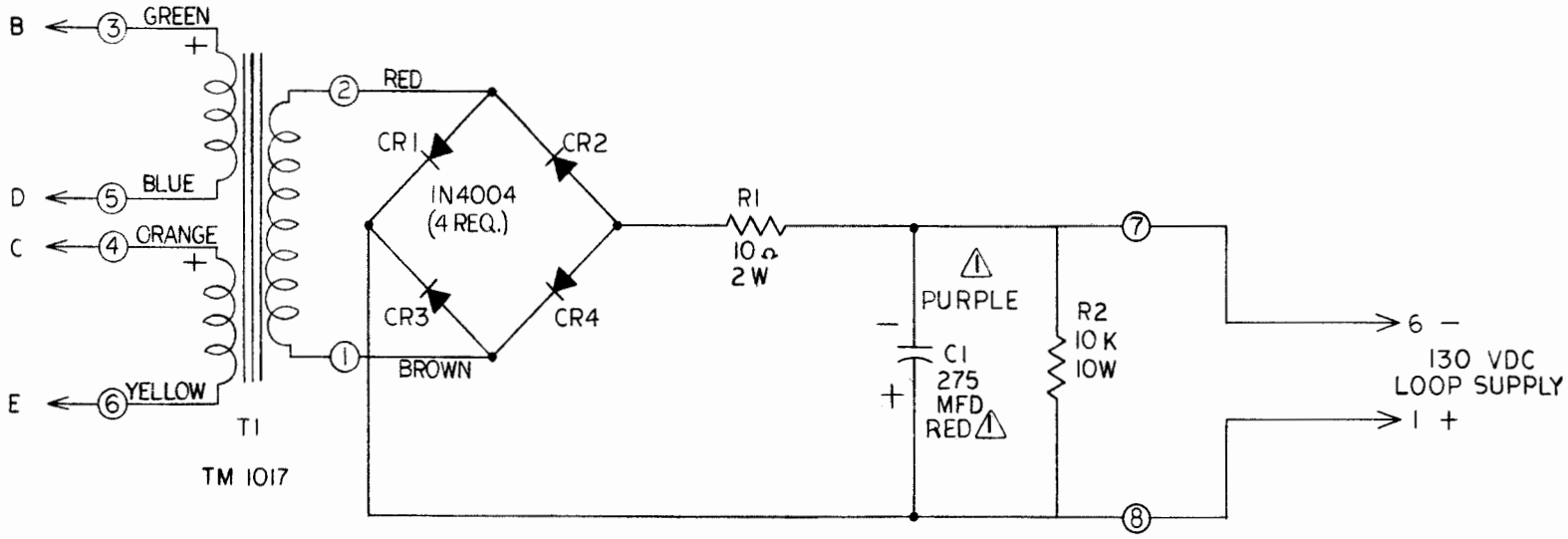
Figure 5-6. Schematic, Optional Isolated Neutral Keyer (D0823E)



NOTES

1 P C BOARD REF NO489A
2 P C BOARD ASSY REF C1332

Figure 5-7. Schematic, Low Level Power Supply (C1329A)



JUMPERS FOR 115VAC OR 230VAC OPERATION INSTALLED ON MATING ASSY.

⚠1 RED WIRE 4 IN. LONG.
PURPLE WIRE 3 1/4 IN. LONG.
BOTH WIRES 22GA, STRIP 1/4 IN BOTH ENDS TIN TIP ONE END.

Figure 5-8. Schematic, Optional Loop Power Supply (B1102A)

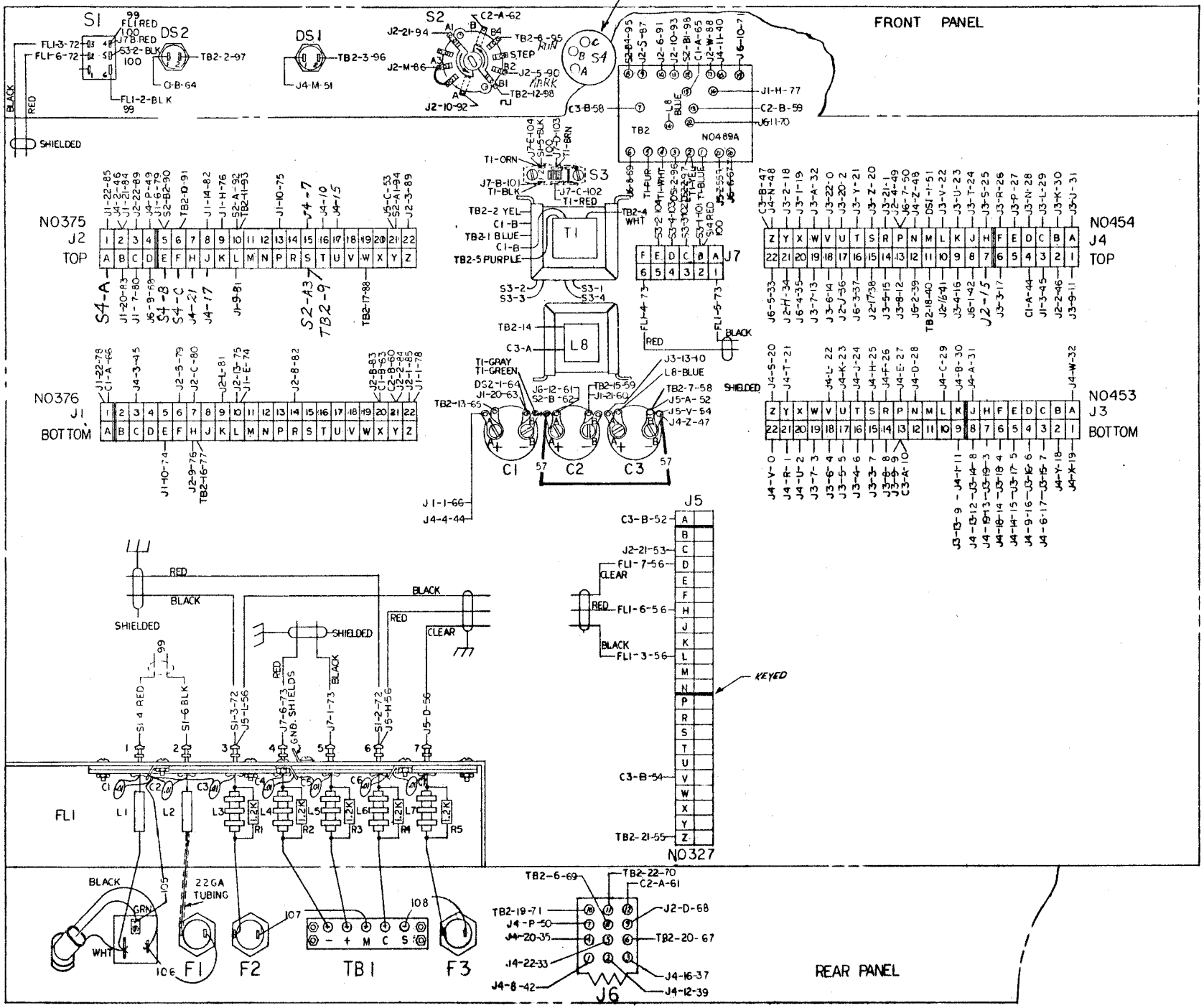


Figure 5-9. Wiring Diagram, Model 1306 (JOB 3182)
(D1149D)

SECTION VI

ASSEMBLY DRAWINGS

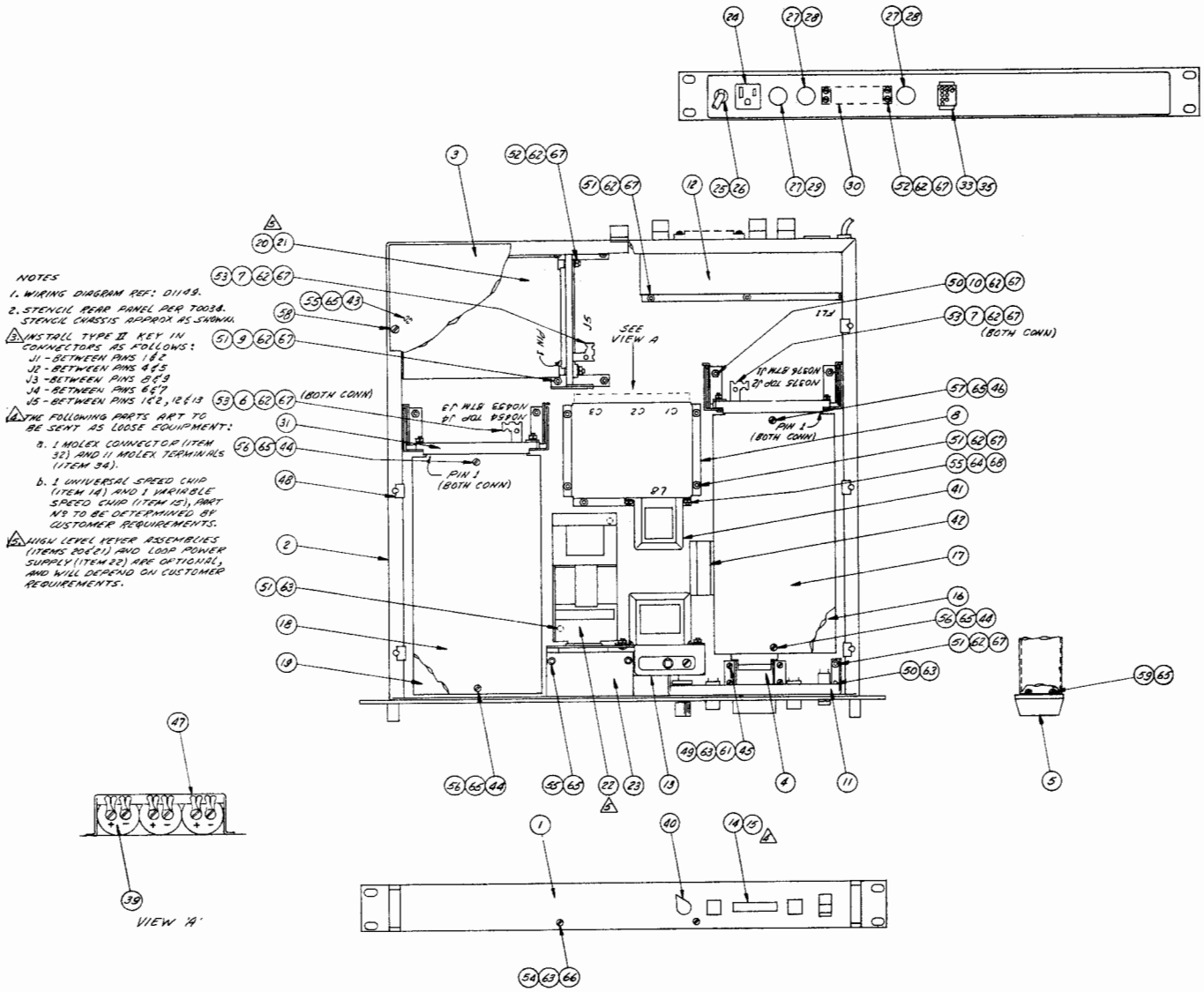
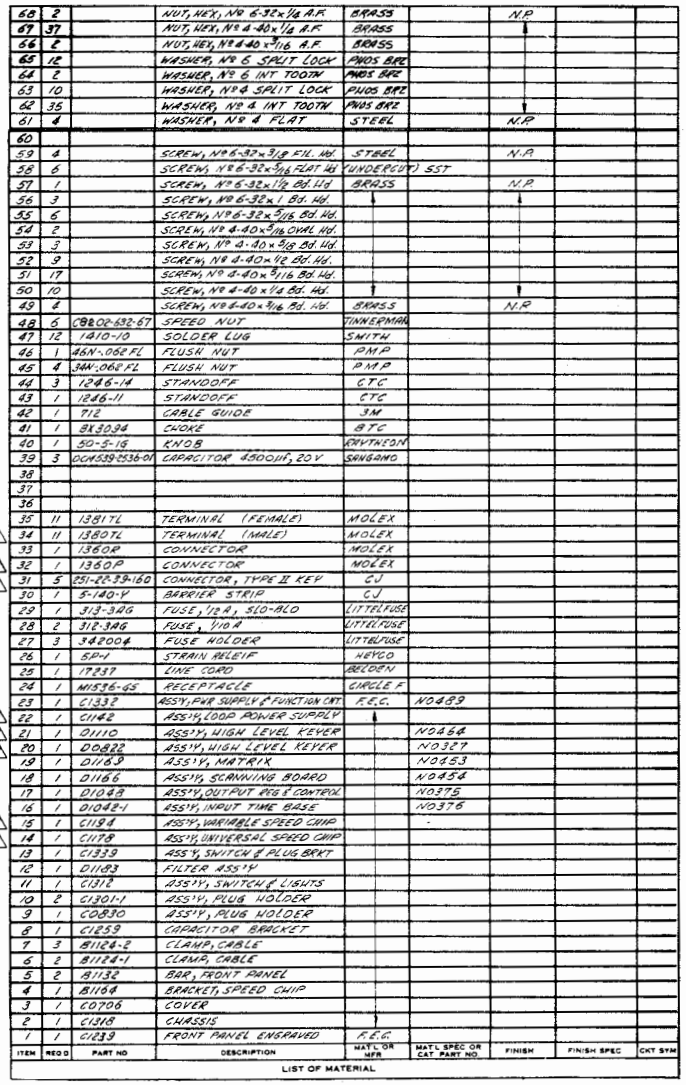


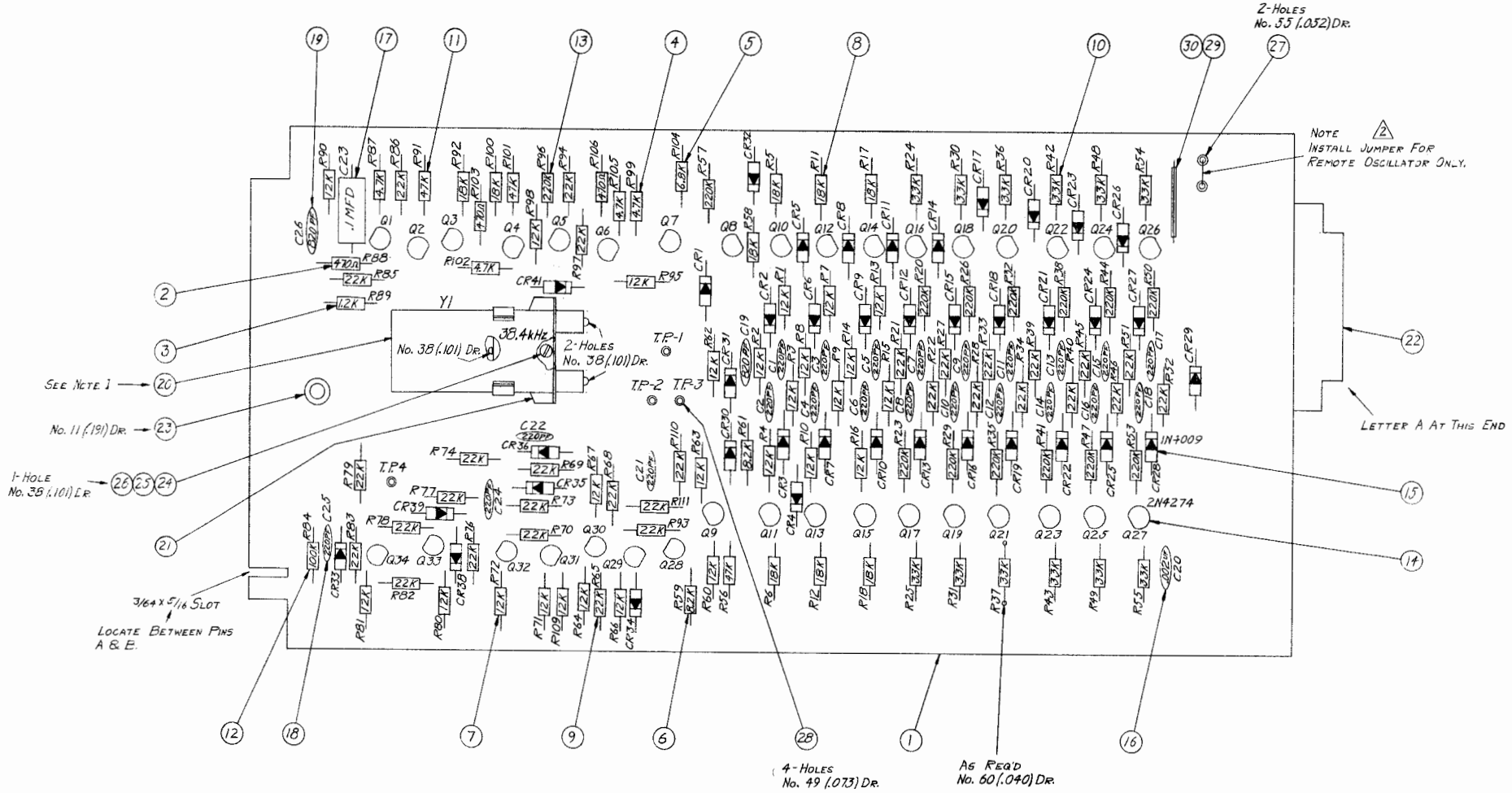
Figure 6-1. Assembly, Model 1306 (D1146A)



ITEM	REQ'D	PART NO	DESCRIPTION	MAT'L OR MFR.	MAT'L SPEC OR CAT. PART NO.	FINISH	FINISH SPEC	CKT SYM
68	2		NUT, HEX, NO 6-32 x 1/8 A.F.	BRASS		N.P.		
67	37		NUT, HEX, NO 4-40 x 1/8 A.F.	BRASS				
66	2		NUT, HEX, NO 4-40 x 3/16 A.F.	BRASS				
65	12		WASHER, NO 6 SPLIT LOCK	PHOS BRZ				
64	2		WASHER, NO 6 INT TOOTH	PHOS BRZ				
63	10		WASHER, NO 4 SPLIT LOCK	PHOS BRZ				
62	35		WASHER, NO 4 INT TOOTH	PHOS BRZ				
61	4		WASHER, NO 4 FLAT	STEEL		N.P.		
60								
59	4		SCREW, NO 6-32 x 3/8 F.H. MS.	STEEL		N.P.		
58	6		SCREW, NO 6-32 x 5/16 FLAT HD	(UNDERCUT) SST				
57	1		SCREW, NO 6-32 x 1/2 BD. HD	BRASS		N.P.		
56	3		SCREW, NO 6-32 x 1 BD. HD.					
55	6		SCREW, NO 6-32 x 5/16 BD. HD.					
54	2		SCREW, NO 4-40 x 5/16 OVAL HD.					
53	3		SCREW, NO 4-40 x 3/8 BD. HD.					
52	3		SCREW, NO 4-40 x 1/2 BD. HD.					
51	17		SCREW, NO 4-40 x 9/16 BD. HD.					
50	10		SCREW, NO 4-40 x 1/4 BD. HD.					
49	8		SCREW, NO 4-40 x 3/16 BD. HD.	BRASS		N.P.		
48	6	CBB02-632-67	SPEED NUT	TINNERMAN				
47	12	1810-10	SOLDER LUG	SMITH				
46	1	46N-062 FL	FLUSH NUT	PMP				
45	4	34N-062 FL	FLUSH NUT	PMP				
44	3	1286-14	STANDOFF	CTC				
43	1	1286-11	STANDOFF	CTC				
42	1	712	CABLE GUIDE	3M				
41	1	BK3034	CHOKE	BTC				
40	1	50-5-16	KNOB	CRYTHEON				
39	3	DCM539-2336-01	CAPACITOR 4500μF, 20 V.	SANGAMO				
38								
37								
36								
35	11	1381TL	TERMINAL (FEMALE)	MOLEX				
4 34	11	1380TL	TERMINAL (MALE)	MOLEX				
33	1	1360P	CONNECTOR	MOLEX				
4 32	1	1360P	CONNECTOR	MOLEX				
3 31	5	251-22-39-160	CONNECTOR, TYPE II KEY	CJ				
30	1	5-140-Y	BARRIER STRIP	CJ				
29	1	313-3AG	FUSE, 1/2 A, SLO-BLO	LITTELFUSE				
28	2	312-3AG	FUSE, 1/10 A	LITTELFUSE				
27	3	342004	FUSE HOLDER	LITTELFUSE				
26	1	SP-1	STRAIN RELEIF	HEYCO				
25	1	17237	LINE CORD	BELDEN				
24	1	MIS36-GS	RECEPTACLE	CIRCLE F				
23	1	C1332	ASSY, PWR SUPPLY & FUNCTION UNT.	F.E.C.	N0489			
5 22	1	C1142	ASS'Y, LOOP POWER SUPPLY					
5 21	1	D1110	ASS'Y, HIGH LEVEL KEYER		N0454			
5 20	1	D0822	ASS'Y, HIGH LEVEL KEYER		N0327			
19	1	D1169	ASS'Y, MATRIX		N0453			
18	1	D1166	ASS'Y, SCANNING BOARD		N0454			
17	1	D1048	ASS'Y, OUTPUT REG & CONTROL		N0375			
16	1	D1048-1	ASS'Y, INPUT TIME BASE		N0376			
4 15	1	C1194	ASS'Y, VARIABLE SPEED CHIP					
4 14	1	C1178	ASS'Y, UNIVERSAL SPEED CHIP					
13	1	C1333	ASS'Y, SWITCH & PLUG BRKT					
12	1	D1183	FILTER ASS'Y					
11	1	C1312	ASS'Y, SWITCH & LIGHTS					
10	2	C1301-1	ASS'Y, PLUG HOLDER					
9	1	C0830	ASS'Y, PLUG HOLDER					
8	1	C1259	CAPACITOR BRACKET					
7	3	B1124-2	CLAMP, CABLE					
6	2	B1124-1	CLAMP, CABLE					
5	2	B1132	BAR, FRONT PANEL					
4	1	B1164	BRACKET, SPEED CHIP					
3	1	C0706	COVER					
2	1	C1318	CHASSIS					
1	1	C1239	FRONT PANEL ENGRAVED	F.E.C.				

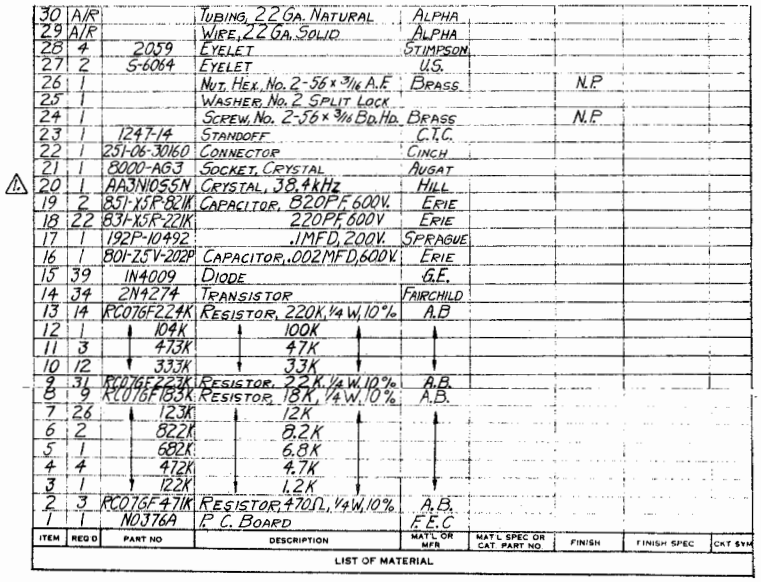
LIST OF MATERIAL

Figure 6-1. Parts List
(D1146A)



NOTE
1. INPUT TIME BASE BOARD, PART NO. D1042-1 WILL HAVE 38.4 kHz CRYSTAL INSTALLED.
2. OUTPUT TIME BASE BOARD, PART NO. D1042-2 WILL HAVE JUMPER INSTALLED AS PER NOTE, IN LIEU OF CRYSTAL, (ITEM 20).
3. SCH. REF. D1043

Figure 6-2. P.C. Board Assembly, Time Base Circuits (D1042)



ITEM	REQ'D	PART NO	DESCRIPTION	MAT'L OR MFR	MAT'L SPEC OR CAT. PART NO.	FINISH	FINISH SPEC	CKT SYM
30	A/R		TUBING, 22 GA. NATURAL	ALPHA				
29	A/R		WIRE, 22 GA. SOLID	ALPHA				
28	4	2059	EYELET	STIMPSON				
27	2	5-6064	EYELET	U.S.				
26	1		NUT, HEX, NO. 2-56 x 3/16 A.F.	BRASS		N.P.		
25	1		WASHER, NO. 2 SPLIT LOCK					
24	1		SCREW, NO. 2-56 x 3/16 BD. HD.	BRASS		N.P.		
23	1	1247-14	STANDOFF	C.T.C.				
22	1	251-06-30160	CONNECTOR	CINCH				
21	1	8000-AG3	SOCKET, CRYSTAL	AUGAT				
⚠1 20	1	AA3N1055N	CRYSTAL, 38.4kHz	HILL				
19	2	851-X5F-821K	CAPACITOR, 820PF 600V.	ERIE				
18	22	831-X5F-221K	220PF, 600V	ERIE				
17	1	192P-10492	.1MFD, 200V.	SPRAGUE				
16	1	801-Z5V-202P	CAPACITOR, .002MFD, 600V.	ERIE				
15	39	1N4009	DIODE	G.E.				
14	34	2N4274	TRANSISTOR	FAIRCHILD				
13	14	RC07GF224K	RESISTOR, 220K, 1/4 W, 10%	A.B.				
12	1	104K	100K					
11	3	473K	47K					
10	12	333K	33K					
9	31	RC07GF223K	RESISTOR, 22K 1/4 W, 10%	A.B.				
8	9	RC07GF183K	RESISTOR, 18K, 1/4 W, 10%	A.B.				
7	26	123K	12K					
6	2	822K	8.2K					
5	1	682K	6.8K					
4	4	472K	4.7K					
3	1	122K	1.2K					
2	3	RC07GF471K	RESISTOR, 470Ω, 1/4 W, 10%	A.B.				
1	1	N0376A	P. C. BOARD	F.E.C.				

LIST OF MATERIAL

Figure 6-2. Parts List
(D1042)

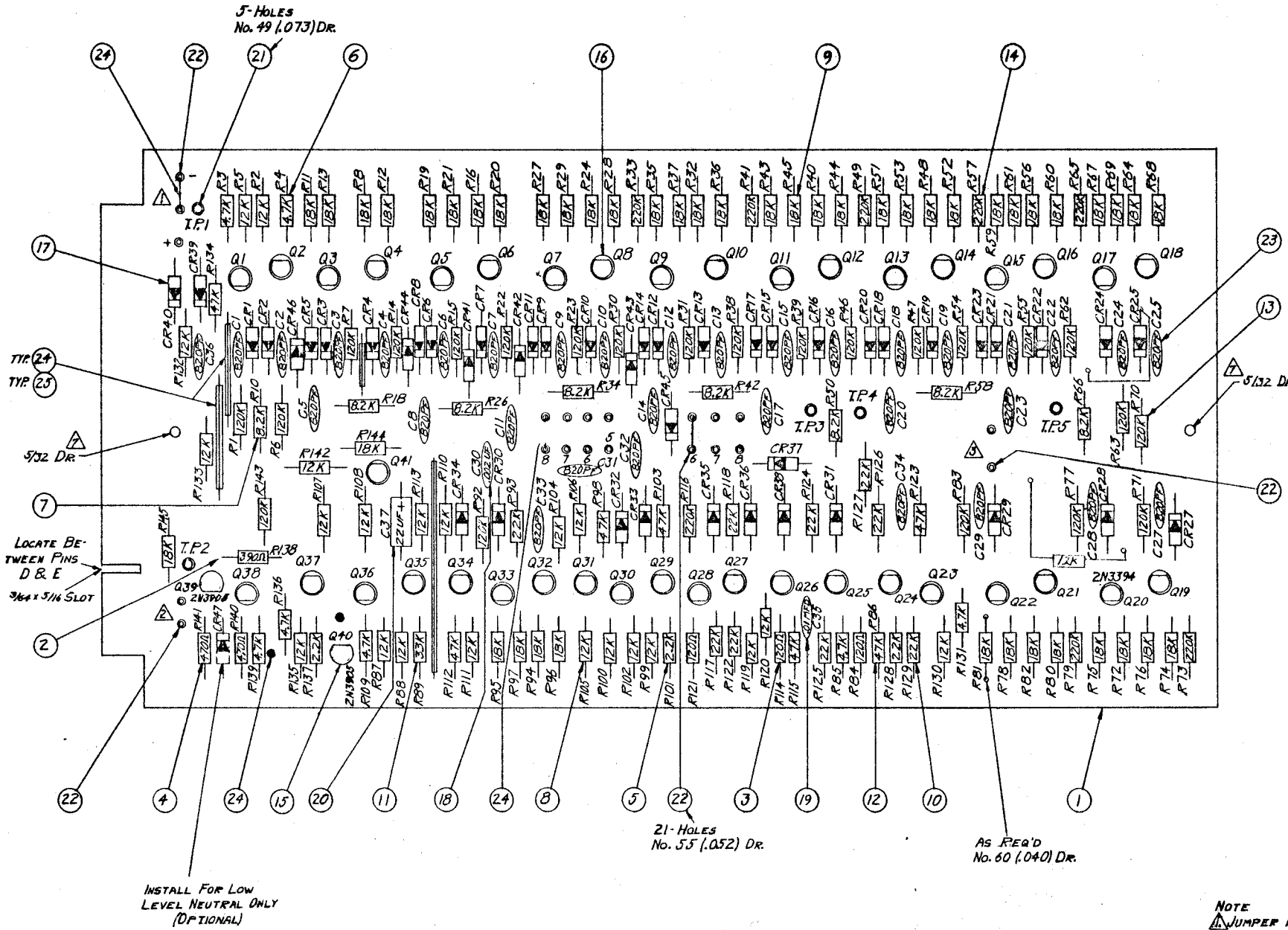
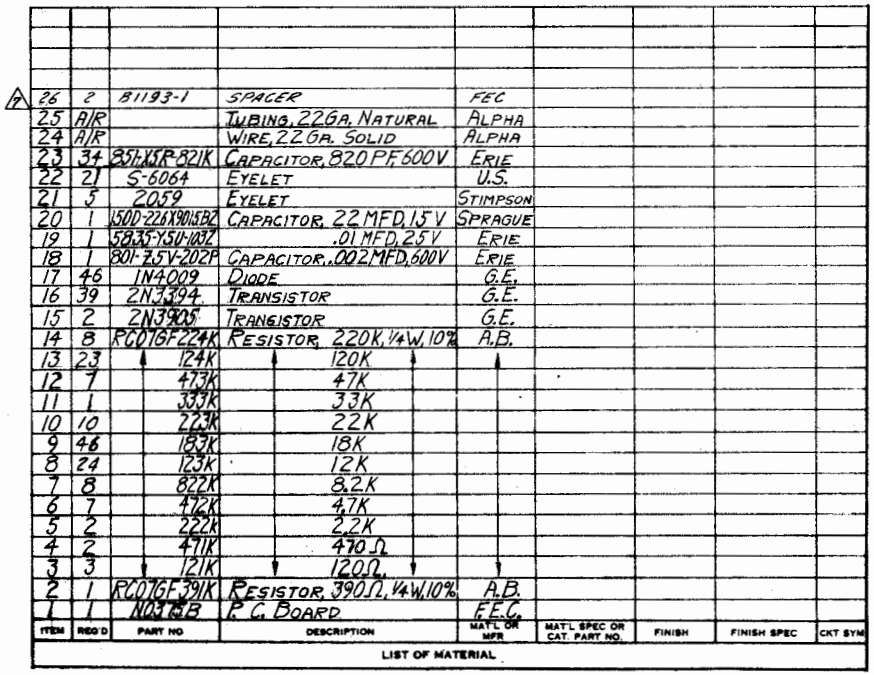


Figure 6-3. P.C. Board Assembly, Parallel-To-Serial Shift Register (JOB 3182)
(D1048A)

NOTE
1. JUMPER FOR EITHER MINUS OR PLUS MARK.
2. ADD JUMPER FOR ADDITIONAL 1/2 UNIT STOP.
3. ADD JUMPER FOR ADDITIONAL ONE UNIT STOP.
4. JUMPER FOR CODE LEVEL
5. ABOVE JUMPERS TO BE 1/4 IN HEIGHT
6. SCHEMATIC REF D1049
7. DRILL HOLES NO 11 (.191) DR AND INSTALL 2 SPACERS B1193-1 (ITEM 26) ON COMPONENT SIDE OF BOARD WHEN ASS'Y IS USED IN MODE



ITEM	REQ'D	PART NO	DESCRIPTION	MAT'L OR MFR	MAT'L SPEC OR CAT. PART NO.	FINISH	FINISH SPEC	CKT SYM
A 26	2	B1193-1	SPACER	FEC				
25	A/R		TUBING, 22GA. NATURAL	ALPHA				
24	A/R		WIRE, 22 GA. SOLID	ALPHA				
23	34	851-X5R-821K	CAPACITOR, 820 PF, 600V	ERIE				
22	21	S-6064	EYELET	U.S.				
21	5	2059	EYELET	STIMPSON				
20	1	150D-226X9015B2	CAPACITOR, 22 MFD, 15 V	SPRAGUE				
19	1	5835-Y5U-103Z	.01 MFD, 25 V	ERIE				
18	1	801-Z5V-202P	CAPACITOR, .002 MFD, 600V	ERIE				
17	46	1N4009	DIODE	G.E.				
16	39	2N3394	TRANSISTOR	G.E.				
15	2	2N3905	TRANSISTOR	G.E.				
14	8	RC07GF224K	RESISTOR, 220K, 1/4W, 10%	A.B.				
13	23	124K	120K					
12	7	473K	47K					
11	1	333K	33K					
10	10	223K	22K					
9	46	183K	18K					
8	24	123K	12K					
7	8	822K	8.2K					
6	7	472K	4.7K					
5	2	222K	2.2K					
4	2	471K	470 Ω					
3	3	121K	120 Ω					
2	1	RC07GF391K	RESISTOR, 390 Ω, 1/4W, 10%	A.B.				
1	1	N03-B	P. C. BOARD	F.E.C.				

LIST OF MATERIAL

Figure 6-3. Parts List
(D1048A)

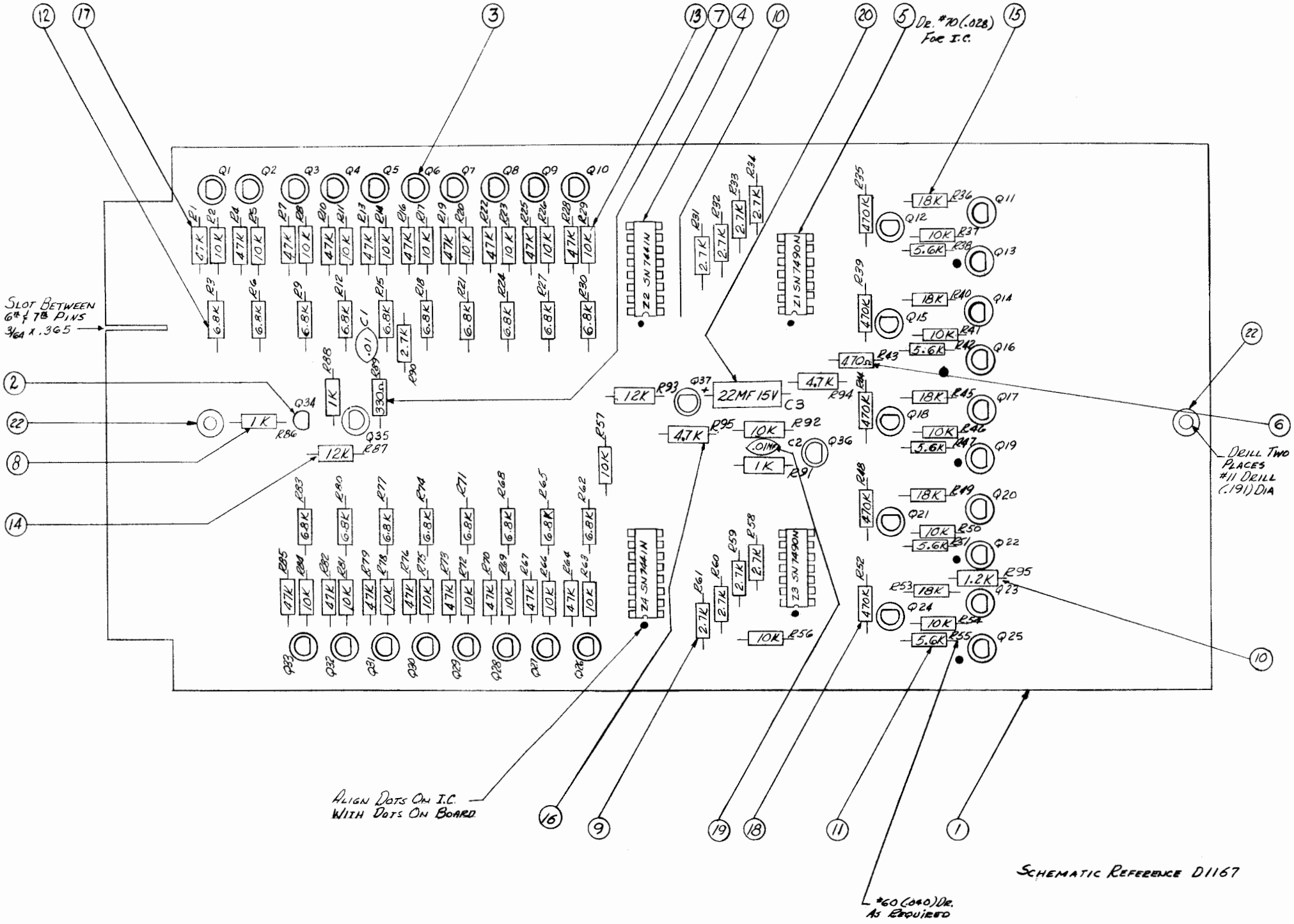
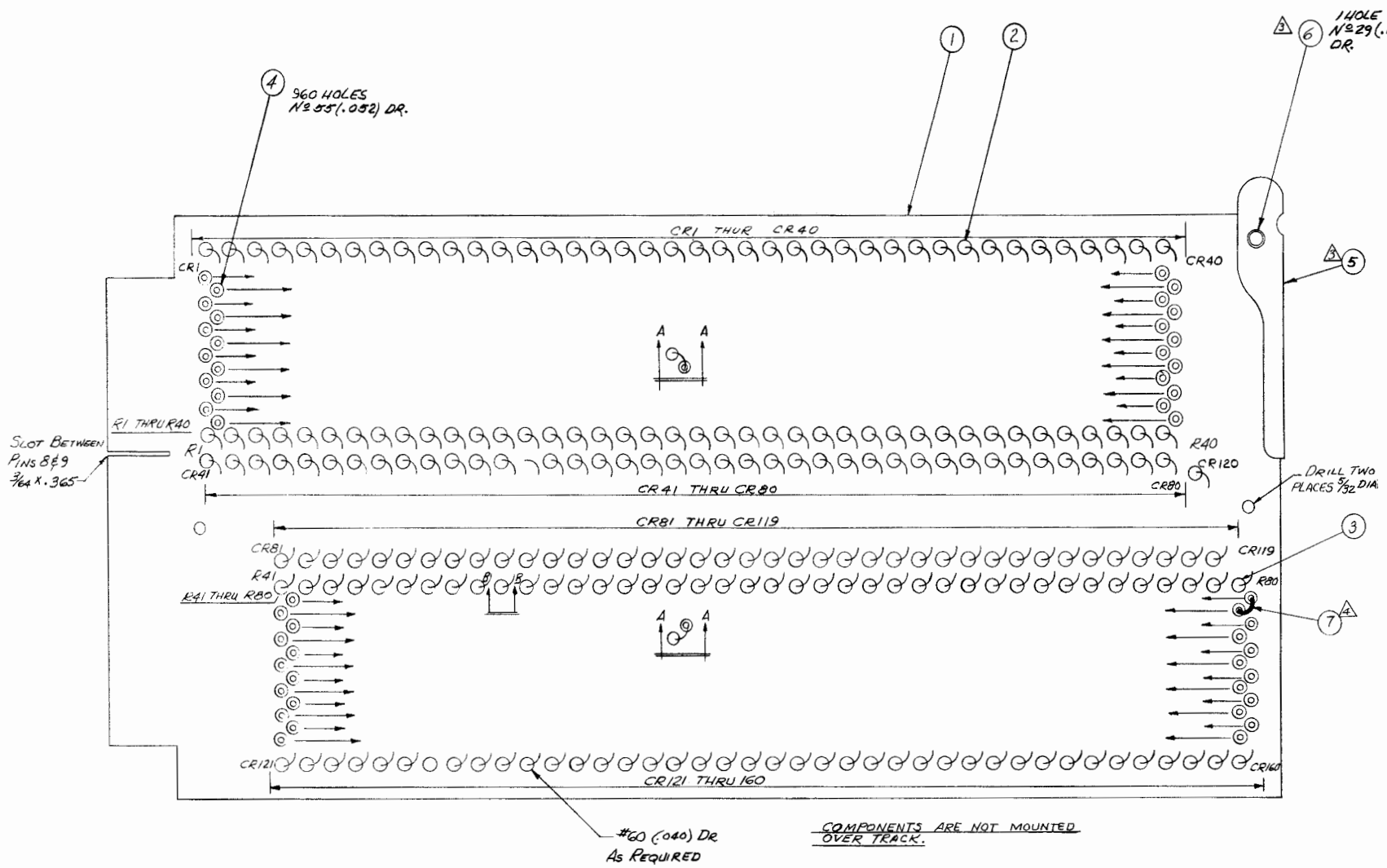


Figure 6-4. P.C. Board Assembly, Matrix Scanning Circuits (D1166B)

ITEM	REQ'D	PART NO	DESCRIPTION	MAT'L OR MFR	MAT'L SPEC OR CAT. PART NO.	FINISH	FINISH SPEC	CKT SYM
22	2	B1193-1	STANDOFF	F.E.C.				
21								
20	1	1500	CAPACITOR 22MF, 15V., 10%	SPRAGUE				
19	2	5B35Y5U103Z	CAPACITOR (DISC) .01MF, 25V.	ERIE				
18	5		RESISTOR 470K, 1/4W, 10%	A.B.				
17	18		47K, 1/4W, 10%					
16	2		4.7K, 1/4W, 10%					
15	5		18K, 1/4W, 10%					
14	2		12K, 1/4W, 10%					
13	26		10K, 1/4W, 10%					
12	18		6.8K, 1/4W, 10%					
11	5		5.6K, 1/4W, 10%					
10	1		1.2K 1/4W, 10%					
9	9		2.7K 1/4W, 10%					
8	3		1K, 1/4W, 10%					
7	1		330 Ω, 1/4W, 10%					
6	1		RESISTOR 470Ω, 1/4W, 10%	A.B.				
5	2	SN7490N	INT. CIRCUIT	T.I.				
4	2	SN7441N	INT. CIRCUIT	T.I.				
3	36	2N3394	TRANSISTOR	G.E.				
2	1	2N3905	TRANSISTOR	G.E.				
1	1	N0454A	P.C. BOARD	FEC				

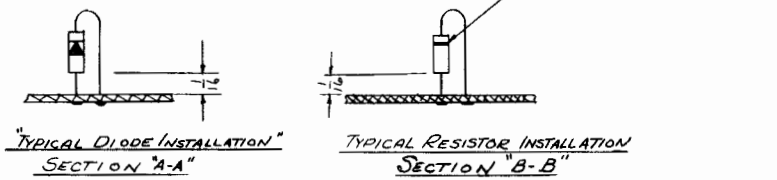
LIST OF MATERIAL

Figure 6-4. Parts List
(D1166B)



NOTES

1. SCHEMATIC REFERENCE D1170
2. DIODE QUANTITY AND INSTALLATION WILL DEPEND UPON CUSTOMERS. REQUIREMENTS.
3. ON BOARDS FOR 1319A; INSTALL BOARD RELEASE LEVER (ITEM 5) AND EYELET (ITEM 9B).
4. JUMPER OR DIODE USED IN THIS POSITION DEPENDS ON CUSTOMER REQ'S



"TYPICAL DIODE INSTALLATION" SECTION "A-A"

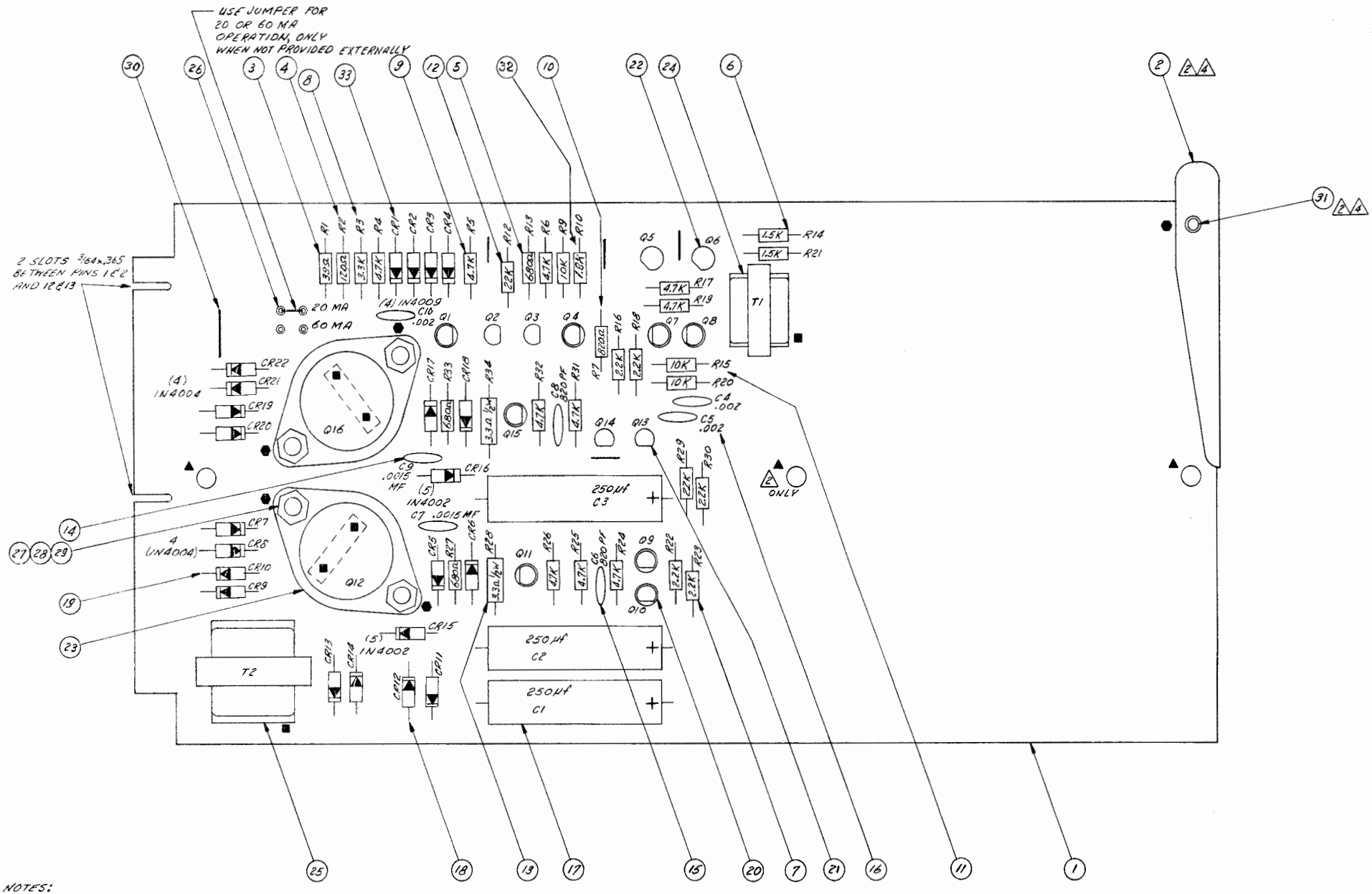
TYPICAL RESISTOR INSTALLATION SECTION "B-B"

Figure 6-5. P.C. Board Assembly, Matrix Circuits

ITEM	REQ'D	PART NO	DESCRIPTION	MAT'L OR MFR	MAT'L SPEC OR CAT. PART NO.	FINISH	FINISH SPEC	CKT SYM
6	1	A916	EYELET	STIMPSON				
5	1	B0977	BOARD RELEASE LEVER	F.E.C.				
4	960	56064	EYELETS	U.S.				
3	80		RESISTORS 4.7K, 1/4 W, 10%	AB				
2	160	IN4009	DIODES	GE				
1	1	NO453	P.C. BOARD	FEC				

LIST OF MATERIAL

Figure 6-5. Parts List
(D1169C)



NOTES:

1. SCHEMATIC REF D0823, SHEET 3
2. WHEN ASS'Y IS USED ON MODEL 1301 & 1309, DO NOT INSTALL ITEMS 2 & 31; SHEAR BOARD TO SHORT LENGTH; ALSO 1305, 1306.
3. DRILL ALL COMPONENT MTG HOLES NO. 60 (.040) DR, EXCEPT AS NOTED:
   - ■ - 16 HOLES, NO. 55 (.052) DR.
   - ● - 5 HOLES, NO. 30 (.128) DR.
   - ▲ - 2 HOLES, NO. 22 (.157) DR.
4. DO NOT INSTALL ITEMS 2 & 31 ON MODEL 1300, 1202A, 1202B, 1305, 1306

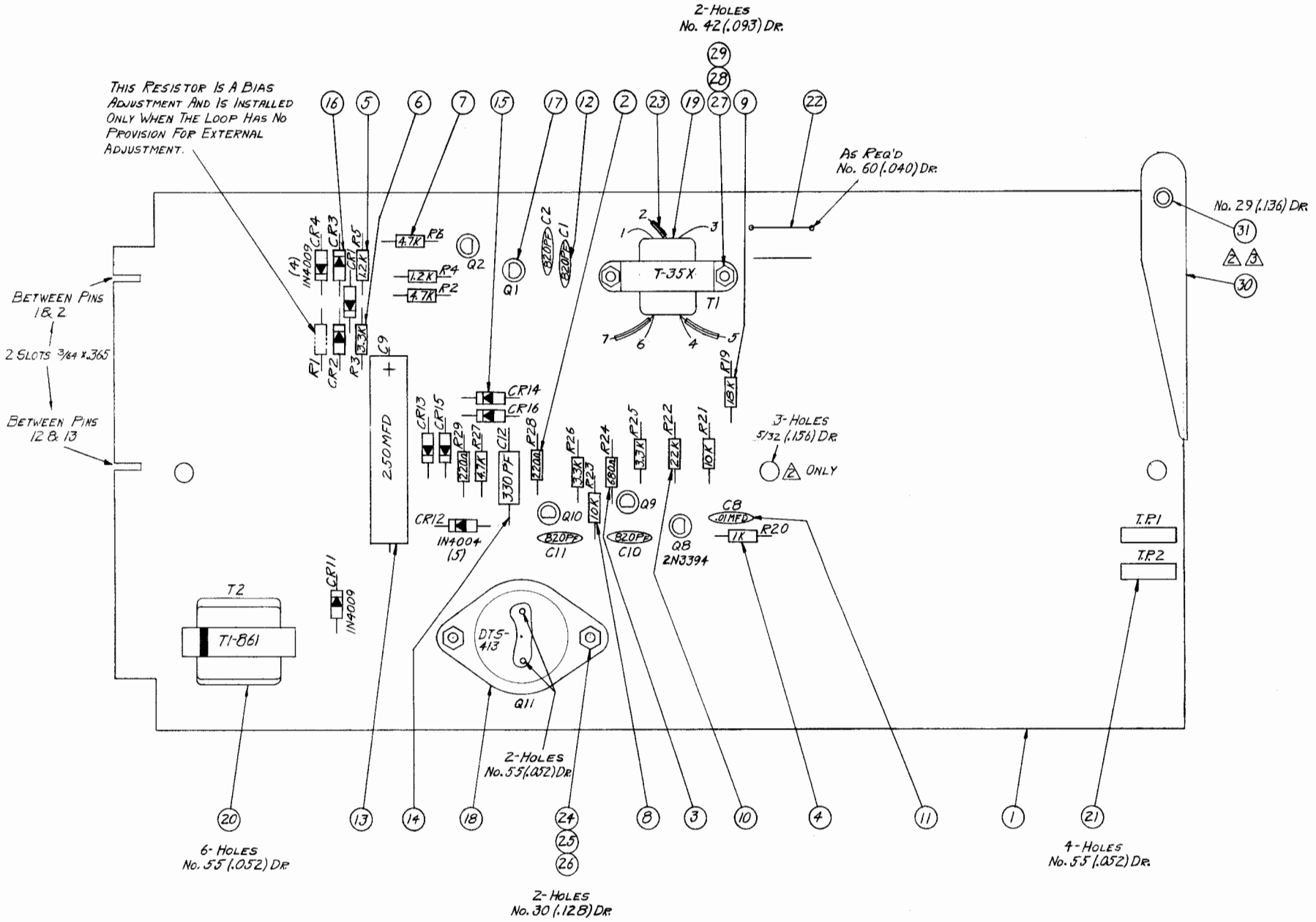
Figure 6-6. P.C. Board Assembly, Optional Isolated Polar Keyer (D0822J)

1N4002 = 200 P.I.V. Si
400 V = 400 P.I.V. Si

ITEM	REQ'D	PART NO	DESCRIPTION	MAT'L OR MFR	MAT'L SPEC OR CAT. PART NO.	FINISH	FINISH SPEC	CKT SYM
33	4	1N4009	DIODE	G.E.				
32	1		RESISTOR, 1.8K 1/4W 10%	A.B.				
2 4 31	1		RIVET, TUBULAR, 1/8 D x 3/16 LG	STIMPSON	BRASS	N.P.		
30	A/R		WIRE, Nº 22 GA, SOLID	ALPHA				
29	4		NUT, HEX, Nº 4-40 x 3/16 A.F.	BRASS		N.P.		
28	4		WASHER, Nº 4 SPLIT LOCK	PHOZ BRZ		N.P.		
27	4		SCREW, Nº 4-40 x 5/16 Bd. Hd.	BRASS		N.P.		
26	4	S-6064	EYELET	U.S.				
25	1	TM1127	TRANSFORMER	XMFRS INC				
24	1	TM1124	TRANSFORMER	XMFRS INC				
23	2	07S 413	TRANSISTOR	DELCO				
22	2	2N4274	TRANSISTOR	FAIRCHILD				
21	4	2N3905	TRANSISTOR	MOTOROLA				
20	8	2N3394	TRANSISTOR	G.E.				
19	8	1N4004	DIODE	MOTOROLA				
18	10	1N4002	DIODE	MOTOROLA				
17	3	TE 1138	CAPACITOR, 250 µf, 12V	SPRAGUE				
16	3	801 Z5V 202P	.002 µf, 600V	ERIE				
15	2	851 X5R 821	820PF, 1000V	ERIE				
14	2	801 Z5V 152P	CAPACITOR, .0015 µf, 600V	ERIE				
13	2	RC20GF3R3K	RESISTOR, 3.3Ω, 1/2 W, 10%	A.B.				
12	1	RC07GF223K	22K, 1/4 W, 10%					
11	3	103K	10K					
10	1	821K	820Ω					
9	10	472K	4.7K					
8	1	332K	3.3K					
7	7	222K	2.2K					
6	2	152K	1.5K					
5	3	681K	680Ω					
4	1	121K	120Ω					
3	1	RC07GF390K	RESISTOR, 39Ω, 1/4 W, 10%	A.B.				
2 4 2	1	80977	BOARD RELEASE LEVER	F.E.C.				
1	1	N0327C	P.C. BOARD	F.E.C.				

LIST OF MATERIAL

Figure 6-6. Parts List
(D0822J)



NOTES

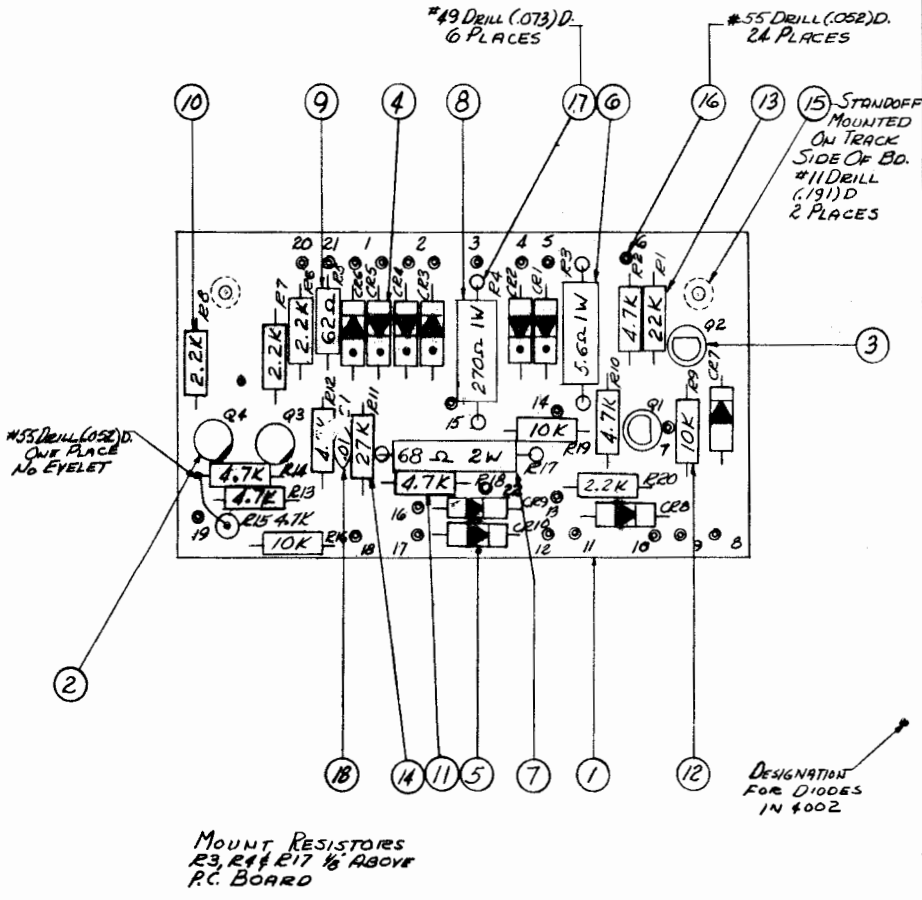
1. SCHEMATIC REF D0823, SHEET 2.
2. WHEN ASSY IS USED ON MODEL 1301, 1305, 1306 & 1309, DO NOT INSTALL ITEMS 30 & 31; SHEAR BOARD TO SHORT LENGTH.
3. DO NOT INSTALL ITEMS 30 & 31 ON MODEL 1202A, 1202B, 1300, 1305 & 1306

Figure 6-7. P.C. Board Assembly, Optional Isolated Neutral Keyer (D1110A)

ITEM	REQ'D	PART NO	DESCRIPTION	MAT'L OR MFR	MAT'L SPEC OR CAT. PART NO.	FINISH	FINISH SPEC	CKT SYM
31	1	A916	EYELET	STIMPSON				
30	1	B0977	BOARD RELEASE LEVER	F.E.C.				
29	2		NUT, HEX., NO. 2-56 x 3/16 A.F.	BRASS		N.P.		
28	2		WASHER, NO. 2 SPLIT LOCK	↑		↑		
27	2		SCREW, NO. 2-56 x 1/4 BD. HD.					
26	2		NUT, HEX., NO. 4-40 x 3/16 A.F.					
25	2		WASHER, NO. 4 SPLIT LOCK	↓		↓		
24	2		SCREW, NO. 4-40 x 5/16 BD. HD.	BRASS		N.P.		
23	A/R		TUBING, 22 GA., NATURAL	ALPHA				
22	A/R		WIRE, 22 GA. SOLID	ALPHA				
21	2	2-582118-2	TEST POINT	AMP				
20	1	T1-861	TRANSFORMER	TRANS. INC.				
19	1	T-35X	TRANSFORMER	TRIAD				
18	1	DTS-413	TRANSISTOR	DELCO				
17	5	2N3394	TRANSISTOR	G.E.				
16	5	IN4009	DIODE	G.E.				
15	5	IN4004	DIODE	MOT				
14	1	CM15-E-331J	CAPACITOR, 330 PF, 500 V.	ELMENCO				
13	1	TE-1138	↑ 250 MFD, 12 V.	SPRAGUE				
12	4	851-X5R-B21K	↓ 820 PF, 1000 V.	ERIE				
11	1	5835-Y5U-103Z	CAPACITOR, .01 MFD, 25 V.	ERIE				
10	1	RC07GF223K	RESISTOR, 22K, 1/4 W, 10%	A.B.				
9	1	183K	↑ 18K ↑	↑				
8	2	103K	10K					
7	3	472K	4.7K					
6	3	332K	3.3K					
5	2	122K	1.2K					
4	1	102K	1K					
3	1	681K	↓ 680Ω ↓	↓				
2	2	RC07GF221K	RESISTOR, 220Ω, 1/4 W, 10%	A.B.				
1	1	N0464A	P.C. BOARD	F.E.C.				

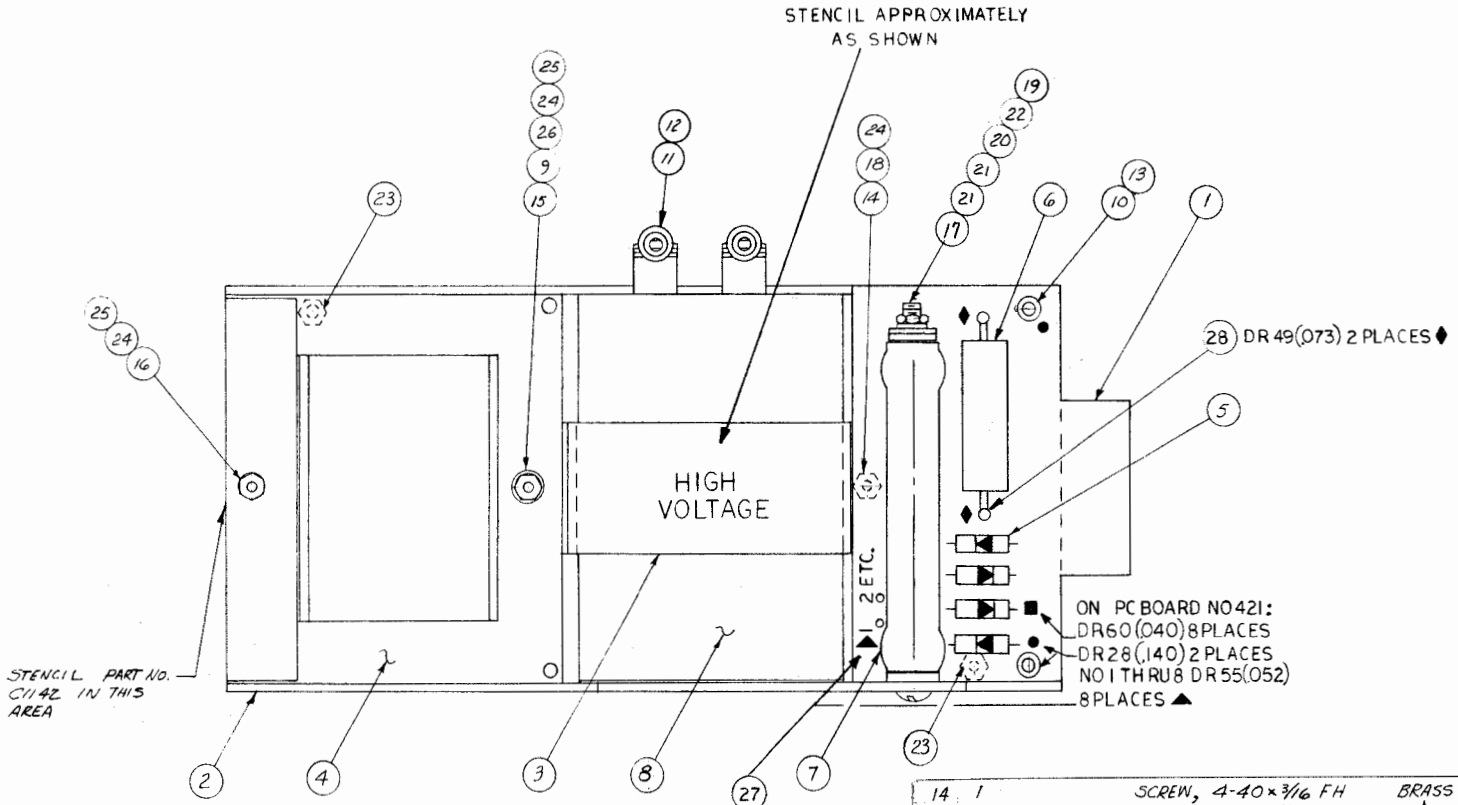
LIST OF MATERIAL

Figure 6-7. Parts List
(D1110A)



ITEM	REQ'D	PART NO	DESCRIPTION	MATL OR MFR	MATL SPEC OR CAT. PART NO	FINISH	FINISH SPEC	CKT SYM
			LIST OF MATERIAL					
18	1	5835 Y5U103Z	Disc. Capacitor .01MF 25V.	Erie				
17	24	S6064	Eyelets	U.S.				
16	6	2059	Eyelets	Stimpson				
15	2	1246-14	Standoffs	CTC				
14	1		27K, 1/4 W, 10%	AB				
13	1		22K, 1/4 W, 10%					
12	3		10K, 1/4W, 10%					
11	7		4.7K, 1/4W 10%					
10	4		2.2K 1/4W, 10%					
9	1		62Ω 1/4W, 10%					
8	1		270Ω 1W, 10%					
7	1		68 Ω 2W, 10%					
6	1		Resistors 5.6Ω 1W. 10%	AB				
5	4	1N4009	Diodes	GE				
4	6	1N4002	Diodes	GE				
3	2	2N3394	Transistor	GE	Q1 Q2			
2	2	2N4274	Transistor	Fairchild	Q3 Q4			
1	1	N0489A	P.C. Board	F.E.C.				

Figure 6-8. P.C. Board Assembly, Low Level Power Supply (C1332A)



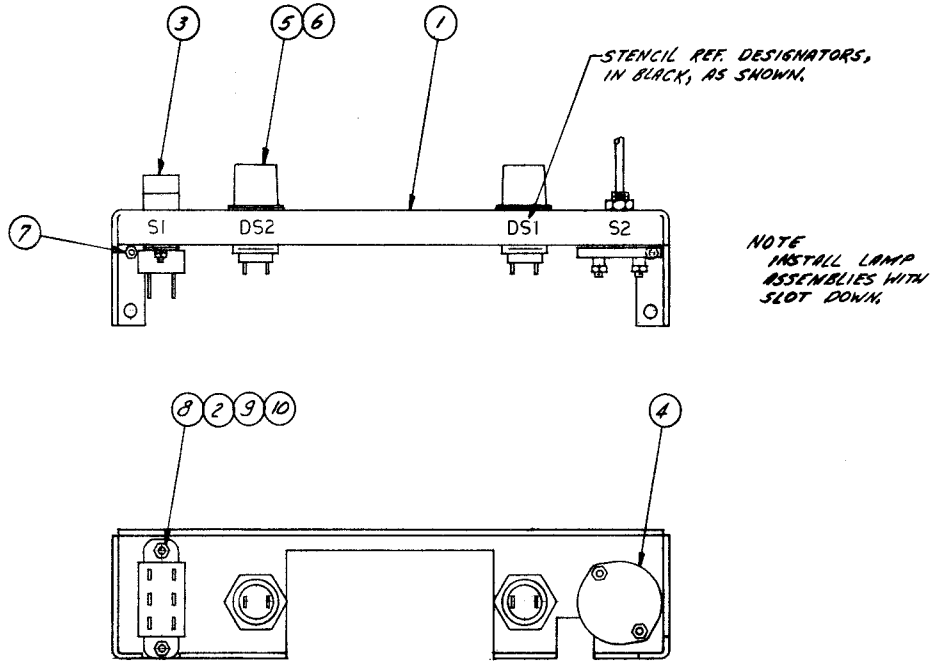
ITEM	REQ'D	PART NO	DESCRIPTION	MAT'L OR MFR	MAT'L SPEC OR CAT. PART NO	FINISH	FINISH SPEC	CKT SYM
28	2	2059	EYELET	STIMPSON				
27	8	S-6064	EYELET	U.S.				
26	1		WASHER, FLAT NO.4	BRASS		NI-P		
25	2		NUT, HEX 4-40 1/4 AF	STAINLESS STEEL				
24	3		WASHER SPLIT LOCK NO4					
23	2	4GN-(.062)-RL	PRESS NUT 6-32	PMP				
22	1		WASHER, SPLIT LOCK NO.6					
21	2	2162	WASHER, FIBRE NO.6	SMITH				
20	1		WASHER, FLAT NO.6	BRASS		NI-P		
19	1		NUT, HEX 6-32 1/4 AF	↕		↕		
18	1		NUT, HEX 4-40 3/16 AF					
17	1		SCREW, 6-32 x 2 1/4 B H	BRASS		NI-P		
16	1		SCREW, 4-40 x 1 B H	STAINLESS STEEL				
15	1		SCREW, 4-40 x 1 3/8 F H	STAINLESS STEEL				

LIST OF MATERIAL

WIRE PER B1102

ITEM	REQ'D	PART NO	DESCRIPTION	MAT'L OR MFR	MAT'L SPEC OR CAT. PART NO	FINISH	FINISH SPEC	CKT SYM
14	1		SCREW, 4-40 x 3/16 F H	BRASS		NHP		
13	2		SCREW, 4-40 x 3/8 F H	↕		↕		
12	2		WASHERS NO. 10 INT. TOOTH	BRASS		NI-P		
11	2	31889	TERMINAL	AMP				
10	2	1300-10	SPACER	CTC				
9	1	1247-3	SPACER	CTC				
8	1	CG2750U150A1	CAPACITOR	MALLORY				
7	1	3826	RESISTOR 10K 10 WATT	OHMITE				
6	1	M535045-1	RESISTOR 10Ω 2 WATT	A-B				
5	4	IN4004	RECTIFIER DIODE	GE				
4	1	TM1017	TRANSFORMER	TRANS. INC.				
3	1	B1117	BRACKET	FEC				
2	1	C1173	CHASSIS	↕				
1	1	NO421	P.C. BOARD	FEC				

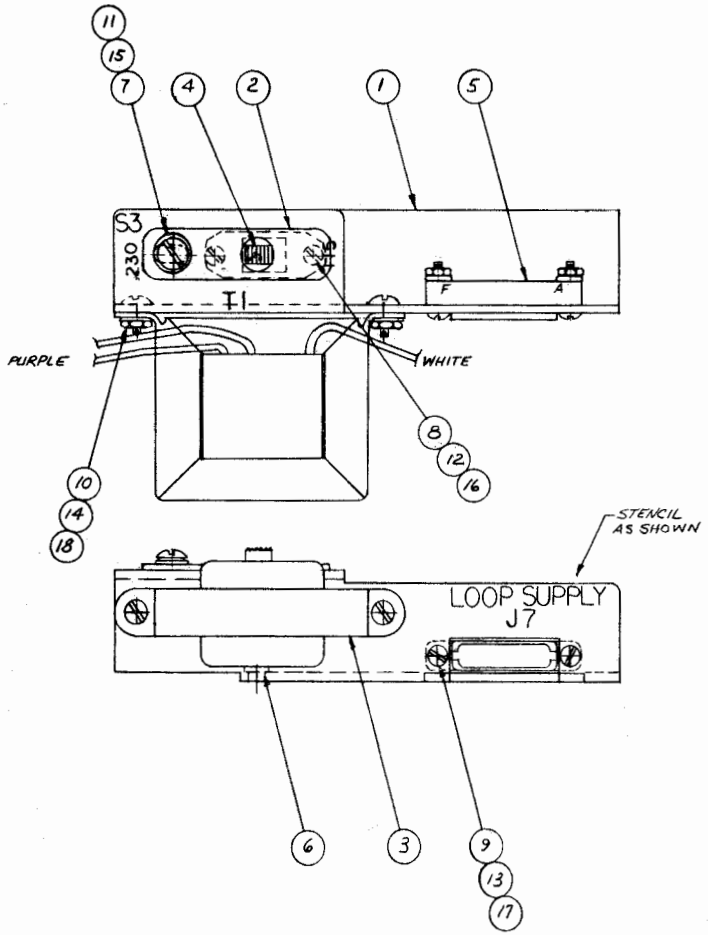
Figure 6-9. Assembly, Optional Loop Power Supply (C1142B)



ITEM	REQ'D	PART NO	DESCRIPTION	MAT'L OR MFR	MAT'L SPEC OR CAT. PART NO.	FINISH	FINISH SPEC	CKT SYM
10	2		NUT, HEX, Nº 4-40 x 3/16 A.F.	BRASS		N.P.		
9	2		WASHER, Nº 4 SPLIT LOCK	PHOS BRZ		N.P.		
8	2		SCREW, Nº 4-40 x 5/8 FLT Hd.	BRASS		N.P.		
7	2	PN 34N.062FL	FLUSH NUT	PMP				
6	2	327	BULB	G.E.				
5	2	2730-L-256-WA-P	LAMP ASS'Y	PENDAR				
4	1	X7204IN	SWITCH ROTARY	J.B.T.	1/2" LONG ROUND SHAFT			
3	1	RS-72	SWITCH DPDT	STACKPOLE				
2	2	B1139	SPACER	F.E.C.				
1	1	C1242	BRACKET	F.E.C.				

LIST OF MATERIAL

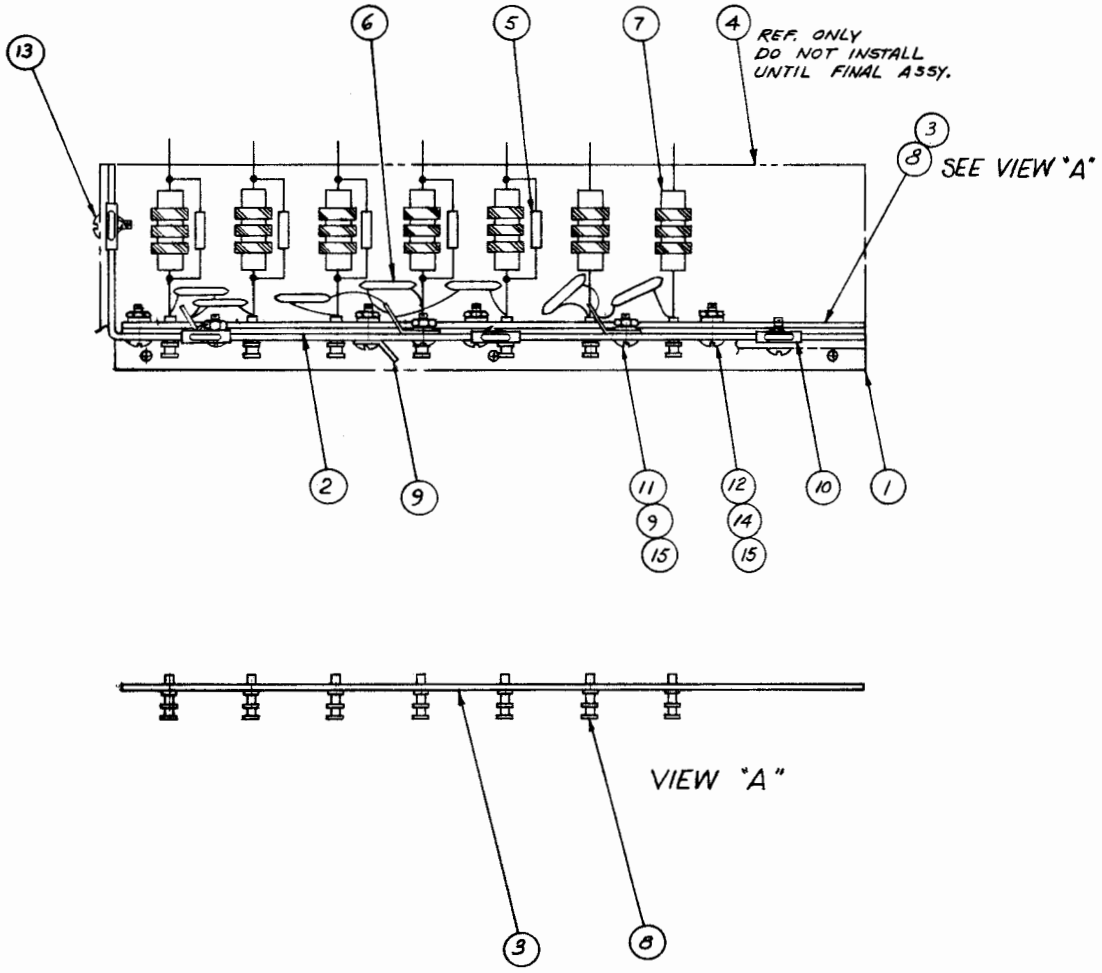
Figure 6-10. Assembly, Switch And Lights Bracket (C1312A)



ITEM	REQ'D	PART NO	DESCRIPTION	MAT'L OR MFR	MAT'L SPEC OR CAT. PART NO.	FINISH	FINISH SPEC	CKT SYM
18	2		NUT, HEX 6-32 × 1/4 AF	BRASS		NP		
17	2		NUT, HEX 4-40 × 1/4 AF	BRASS				
16	2		NUT, HEX 4-40 × 3/16 AF	BRASS				
15	1		WASHER, NO. 8 FLAT	STEEL				
14	2		WASHER, NO. 6 INT. TOOTH	PHOS. BRZ.				
13	2		WASHER, NO. 4 INT. TOOTH	PHOS. BRZ.				
12	2		WASHER, NO. 4 SPLIT LOCK	PHOS. BRZ.				
11	1		SCREW, 8-32 × 1/4 BD. HD.	BRASS				
10	2		SCREW, 6-32 × 5/16 BD. HD.	BRASS				
9	2		SCREW, 4-40-1/2 BD. HD.	BRASS				
8	2		SCREW, 4-40-1/4 FLAT HD.	BRASS		NP		
7	1	8-32 X .086	LAMSON NUT	LAM. SESS.				
6	1	6-32 X .086	LAMSON NUT	LAM. SESS.				
5	1	251-06-30-160	CONNECTOR	CJ				
4	1	G326	SWITCH, 2PDT	CONT. WIRT				
3	1	TM1094	TRANSFORMER	TRAN. INC.				
2	1	B1022	PLATE, SWITCH	FEC				
1	1	C1319	BRACKET, SWITCH	FEC				

LIST OF MATERIAL

Figure 6-11. Assembly, Switch And Transformer Bracket (C1339)



REF. W/D D1149

Figure 6-12. Assembly, Output Filter (D1183)

ITEM	REQ'D	PART NO	DESCRIPTION	MAT'L OR MFR	MAT'L SPEC OR CAT. PART NO.	FINISH	FINISH SPEC	CKT SYM
15	7		NUT, HEX NO. 4-40×1/4 AF	BRASS		NI.-P.		
14	4		WASHER, NO. 4 INT. TOOTH	PHOS. BRZ.		↕		
13	4		SCREW, 6-32 × 5/16 BD. HD.	BRASS				
12	4		SCREW, 4-40× 5/16 BD. HD.	BRASS				
11	3		SCREW, 4-40 × 1/4 BD. HD.	BRASS		NI.-P.		
10	4	C8020-632-67	SPEED NUT	TINNERMAN				
9	4	1416-4	SOLDER LUG	SMITH				
8	7	1548-2	TERMINAL	CTC				
7	7	6302	CHOKE	MILLER				
6	7	5HK-510	CAPACITOR, .01μF, 1000 V	SPRAGUE				
5	5		RESISTOR, 1.2K, 1/4W 10%	A-B				
4	1	C1331	COVER	FEC				
3	1	B1218	TERMINAL BOARD	↕				
2	1	B1219	INSULATOR					
1	1	C1330	BRACKET	FEC				

LIST OF MATERIAL

Figure 6-12. Parts List
(D1183)