## INSTRUCTION MANUAL

## MODEL 1550A FREQUENCY SYNTHESIZER

## November 1971

FREDERICK ELECTRONICS CORPORATION Hayward Road, Post Office Box 502 Frederick, Maryland 21701

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Figure 1-1. Mode1 1550A Frequency Synthesizer


SECTION I

## INTRODUCTION

### 1.1 PURPOSE OF EQUIPMENT

The Model 1550A Frequency Synthesizer is designed for operation with the FEC Model 1500 Series FSK Receivers to accurately tune the Receivers to signals throughout the range of 10 kHz to 30 MHz .

The Receivers use a narrow-band first IF filter centered on 9 MHz . The plan of the Receiver is such that for signal frequencies between 0 and 13 MHz , the local oscillator (LO) is 9 MHz above the incoming signal frequency or in the range of 9 to 22 MHz . For signal frequencies between 13 and 30 MHz , the LO is 9 MHz below the signal frequency or between 4 and 21 MHz . Thus the Frequency Synthesizer covers a range of 4 to 22 MHz .

Six rotary switches on the front panel digitally control the Synthesizer frequency in steps of $10 \mathrm{MHz}, 1 \mathrm{MHz}, 100 \mathrm{kHz}$, $10 \mathrm{kHz}, 1 \mathrm{kHz}$, and 100 Hz . A $10-t u r n$ vernier control potentiometer can also be selected in place of the 1 kHz and 100 Hz switches to provide continuous tuning of the output frequency with a tuning sensitivity of 1 kHz per turn. Logic built into the Model 1550A introduces the required 9 MHz offset permitting the controls to be set for the desired Receiver frequency.

The Synthesizer produces a nominal 1 volt peak-to-peak output into a 50 ohm load at two separate rear panel connectors. These outputs are electrically isolated from each other and have a $90^{\circ}$ phase difference.

### 1.2 PHYSICAL DESCRIPTION

The Model 1550A Synthesizer contains easily removable printed circuit boards which are separated into high and low frequency circuits.

The high frequency circuits consist of boards for a main Voltage-Controlled Oscillator (VCO) A5, a programmable divider A2, and a pulse phase comparator A4. The HF circuits control the VCO output frequency in response to different positions of the front panel $10 \mathrm{MHz}, 1 \mathrm{MHz}, 100 \mathrm{KHz}$, and 10 KHz switches.

The low frequency circuits consist of boards for an offset voltage-controlled oscillator and mixer A3, a programmable divider A7, and a pulse phase comparator A8. The LF circuits control the frequency of the offset oscillator to determine the 1 kHz and 100 Hz component of the output signal. The offset oscillator can be controlled by either the front panel 1 KHz and 100 Hz selector switches or by the front panel 10-turn VERNIER control.

The Synthesizer is conveniently packaged for mounting in a standard 19" equipment rack. The unit measures 19" wide, 17" deep, and $13 / 4^{\prime \prime}$ high and weighs approximately 10 lbs.

Wiring is accomplished with small Molex connectors to avoid grouping of critical HF signal wires thus minimizing RF interaction in the Synthesizer. Critical circuits are also isolated and filtered to prevent audio or RF interference with their normal circuit functions. The Power Supply utilizes seriesregulators to prevent intercoupling resulting from line or load variations.

### 1.3 SPECIFICATIONS

General specifications for the Synthesizer are listed in Table 1-1.

Table 1-1. Specifications For Model 1550A Frequency Synthesizer

## ELECTRICAL

Receiver Range Covered . . . 10 kHz to 30 MHz
Receiver IF Frequency . . . 9 MHz
Receiver Conversion Plan .. 9 MHz above received frequency in range 10 kHz to 13 MHz 9 MHz below received frequency in range 13 MHz to 30 MHz

Synthesizer Output Range .. 4 to 22 MHz with fine tuning in 100 Hz steps

Frequency Selection . . . . Dialed to direct operating frequency of Receiver ( 10 kHz to 30 MHz )

# Table 1-1. Specifications For Mode1 1550A Frequency Synthesizer (cont.) 

Frequency Control
Vernier Mode . . . . . . Synthesized from internal reference crystal oscillator and vernier offset oscillator
Digital Mode . . . . . . Synthesized from internal reference oscillator

Frequency Stability
Vernier Mode . . . . . TCXO frequency standard stability $\pm 100 \mathrm{~Hz}$ from $0^{\circ}$ to $50^{\circ} \mathrm{C}$

Digital Mode . . . . . . Determined by TCXO frequency standard option:

TCXO Part B1690-1 gives $\pm 1$ PPM from $0^{\circ}$ to $50^{\circ} \mathrm{C}$

TCXO Part B1690-2 gives $\pm 1$ PPM from $0^{\circ}$ to $25^{\circ} \mathrm{C} / \pm 0.5 \mathrm{PPM}$ from 250 to $50^{\circ} \mathrm{C}$


Frequency Accuracy
Vernier Mode . . . . . 100 Hz after calibration at operating
Digital Mode . . . . . . $\pm 3 \mathrm{~Hz}$ after calibration at operating temperature

Settling Time Of HF
Phase-Lock Loop . . . . . . Less than 1 second
Settling Time Of LF
Phase-Lock Loop . . . . . . Less than 1 second
Output Levels . . . . . . Two, individually adjustable up to nominal 1 volt peak-to-peak

Load Impedance. . . . . . . Nominal 50 ohms unbalanced

# Table 1-1. Specifications For Model 1550A Frequency Synthesizer (cont.) 

Spurious Output. . . . . . .Non-Harmonic: 55 db down
Suppression. . . . . . . . .Harmonic: 31 db down for 2 nd and 3 rd , 36 db or better for 4 th and higher

Input Power. . . . . . . . .115/230 vac
47 to 63 Hz single phase, 25 watts maximum

ENVI RONMENTAL
Operating Temperature
Range. . . . . . . . . . . $0^{\circ}$ to $50^{\circ} \mathrm{C}$
Relative Humidity. . . . .Up to 95\%
MECHANICAL
Dimensions. . . . . . . . 19 inches wide 1-3/4 inches high 17 inches deep

Mounting . . . . . . . .Fixed or slide mounting in a standard 19 -inch equipment rack

Weight. . . . . . . . . . 10 pounds
Electrical Connections . . RF Outputs: Two female BNC on rear panel

AC Power: 3-prong plug on rear pane1

## SECTION II

I NSTALLAT ION

### 2.1 INSPECTION

After removal from its shipping container the unit should be inspected. If any physical damage is found, file a written claim with the shipping agency. Send a copy of this claim to Frederick Electronics Corporation, P. O. Box 502, Frederick, Maryland 21701.
2.1.1 EQUIPMENT SUPPLIED

Equipment supplied includes those items listed in Table 2-1.

Table 2-1. Equipment Supplied

| Number Of <br> Shipping Boxes | Contents |
| :---: | :---: |
| 1 | 1 Model 1550A Frequency <br> Synthesizer <br> 2 Instruction Manuals |

## NOTE

More than one unit may be packed in a single container when bulk orders are shipped to a common point.

### 2.1.2 EQUIPMENT REQUIRED BUT NOT SUPPLIED

Equipment required but not supplied includes those items listed below.

1. Coaxial cables to connect Synthesizer to Receiver.
2. Four rack mounting screws.

### 2.2 POWER REQUIREMENTS

The Synthesizer is shipped ready to operate directly on 105130 vac, $47-63 \mathrm{~Hz}$ current. Power is applied to the Synthesizer by plugging its power cord into an ac outlet. Provision is also made in the Synthesizer for operation from a $230-v o l t$ source by repositioning switch Sl located on Power Supply board A1.

## CAUTION

Switch must be in correct position before the Synthesizer can operate on 230 volts. Serious damage will result if the unit is connected to 230 volts without this change.

### 2.3 MOUNT ING

The Synthesizer is designed to mount in a standard 19-inch equipment rack. A vertical rack space of $1-3 / 4$ inches is required.

### 2.4 OUTPUT CONNECTIONS

The Synthesizer is designed to deliver RF outputs into coaxial transmission lines having an impedance of 50 ohms. Connections from the Synthesizer to the associated Receiver are provided at $B N C$ jacks located on the rear panel of the unit.

The coaxial cables used to connect the Synthesizer to the Receiver should be of high quality in order to minimize radiation of the output signal. It is particularly important that the BNC connectors at the cable ends be well attached so that there is good electrical continuity between the shield braid of the coaxial cable and the external housing of the connector. Detailed information on transmission lines can be found in the Radio Amateurs Handbook and the ARRL Antenna Handbook, both published by the American Radio Relay League, Newington, Connecticut, U.S.A.

The Synthesizer will not be harmed if the outputs are open circuited or temporarily short circuited. Figure 2-1 below shows a Model 1550A connected to a pair of Model 1500B Receivers in a typical space diversity system.


Figure 2-1. Typical Synthesizer Connections

### 2.5 INITIAL TESTS

After the Model 1550A is properly installed, tests should be conducted to insure that the unit is operating properly. Operating steps are provided in Section 3 and Minimum Performance Tests are provided in Section 5.

OPERATION

### 3.1 CONTROLS AND INDICATORS

Operating controls and indicators are located on the front panel of the Model 1550A and the functions are listed in Table 3-1.

Table 3-1. Controls And Indicators

| CONTROL OR I NDI CATOR | FUNCTION |
| :---: | :---: |
| POWER Lamp DS1 | Lights when ac power is applied to the Synthesizer. No power switch is provided. |
| LOSS OF LOCK Lamp DS2 | Lights to indicate a malfunction in the VCO phase-lock loop. Also lights when OPER SBY switch is in SBY position. |
| OPER SBY Switch Sl | SBY position removes dc power from the VCO to disable the Synthesizer outputs and lights LOSS OF LOCK lamp. OPER position applies de power to VCO to generate the Synthesizer outputs. |
| Mode Switch S2 | VERNIER position selects VERNIER control of 0 to 10 kHz component of output frequency. <br> $1 \mathrm{KHz}-100 \mathrm{~Hz}$ position selects 1 KHz and 100 Hz switches to control 0 to 10 kHz component of output frequency. |
| HF Selector Switches (S1-S4 on board A2) | 10 MHz switch S 1 selects receiver frequency range of 0 to 9 MHz (position 0), 10 to 19 MHz (position 1), or 20 to 22 MHz (position 2). <br> 1 MHz switch S 2 selects frequency component over range of 0 to 9 MHz in 1 MHz steps. <br> 100 KHz switch S 3 selects frequency component over range of 0 to 900 kHz in 100 kHz steps. |

Table 3-1. Controls And Indicators (cont.)

| CONTROL OR INDICATOR | FUNCTION |
| :---: | :---: |
| HF Selector Switches (cont.) | 10 KHz switch S 4 selects frequency component over range of 0 to 90 kHz in 10 kHz steps. |
| LF Selector Switches (S1-S2 on board A7) | 1 KHz switch S1 selects frequency component over range of 0 to 9 kHz in 1 kHz steps. |
|  | 100 Hz switch S 2 selects frequency component over range of 0 to 900 Hz in 100 Hz steps. |
| VERNIER Control R3 | Allows continuous tuning of receiver frequency over a range of 0 to 10 kHz . |

### 3.2 USE OF CONTROLS

The frequency selector switches may be set in any sequence to dial the desired receiver frequency. If the desired frequency is 15.7374 the first four digits are selected by setting the switches as shown below.

$$
\begin{aligned}
10 \mathrm{MHz} \text { switch to } 1 & =10.000 \mathrm{MHz} \\
1 \mathrm{MHz} \text { switch to } 5 & =05.000 \mathrm{MHz} \\
100 \mathrm{KHz} \text { switch to } 7 & =00.700 \mathrm{MHz} \\
10 \mathrm{KHz} \text { switch to } 3 & =\frac{00.030}{15.730} \mathrm{MHz}
\end{aligned}
$$

The last two digits of the desired frequency can be selected with either the 1 KHz and 100 Hz selector switches or the continuous tune VERNIER control depending on the setting of the mode switch.

When the digital mode is selected, the last two digits are determined by setting the $1 \mathrm{KHz}-100 \mathrm{~Hz}$ switches as shown below.

1 KHz switch to $7=00.0070 \mathrm{MHz}$
J.00 Hz switch to $4=\underline{00.0004} \mathrm{MHz}$
00.0074 MHz
$+15.7300 \mathrm{MHz}$
15.7374 MHz

When the VERNIER mode is selected, the last portion of the frequency is dialed by rotating the VERNIER control to a reading of 7.40 as shown below:


This position sets the offset oscillator to within 100 Hz of 7.4 kHz to produce approximately the same output frequency as selected above by the $1 \mathrm{KHz}-100 \mathrm{~Hz}$ switches. Further adjustments of the VERNIER frequency control can be made on the basis of the received signal quality from the receiver.

The digital mode provides considerably improved stability over the VERNIER mode and, thus, should normally be selected. However, it is often convenient for the operator to tune the receiver with the VERNIER control if the exact received frequency is not known. After the receiver is tuned the 1 KHz and 100 Hz selector switches are set to the VERNIER reading and the Synthesizer is switched to the $1 \mathrm{KHz-100} \mathrm{~Hz}$ position.

Digital logic built into the Synthesizer automatically produces the frequency offset required to convert the received carrier to the 9 MHz If of the receiver. The 9 MHz offset is above the dialed frequency in the range of 0 to 13 MHz and below the dialed frequency in the range of 13 to 30 MHz .

In the above example, since the received frequency is in the range of $13-30 \mathrm{MHz}$, the actual Synthesizer output frequency will be 9 MHz below the received frequency or 6.7374 MHz .

### 3.3 OPERATING THE SYNTHESIZER

Before operating the Synthesizer, make sure that it is properly installed as described in Section II of this manual. Review the associated Receiver instruction manual to become familiar with Receiver tuning procedures. Then proceed as follows:

1. Check that POWER indicator lamp is lit.
2. Determine operating frequency for associated Receiver. Set mode switch to VERNIER position.

## NOTE

Synthesizer can be set directly to digital position when precise Receiver Frequency is known.
3. Set frequency selector switches and VERNIER control to match desired Receiver frequency.
4. Set Receiver controls for operation from a remote oscillator (crystal switch to position $R$ on Model 1500).
5. Apply power to Receiver and tune preselector to operating frequency.
6. After preselector is tuned, carefully adjust VERNIER control on Synthesizer for a maximum signal amplitude on Receiver S-Meter. Note reading on VERNIER dial and set 1 KHz and 100 Hz switches to VERNIER reading. Set mode switch to $1 \mathrm{KHz}-100 \mathrm{~Hz}$ position.
7. Adjust Receiver audio output level and BFO settings to suit the associated demodulator input requirements.

## SECTION IV

THEORY OF OPERATION

### 4.1 INTRODUCT ION

The Model 1550A Synthesizer uses a modified version of a digital phase-lock loop principle. Its operation may be described in terms of four frequency variables defined below and the digital frequency division ratio $N$ of a set of high speed counters where $N$ depends on the setting of the 10 MHz , $1 \mathrm{MHZ}, 100 \mathrm{KHz}$, and 10 KHz frequency selector switches.
$F_{0}=$ the actual output frequency of the Synthesizer generated by a HF voltage-controlled oscillator (VCO) in the range of 4 to 22 MHz .
$\mathrm{F}_{\mathrm{d}}=$ an offset frequency in the range of 20 to 30 kHz produced by a LF voltage-controlled oscillator.
$F_{t h}=$ an approximate 5 kHz tachometer frequency or PRF (Pulse Repetition Frequency) generated from the resultant of $\underline{F_{0}-F d}$ by the HF divide-by-N logic.
$\mathrm{F}_{\mathrm{rh}}=\mathrm{a} 5 \mathrm{kHz}$ reference frequency generated from a 4 MHz crystal oscillator frequency standard.

The main voltage-controlled oscillator of the Synthesizer operates at $\mathrm{F}_{0}$. A sample of the $\mathrm{F}_{0}$ signal is mixed in a single sideband mixer with $\mathrm{F}_{\mathrm{d}}$ to produce a result $\mathrm{F}_{\mathrm{O}}-\mathrm{Fd}$ which is divided first by 2 and again by factor $N$ to produce the frequency $F_{t h}$ given by

$$
\mathrm{F}_{\mathrm{th}}=\frac{\mathrm{Fo}_{\mathrm{O}}-\mathrm{Fd}}{2 \mathrm{~N}}
$$

A HF pulse phase comparator compares Fth with Frh to generate a control voltage input to the main VCO which maintains the two frequencies in exact agreement. Thus, the VCO phase-lock loop in effect solves the equation

$$
\mathrm{Frh}_{\mathrm{rh}}=\frac{\mathrm{Fo}_{0}-\mathrm{Fd}_{\mathrm{d}}}{2 \mathrm{~N}}
$$

which can be rearranged to the form

$$
\mathrm{F}_{\mathrm{o}}=\mathrm{N}\left(2 \mathrm{~F}_{\mathrm{rh}}\right)+\mathrm{F}_{\mathrm{d}}
$$

The second equation shows that the actual output frequency can be adjusted by varying $N$ through various integer values and/or by varying $\mathrm{F}_{\mathrm{d}}$ (offset frequency). For the numerical example where the output frequency $F_{0}$ is 6.1374 , the solved values are

$$
N-611
$$

$\mathrm{F}_{\mathrm{d}}-27.4 \mathrm{kHz}$
The frequency $F_{d}$ is developed by a similar $L F$ phase comparison when the digital mode is selected. The LF frequency variables are defined below and the digital division ratio $N$ depends on the settings of the 1 KHz and 100 Hz frequency selector switches.

$$
\begin{aligned}
\mathrm{F}_{\mathrm{d} 1}= & \text { The actual offset oscillator output frequency before } \\
& \text { a division by four or } \mathrm{F}_{\mathrm{d}} 4 . \text { Covers a range of } 80 \text { to } \\
& 119.6 \mathrm{kHz} .
\end{aligned}
$$

A sample of the offset oscillator output ( Fdl ) is divided by factor $N$ to produce $\mathrm{F}_{\mathrm{tl}}$ given by

$$
F_{t 1}=\frac{F_{d 1}}{N}
$$

A LF pulse phase comparator compares $\mathrm{F}_{\mathrm{t}} \mathrm{l}$ with $\mathrm{Frl}_{\mathrm{r}}$ to produce a control voltage to the offset oscillator which maintains $\mathrm{F}_{\mathrm{t}}$ and Frl in exact agreement. Thus, the LF phase-lock loop solves the equation

$$
\begin{aligned}
& \mathrm{Fr}_{\mathrm{l}}=\frac{\mathrm{F}_{\mathrm{d} 1}}{\mathrm{~N}} \\
& \text { or } \\
& \mathrm{F}_{\mathrm{d} 1}=\mathrm{N}\left(\mathrm{~F}_{\mathrm{r} 1}\right)
\end{aligned}
$$

The equation shows that the actual output frequency $\mathrm{F}_{\mathrm{d}}$ is also adjusted by varying $N$ through various integer values.

When the VERNIER mode is selected the LF digital loop is disabled and the offset oscillator output frequency is controlled directly by the VERNIER potentiometer impedance.

### 4.2 FUNCTIONAL DESCRI PTION

A block diagram of the Model 1550A is shown in Figure 4-1. The heart of the Synthesizer is the main Voltage-Controlled Oscillator (VCO) which can be electronically tuned over the range 4 to 22 MHz . The VCO develops two constant amplitude outputs which are nominally in phase quadrature (i.e., $90^{\circ}$ phase difference). Referred to as the $P$-phase and Q-phase, these outputs are supplied through buffer amplifiers to two output connectors on the rear of the Synthesizer chassis and to a Single Sideband (SSB) Mixer.

A second pair of inputs to the SSB mixer is developed from the offset oscillator whose output frequency $\mathrm{F}_{\mathrm{d}} \mathrm{can}$ be tuned between 20 and 30 kHz . A divide-by-4 counter at the output of the offset oscillator develops a pair of quadrature outputs at frequency $F_{d}$. The mixer difference frequency is applied through suitable interfacing circuitry to a high-speed divide-by-2 counter. The counter output drives the HF programmable digital divider with a division ratio $N$ which is determined by the setting of the $10 \mathrm{MHz}, 1 \mathrm{MHz}, 100 \mathrm{KHz}$ and 10 KHz front panel switches.

The HF programmable divider output produces the tach signal $\mathrm{F}_{\mathrm{th}}$ which is compared with the crystal reference signal Frh by a pulse phase comparator. The comparator produces a control voltage that varies as a function of changes in $F$ th. The phase-lock voltage controls the output frequency $\mathrm{F}_{\mathrm{o}}$ from the VCO to maintain continuous agreement between $\mathrm{F}_{\mathrm{th}}$ and Frh .

When the front panel switches are repositioned the phase comparator will tune the VCO output frequency until $\mathrm{F}_{\mathrm{th}}$ is returned to approximately 5 kHz . Thus, by appropriately wiring the programmable divider a Synthesizer output $\mathrm{F}_{\mathrm{O}}$ is generated which is directly related to the settings of the frequency switches and the offset oscillator.

The offset VCO frequency is controlled either by the continuously adjustable VERNIER potentiometer or by the LF programmable digital phase-1ock loop. The LF phase-1ock loop is similar in operation to the HF phase-lock loop.


Figure 4-1. Frequency Synthesizer Functiona1 B1ock Diagram D2123

In the digital mode, $\mathrm{F}_{\mathrm{d}}$ signals between 80 to 120 kHz are connected directly from the offset oscillator to the LF programmable divider. The selected divider ratio produces an output signal which is compared with the 400 Hz reference signal $\mathrm{F}_{\mathrm{r}}$ by the LF pulse phase comparator.

The comparator generates a voltage representative of the frequency difference between $\mathrm{F}_{\mathrm{t}}$ and $\mathrm{F}_{\mathrm{rl}}$ which causes an electronic vernier circuit to adjust the oscillator output accordingly. Phase-1ock is obtained when the oscillator produces an output frequency which divided by N is $\simeq 400 \mathrm{~Hz}$. Thus, when the $1 \mathrm{KHz-100} \mathrm{~Hz}$ switch settings are changed the comparator output adjusts the oscillator frequency until phase-lock is again obtained. The digital offset mode offers frequency accuracy on the order of $\pm 3 \mathrm{~Hz}$ versus a vernier mode accuracy of $\pm 100 \mathrm{~Hz}$.

A LOSS OF LOCK detector monitors both phase comparators to indicate when the Synthesizer is on frequency.

### 4.3 DETAILED CIRCUIT ANALYSIS

### 4.3.1 VOLTAGE-CONTROLLED OSCILLATOR (Figure 6-1)

The main VCO operates directly at the output frequency of the Synthesizer as determined by two RC all-pass sections connected to the HF phase-lock feedback loop from the phase comparator. Each all-pass section has a normalized transfer function $1-s / 1+s$ where $s=j F / F_{0}$ and contributes a $90^{\circ}$ phase shift at the tuned center frequency $F_{0}$. Thus, the conditions for oscillation at frequency $F_{0}$ are satisfied because the buffer amplifiers introduce an additional net phase shift of $180^{\circ}$ and the loop gain is unity.

The VCO is contained on board A5 and consists of two identical all-pass networks, feedback amplifier Q14, emitter followers Q10 and Q13, and output amp1ifiers Q11 and Q15. One al1pass section is driven by emitter follower Q13 and consists of unity amplifier Q9, voltage tuning control Field Effect Transistors (FET) Q2-Q3-Q4, and tuning capacitor C5. The other all-pass section is identical to the first and consists of Q12, Q5-Q6-Q7, and C21.

Each all-pass network introduces a $90^{\circ}$ phase shift from input signal to output signal when the oscillator frequency is $\mathrm{F}_{\mathrm{o}}$. This phase shift is produced by tuning the RC networks in the bases of Q9 and Q12. Since the emitter follower outputs are applied to both the base and emitter of amplifiers Q9 and Q12 a $90^{\circ}$ shift is obtained at the output only when the tuned base circuits produce the same drive to Q9 and Q12 as the emitter coupling. Thus, the strength of the $180^{\circ}$ shift imposed by the base drive equals the strength of the $0^{\circ}$ shift imposed
by the emitter drive producing a net result of $90^{\circ}$ phase shift at the collectors of Q9 and Q12. Feedback amplifier Q14 completes the phase-shift loop by introducing a $180^{\circ}$ shift with unity gain to produce a $360^{\circ}$ phase-shift which reinforces oscillation at frequency $\mathrm{F}_{0}$.

$$
900+900+1800=360^{\circ} \text { reinforces oscillation }
$$

For convenience, the all-pass section built around Q 9 is discussed in the following circuit analysis.

At frequencies well below the tuned frequency $F_{0}$, the base of Q9 is effectively grounded through R5 and the parallel conductance of $Q 2, Q 3$, and $Q 4$ because the reactance of C5 becomes large compared to the net resistance to ground. Since the base of $Q 9$ is near ground, RF signal current at the emitter is unrestricted by base drive causing the resultant current flow from Q13 to the collector of Q9 to induce an in-phase voltage at the collector of Q9. Because of the 00 phase-shift of both all-pass sections and the additional 1800 phase-shift introduced by feedback amplifier Q14, the feedback signal opposes oscillation at frequencies below $\mathrm{F}_{\mathrm{o}}$.

$$
0^{0}+00+1800=1800 \text { opposes oscillation }
$$

At frequencies well above the tuned frequency $\mathrm{F}_{0}$, capacitor C5 becomes a virtual short circuit so that the voltage at the emitter of Q13 is coupled to the base of Q9. In this frequency range, Q9 operates as a common-emitter stage with emitter degeneration provided by R9. The nominal gain remains unity but a voltage phase-shift of $180^{\circ}$ is introduced thru $Q 9$ and the feedback loop will not sustain oscillation at frequencies above $\mathrm{F}_{0}$.

$$
180^{\circ}+180^{\circ}+1800=00+180^{\circ}=180^{\circ} \text { opposes oscillation }
$$

At the selected frequency $F_{0}$, where the capacitive reactance of C5 just equals the net resistance of $R 5$ in parallel with the associated FET's, the phase-shift through amplifying stage Q9 is $90^{\circ}$. The signal, phase-shifted by this amount, is then buffered by emitter follower Q10 and applied to the second all-pass stage consisting of transistor Q12 which similarly introduces a $90^{\circ}$ phase-shift.

The resistance seen by capacitors C5 and C21 is voltagecontrolled by the parallel connected FET's. The FET's have drain-source conductance that is nearly a linear function of the voltage applied to the gates. Increasing the reverse
bias on these gates reduces conductance, increases the resistance, and thus lowers $\mathrm{F}_{\mathrm{O}}$. Since the total range of conductance in the FET's exceeds 10 to 1 , the result is an electronic tuning range which is approximately 10 to 1.

To ensure that the phase-lock loop has the required control range and damping factor, the control voltage produced by the pulse phase comparator is conditioned before being applied to the control junctions of the tuning FET's. The required filter consists of R2, R3, and C9. High frequency components are rolled off in this filter by means of the series resistance R2 and the shunt capacity C9. By introducing a low value resistance R3 in series with C9, phase lead compensation is obtained which tends to improve the damping factor of the loop. In normal operation with the loop locked, the variations in the control voltage applied to the oscillator are insufficient to forward bias either CR2 or CR1, which are in shunt with R2. Thus, the full filtering effect of $R 2$ is realized. However, when the Synthesizer is first turned on or when it is switched from one frequency to another, a large momentary error signal is generated in the phaselock loop. Under these conditions, a large value of R 2 would make the Synthesizer slow to acquire the desired output frequency. By limiting the voltage drop across R2, CR1 and CR2 reduce the effective value of R2 thus increasing the bandwidth of the feedback loop during frequency acquisition.

The oscillator produces quadrature outputs, designated the P-phase and the $Q$-phase, which are buffered by emitter followers Q11 and Q15, respectively. The outputs are applied to wideband amplifiers having a nominal gain of 5. The P-phase wideband amplifier (see Figure 6-1, Sheet 2) consists of a complementary differential stage (transistors Q16 and Q17) driving an output stage (Q18-Q19). A divider network, R27 and R25, monitors the average push-pull output level to provide negative feedback to Q16. The Q-phase amplifier is functionally identical but consists of Q22-Q23 and Q24-Q25. By using negative feedback to simultaneously amplify and attenuate the RF signal, the VCO is isolated from signals which might otherwise leak through the output amplifiers in the reverse direction.

The push-pull output is further isolated by a pair of complementary emitter follower circuits consisting of Q20-Q21 and Q26-Q27 for the P-phase and Q28-Q29 and Q30-Q31 for the Q-phase outputs.

One of the complementary outputs of each phase is applied to the SSB mixer circuit where it is heterodyned with the offset oscillator output.

The other output of each phase is applied to a rear panel BNC connector via a RF low-pass filter network and an output level potentiometer. The filter networks block harmonics above 22 MHz .

The Q-phase output is connected to Jl and the P-phase output is connected to J2. The $\mathrm{F}_{\mathrm{o}}$ signal is injected at the receiver remote oscillator input and replaces the standard Local Oscillator signal.

The P-phase amplifier also drives a VCO level control circuit through C20 (see 2 Figure 6-1, Sheet 1). In this circuit, CR5 and CR6 charge C18 to a voltage which is equal to the sum of a dc bias determined by potentiometer R18 and the peak-to-peak amplitude of the RF output of the wideband amplifier. If the output amplitude increases beyond the preset point, series diodes CR3 and CR4 become slightly forward-biased. These diodes act partly as clippers and partly as variable resistance elements. The level at the diode junction is ac coupled by C17 into the collector load of Q12 with the result that, as the diodes conduct more heavily, loop gain in the phase-shift oscillator is reduced thus lowering the level of oscillation. In this way, the level of oscillation is stabilized at a value which depends on the setting of potentiometer R1 8.

Since short-term frequency stability is extremely important in the VCO, the oscillator circuit must be well protected against audio or RF interference. Interference conducted through the Power Supply leads is shunted with RFI filters L1-L2 and the associated capacitors in the +12 and -12 volt lines.

Further isolation is provided by L14-C1 and L15-C12. L1 together with C2 and C4, form an RFI filter for the +12 volt supply. The -12 volt supply is similarly filtered.

RF harmonics generated by the VCO are reduced by two special filter circuits. The first filter connects at the junction of Q13-Q14 and is tuned with R75 to reduce harmonics when the output is in the range of 4 to 13 MHz . The second filter (one for each output line) is a low-pass filter which reduces harmonics in the range of 13 to 22 MHz .

Adjustment procedures for the VCO are provided in Section 5 of this manual.

### 4.3.2 HF PHASE-LOCK LOOP

The HF phase-lock loop consists of the SSB mixer, the programmable divider, and the pulse phase comparator.
4.3.2.1 SSB MIXER. Refer to Figure 6-2. The SSB mixer is contained on board A3. The mixer, which consists of two balanced modulators (Q2-Q3 and Q9-Q10), and a combiner (Q4-Q5), heterodynes the P-phase and Q-phase outputs of the VCO and the offset oscillator to produce a difference frequency of $\mathrm{F}_{\mathrm{o}}-\mathrm{F}_{\mathrm{d}}$. The operation of the mixer is expressed in the following trigonometric development.

Let $\theta=2 \pi F_{o} t$ be the phase of the $V C O$ and let $\tau=2 \pi F_{d t}$ be the phase of the offset oscillator. In terms of these variables, the $P$-phase and Q-phase outputs of the VCO can be written as $\cos \theta$ and $\sin \theta$ respectively, while the analogous quantities for the offset oscillator outputs are $\cos \tau$ and sin $\tau$. The first balanced modulator, $Q 2$ and $Q 3$, has an output proportional to the product of $\sin \theta$ sin $\tau$. The output of the second modulator $Q 9$ and Q 10 , is expressed as the product of $\cos \theta \cos \tau$.

Using a trigonometric identity, these two outputs can be expanded as follows:

$$
\begin{aligned}
& 2 \cdot \cos \theta \cos \tau=\cos (\theta+\tau)+\cos (\theta-\tau) \\
& 2 \cdot \sin \theta \sin \tau=-\cos (\theta+\tau)+\cos (\theta-\tau)
\end{aligned}
$$

When these two outputs are added together in combiner Q4 and Q5, certain terms cancel leaving the result $\cos (\theta-\tau)$ or a sinewave of frequency $\mathrm{F}_{0}$ - $\mathrm{F}_{\mathrm{d}}$. This is the desired clock input to the HF programmable divider.
4.3.2.2 HF PROGRAMMABLE DIVIDER. Refer to Figure 6-3. The high-speed programmable divider consists of four presettable decade counters $Z 8$ thru Z11. These counters operate in a nines-complement mode. Since overflow occurs at count 9999, the complement of the desired division ratio is preset into the dividers by the front panel switches. For example, a division ratio of 1492 is obtained when the nines-complement counters are preset to 8507 with the $10 \mathrm{MHz}, 1 \mathrm{MHz}, 100 \mathrm{KHz}$, and 10 KHz front panel frequency switches.

Because the Synthesizer must introduce a $\pm 9 \mathrm{MHz}$ differential between the dial readings and the actual output frequency $\mathrm{F}_{\mathrm{O}}$, the outputs of the 1 and 10 MHz switches are decoded to produce the appropriate offset. The offset decoding is accomplished using a combination of the wiring of the $1 / 10 \mathrm{MHz}$ switches and
the logic of a set of NAND/NOR gates. The plan of the receiver is such that for operating frequencies between $0-13 \mathrm{MHz}$ the dividers are preset to produce an $\mathrm{F}_{\mathrm{o}}$ signal which is 9 MHz above the operating frequency. The dividers are preset to produce an $\mathrm{F}_{\mathrm{o}}$ signal which is 9 MHz below the operating frequency in the range of $13-30 \mathrm{MHz}$.

The decoded preset bits corresponding to 10 MHz steps are set into $Z 8$, the first counter. Similarly, the preset bits corresponding to 1 MHz increments are set into 29 .

Since the 10 kHz and 100 kHz step counters are not involved in the 9 MHz IF offset, the front panel switches are wired directly to the counter $B C D$ preset inputs.

Table 4-1 lists the bits preset into each decade counter at the different HF frequency selector switch settings.

To compensate for the $20-30 \mathrm{kHz}$ offset introduced by the offset oscillator, the Q1 and Q2 outputs of 10 kHz divider $Z 11$ are wired into NAND gate $Z 6-B$ so that an output pulse is generated at the count of 9997 instead of the normal 9999. The output of $\mathrm{Z} 6-\mathrm{B}$ is inverted by $\mathrm{Z7}-\mathrm{B}$ to produce $\mathrm{a} \simeq 5 \mathrm{kHz}$ tachometer pulse train ( $\mathrm{F}_{\mathrm{th}}$ ) at the selected frequency.

Because the counters will not operate reliably at 22 MHz , the RF clock signal from the SSB mixer is divided by two in flip-flop 212 before application to the decade counters. Since the Fth output is 5 kHz , each increment in N corresponds to a 10 kHz shift in the VCO output frequency.

When the Synthesizer is locked on frequency, the tachometer repetition rate of approximately 5 kHz is continuously compared with the reference 5 kHz signal by the Pulse Phase Comparator to control the VCO frequency.
4.3.2.3 PULSE PHASE COMPARATOR. Refer to Figure 6-4. The pulse phase comparator produces an output control voltage which varies proportional to the phase difference of the tachometer signal ( $\mathrm{F}_{\mathrm{th}}$ ) and the reference pulse train ( $\mathrm{F}_{\mathrm{rh}}$ ). As F th gains in phase, the output voltage increases in the negative direction thus reducing the VCO frequency $\mathrm{F}_{\mathrm{o}}$.

The pulse phase comparator consists of tach pulse ramp generator Q1-Q2-Q3, differentiator Q8, differential amplifier Q4 thru Q7, sample and hold circuit C10-C11 and Q9, output amplifier Q10Q11, and loss of lock detector Q12-Q13 and SCR Q14.

Table 4-1. Decade Counter Preset Bits


1. Logic level 1 is $\simeq+5$ volts

Logic level 0 is $\simeq 0$ volts (gnd)
2. Inputs to $P_{0}, P_{1}, P_{2}$, and $P_{3}$ connections are $B C D$ preset inputs
3. Division factor is 9's complement of number preset into counter
4. No. column is decimal equivalent of preset number

The pulse phase comparator operates as a phase discriminator when the VCO is locked on frequency and as a broad range frequency discriminator when establishing lock during frequency changes. During normal operation, C10 is charged via Q6 and R10 and is reset by $Q 5$ when the sawtooth ramp at C7 turns on Q4. The result is a sawtooth waveform at C10 that is synchronized to the $\mathrm{F}_{\mathrm{th}}$ input.

The synchronizing $F_{t h}$ sawtooth is generated by ramp generator Q1-Q2-Q3. Q1 acts as a current source that linearly charges C7 toward ground potential. The ramp appearing on C7 is periodically reset to -12 volts by the positive pulses applied to the base of $Q 3$ from the tachometer input. During phase-lock the ramp on C7 charges up to within a few volts of ground which turns on $Q 4$ and, thereby, switches on Q5. Q5 discharges the ramp voltage on Clo.

Ripple at 5 kHz in the comparator output must be minimal to reduce sidebands in the Synthesizer output. This is achieved by the sample and hold circuit in the comparator. The reference clock pulses $F_{\text {th }}$ are differentiated by C6-R13 and amplified by Q8 to produce negative-going pulses of large amplitude which momentarily switch on FET Q9. When Q9 turns on, the instantaneous ramp voltage on C10 is transferred to C11. To further minimize ripple, charging of C10 is momentarily halted while Q9 is conducting so that C11 sees a constant voltage on C10. This is accomplished by switching off $Q 7$, which momentarily interrupts the flow of charging current through R10.

To prevent drift between sampling times, the voltage on C11 is monitored by a high impedance FET source follower Q10. Q11 provides amplification and level shifting required to interface the dc control level with the VCO input.

During frequency switching, large disparities can occur between $F_{\text {th }}$ and $F_{r h}$. Were these two frequencies to be compared in a simple phase discriminator, the result would be a rapidly varying phase signal which would average nearly to zero in the loop filter, and the loop would not lock up. To avoid this problem, the comparator operates as a broad range frequency discriminator while attempting to phase-lock.

If, during a change in switch settings, $\mathrm{F}_{\mathrm{th}}$ is substantially above $F_{\text {rh }}$, C7 is reset prematurely to -12 volts and $Q 4$ never switches on. Thus, C10 is not reset, and the voltage sampled by Q9 is consistently large and negative. This action forces the comparator output to rise negative and rapidly tune the VCO down in frequency as is required to reduce $\mathrm{F}_{\mathrm{th}}$.

If $F_{\text {th }}$ is substantially lower than $F_{r h}, Q 4$ and $Q 5$ remain conducting for substantial intervals holding C10 at a large positive potential. Thus, when Q9 samples C10, the positive voltage transferred to C11 holds the pulse phase comparator output near the positive limit of its voltage range which rapidly increases the frequency of the VCO.

In this way, gross frequency errors are quickly corrected. When the $F$ th and $F_{\text {rh }}$ signals near agreement, the comparator reverts to tha phase discriminator mode and phase-lock results.

To detect a loss of lock condition, a sample of the comparator phase-lock voltage is ac coupled through C14 to the base of Q12. In the frequency discriminator mode, the ac amplitude swing of the comparator output voltage reaches several volts causing Q12 to conduct, which turns on Q13. Q13 triggers SCR Q14, which turns on the LOSS OF LOCK indicator. Since the lamp supply voltage is the unfiltered output of the 5 -volt rectifier, this voltage goes to zero 120 times per second allowing the SCR to turn off after forward bias is removed from its gate input. A similar lamp driver in the LF Pulse Phase Comparator also turns on the LOSS OF LOCK lamp if the offset oscillator loses lock. In addition, the LOSS OF LOCK lamp is turned on when the OPER SBY switch is placed in SBY.

### 4.3.3 OFFSET OSCILLATOR (Figure 6-2)

The offset oscillator is a voltage-controlled oscillator that is tuned by either a phase-lock loop control voltage derived from the LF programmable divider setting or a voltage derived directly from the front panel VERNIER dial setting. The mode of control for the oscillator is selected by placing front panel switch S2 in the $1 \mathrm{KHz-100} \mathrm{~Hz}$ position to use the phase-lock loop or in the VERNIER position to use the VERNIER control.

The control voltage input linearly tunes the oscillator over a range of 80 to 120 kHz . The circuit consisting of Q11 thru Q14, and 22 form a RC relaxation oscillator. The oscillator drives a pair of J-K flip-flops (Z1) which divide the 80 to 120 kHz output by four to produce quadrature square wave outputs over a range of 20 to 30 kHz . The quadrature outputs are filtered by low-pass networks (R21-C9 and R22-C10) to produce approximate sinewave signals.

The oscillator uses $\mathrm{C} 12-\mathrm{C} 13$ as the reactive element to generate an output frequency proportional to RC. C12-C13 charges thru Z2-A at a rate determined by the control voltage generated in the phase-lock loop in the digital mode or by the impedance of vernier potentiometer 1 R3 in the VERNIER mode. By changing $R$
with 10 -turn 1 inear potentiometer 1 R3 the output frequency becomes a linear function of the shaft rotation. By changing the effective $R$ with the control voltage input, the frequency becomes a function of the division ratio $N$ selected by the 1 KHz and 100 Hz switch settings.

The negative-to-positive ramp buildup at C12-C13 is compared with the voltage at the junction of constant current source $22-B$ and R36 across the emitter-base junction of Q12. When the positive-going charge at C12 drops below the negative voltage at the base of Q12, Q12 turns on. The collector drop at Q12, turns on Q13 which causes Q12 to saturate. The negative current thru Q12 quickly returns C12 to a full negative charge and automatically turns off. A short negative pulse is produced at the junction of Q13 and R36 during this reset operation.

These pulses are coupled to the base of Q11 by C20 and momentarily turn off Q11. The positive output pulses drive divide-by-four flip-flops $Z 1-A$ and $B$. The control voltage input in either mode linearly adjusts the output pulse rate by changing the charge rate of C12.

In the VERNIER mode, trim potentiometer 229 adjusts the oscillator center frequency and trim potentiometer R30 adjusts the oscillator range at the extreme ends of the control range. In the digital mode, potentiometer R 2 on the LF programmable divider adjusts the phase-lock voltage input to the offset oscillator. Since there is interaction between these trim controls, a tuning procedure is provided in Section 5.

### 4.3.4 LF PHASE-LOCK LOOP

The LF phase-lock loop contains a programmable divider and a pulse phase comparator. The LF phase-lock loop is similar to the HF Phase-Lock Loop in that the offset oscillator output ( 80 to 120 kHz ) is divided by a programmable divider and compared to a reference frequency to produce a stable phase-lock loop at any selected output frequency.
4.3.4.1 LF PROGRAMMABLE DIVIDER. Refer to Figure 6-5. The LF divider consists of three decade dividers $\mathrm{Z} 1, \mathrm{Z} 2$, and $\mathrm{Z3}$ contained on board A7. The dividers are programmable, modulo-
 in a manner similar to the HF dividers. However, the LF modules operate in a 1's complement mode instead of a 9's complement mode. Thus, the binary preset inputs to the modules match the desired division factor (i.e., preset binary 8 produces a division of 8). The counters produce division factors between 200 and 299 .

Table 4-2 lists the bits preset into each counter at different settings of the selector switches. The last counter module $Z 3$ is hard-wired to produce a division of 200.

Table 4-2. LF Divider Preset Bits

| 1 KHz Dial |  |  |  |  |  |  | 100 Hz Dial |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Dial <br> Setting | Z2 | $\begin{gathered} \text { Preset } \\ \text { Bits } \\ \div 20 \div 40 \end{gathered}$ |  | $\div 80$ | $\begin{gathered} \text { Decimal } \\ \text { No. } \end{gathered}$ |  | $\begin{aligned} & \text { Dial } \\ & \text { Settings } \end{aligned}$ | $\begin{gathered} \text { z1 Preset } \\ \text { Bits } \\ \div 1 \div 2 \div 4 \div 8 \end{gathered}$ |  |  |  | $\begin{gathered} \text { Decimal } \\ \text { No. } \end{gathered}$ |  |
| 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 |
| 1 | 1 | 0 | 0 | 0 |  | 1 | 1 | 1 | 0 | 0 | 0 |  | 1 |
| 2 | 0 | 1 | 0 | 0 |  | 2 | 2 | 0 | 1 | 0 | 0 |  | 2 |
| 3 | 1 | 1 | 0 | 0 |  | 3 | 3 | 1 | 1 | 0 | 0 |  | 3 |
| 4 | 0 | 0 | 1 | 0 |  | 4 | 4 | 0 | 0 | 1 | 0 |  | 4 |
| 5 | 1 | 0 | 1 | 0 |  | 5 | 5 | 1 | 0 | 1 | 0 |  | 5 |
| 6 | 0 | 1 | 1 | 0 |  | 6 | 6 | 0 | 1 | 1 | 0 |  | 6 |
| 7 | 1 | 1 | 1 | 0 |  | 7 | 7 | 1 | 1 | 1 | 0 |  | 7 |
| 8 | 0 | 0 | 0 | 1 |  | 8 | 8 | 0 | 0 | 0 | 1 |  | 8 |
| 9 | 1 | 0 | 0 | 1 |  | 9 |  | 1 | 0 | 0 | 1 |  | 9 |

Notes:

1. Divider 23 preset inputs are fixed at 0100 or decimal 2
2. Logic level 1 is $\simeq+5$ volts

Logic level 0 is $\simeq 0$ volts (gnd)
3. Division factor is 1's complement of number preset into counters

The net result at the output of the divider is approximately a 400 Hz tach signal $\mathrm{F}_{\mathrm{t}}$ when the offset oscillator is locked on. The $\mathrm{F}_{\mathrm{t}}$ output is compared to a 400 Hz reference clock Frl by the LF Pulse Phase Comparator. The comparator produces the required phase-lock voltage which holds the offset oscillator on frequency.
4.3.4.2 LF PULSE PHASE COMPARATOR. Refer to Figure 6-6. The LF pulse phase comparator produces a control voltage which varies proportional to the phase relationship of the tachometer signal $\mathrm{F}_{\mathrm{t}}$, and the reference signal $\mathrm{F}_{\mathrm{rl}}$. The control voltage increases in a negative direction as $\mathrm{F}_{\mathrm{tl}}$ gains in phase.

The LF comparator uses the same board as the HF Comparator with component values to match the lower frequency operation. The board is designated A8 and consists of tach pulse ramp generator Q1-Q2-Q3, differentiator Q8, differential amplifier Q4 thru Q7, sample and hold circuit C10-C11 and Q9, output amplifier Q10-Q11, and loss of lock detector Q12-Q13 and SCR Q14.

The negative control voltage output from the comparator is returned to an electronic vernier circuit on the LF divider board A7. The attenuator consists of FET stage Q1, fixed resistances which are selected by the 1 KHz switch, and adjustment potentiometer R2. The conduction of Q1 is controlled by the comparator output to control the net positive voltage applied to the fixed resistances. As the phase difference between $F_{t l}$ and $F_{r l}$ increases the comparator output rises negative causing Q 1 to conduct more. This lowers the current flow to the offset oscillator with the result that C12-C13 in the oscillator charges slower which reduces the output frequency.

### 4.3.5 FREQUENCY STANDARD (Figure 6-7)

The frequency standard board A6 produces a 5 kHz reference signal $F_{r h}$ and a 400 Hz reference signal $\mathrm{F}_{\mathrm{rl}}$ for comparison with the two phase-lock loop tachometer signals $\mathrm{F}_{\mathrm{th}}$ and $\mathrm{F}_{\mathrm{t}}$, respectively.

The frequency standard consists of a 4 MHz crystal oscillator module TCXO, $\mathrm{a} \div 100$ counter $Z 1-Z 2$, $\mathrm{a} \div 8$ counter $Z 3-\mathrm{A}$, and another $\div 100$ counter $Z 3-Z 4$. The additional $\div 2$ counter $23-B$ is not used.

The TCXO module mounts on the component side of frequency standard board A6. Different options are offered depending on the stability required over the temperature range of the Synthesizer. The following options are currently offered.

| FEC Part No. | FREQUENCY STABILITY | TEMPERATURE RANGE | AV. PPM/ ${ }^{\circ} \mathrm{C}$ |
| :---: | :---: | :---: | :---: |
| B1690-1 | $\pm 1 \mathrm{PPM}\left(1 \times 10^{-6}\right)$ | 00 to 500 C | $4 \times 10^{-8} / 0 \mathrm{C}$ |
| B1690-2 | $\pm 1 \mathrm{PPM}$ | 00 to 250 C | $4 \times 10^{-8} / 0 \mathrm{C}$ |
|  | $\pm 0.5 \mathrm{PPM}\left(5 \times 10^{-7}\right)$ | $25^{\circ}$ to $50^{\circ} \mathrm{C}$ | $2 \times 10^{-8} / 0 \mathrm{C}$ |
| B1690-3 | $\pm 0.5 \mathrm{PPM}$ | $0^{\circ}$ to $50^{\circ} \mathrm{C}$ | $2 \times 10^{-8} / 0 \mathrm{C}$ |

Options can be ordered with stability up to the state of the art limit of $\pm 0.3 \mathrm{PPM}\left(3 \times 10^{-7}\right)$ or an average $\mathrm{PPM} /{ }^{\circ} \mathrm{C}$ of $1.2 \times 10^{-8} \mathrm{I}^{0} \mathrm{C}$ over the temperature range of 00 to $50^{\circ} \mathrm{C}$. Option B1690-2 offers optimum performance versus cost and is installed if the customer has no optional requirements.

The first $\div 100$ counter $21-22$ and the $\div 8$ counter $23-A$ are connected in series to provide the 5 kHz reference signal $\mathrm{F}_{\text {rh }}$ to the HF Pulse Phase Comparator. The two $\div 100$ counters are connected in series to provide the 400 Hz reference signal $\mathrm{F}_{\mathrm{r}}$ to the LF Pulse Phase Comparator.

An optional jumper position on the board permits selection of either a 5 kHz or a 25 kHz output from $25-\mathrm{A}$ but the 25 kHz position is not used in the 1550A.
4.3.6 POWER SUPPLY (Figure 6-8)

The Model 1550 A uses +5 volts for the IC logic circuits and $\pm 12$ volts for the analog circuits. The power supply utilizes operational amplifiers to regulate these output voltages against load and line variations.

The +12 volt output is referenced to zener diode CR7 which receives pull-up current from the +12 volt output through R9. CR7 holds the non-inverting input of 21 at a fixed voltage. The inverting input is obtained from the +12 volts via precision divider R3-R5. A Darlington pair consisting of Q1 and Q2 serves as the current passing element.

The - 12 volt supply is referenced to the +12 volt operational amplifier $Z 2$ and voltage divider R10-R11. The +5 volt output is referenced to the +12 volt output by 23 .

Since greater currents are required from the 5 -volt supply this supply contains a choke input filter.

RF bypass capacitors across each of the rectifier diodes prevent these diodes from presenting a variable RF impedance to the VCO which could produce unwanted frequency pulling.

## SECTION V

MAINTENANCE

### 5.1 GENERAL

The maintenance information presented in this Section will help assigned personnel to keep the Synthesizer in proper operating condition. Since the Synthesizer is a low level, solid-state device, no preventive maintenance is recommended. Service technicians should possess a thorough understanding of the Synthesizer operation before attempting corrective maintenance.

## WARNING

The rear portion of the Synthesizer chassis and power supply board A1 contains ac voltages as high as 230 volts. THESE VOLTAGES ARE ALWAYS HAZARDOUS TO LIFE. Exercise extreme caution in these areas.

### 5.2 CORRECTIVE MAINTENANCE

Corrective maintenance involves observation of the operating conditions of the Synthesizer to localize a malfunction. To assist the technician in detecting a malfunction a Minimum Performance Procedure is provided which will usually indicate a malfunctioning unit. A Troubleshooting Chart is also provided to help localize a malfunction to a specific circuit.
5.2.1 REQUIRED TEST EQUI PMENT

The following test equipment or its equivalent is required to service the Synthesizer.

Table 5-1. Required Test Equipment

| EQU I PMENT | MANUFACTURER \& TYPE |
| :---: | :---: |
| AF VTVM | HP 400 |
| VOM | Triplett 630 |
| Oscilloscope | Tektronix 453 |
| Frequency Counter | HP 5245L |
| Attenuator | Kay 30-0 |
| Spectrum Analyzer | HP141T + 8552B + 8553 B |
| Variac | Powerstat VS3PN116B |
| Small Non-Inductive Tuning Tool | N.A. |
| Dummyload (Coaxial $50 \Omega, 1 / 2 \mathrm{~W}$ connected to a BNC) | N.A. |

Before starting the Minimum Performance Tests, be certain that the HP5245L Counter is turned of for at least 72 hours and the Synthesizer is turned on for at least 1 hour.
5.2.2 MINIMUM PERFORMANCE TEST.

Proceed as follows:

1. Connect test equipment as shown in Figure 5-1. Set variac to approximately 115 vac.
2. Rotate frequency selector switches and VERNIER control to 00.0000 MHz settings. Set mode switch to $1 \mathrm{KHz}-100 \mathrm{~Hz}$ position. Check that output is $9.0000 \mathrm{MHz} \pm 3 \mathrm{~Hz}$.
3. Slowly change variac setting between 105 and 125 vac. Check that output remains stable and within frequency tolerance at both OUTPUT 1 and OUTPUT 2. Return variac to 115 vac position.
4. Set mode switch to VERNIER position. Check that output is $9.000 \mathrm{MHz} \pm 100 \mathrm{~Hz}$. Repeat step 3 .
5. Rotate frequency selector switches and VERNIER control to 13.0005 MHz settings. Set mode switch to $1 \mathrm{KHz}-100 \mathrm{~Hz}$ position. Check that output frequency is $4.0005 \mathrm{MHz} \pm 3 \mathrm{~Hz}$. Repeat step 3.
6. Set mode switch to VERNIER position. Check that output is $4.0005 \mathrm{MHz} \pm 100 \mathrm{~Hz}$. Repeat step 3 .
7. Rotate frequency selector switches and VERNIER control to 12.9999 MHz settings. Set mode switch to $1 \mathrm{KHz}-100 \mathrm{~Hz}$ position. Check that output frequency is $21.9999 \mathrm{MHz} \pm 3 \mathrm{~Hz}$. Repeat step 3.
8. Set mode switch to VERNIER position. Check that output is $21.9999 \mathrm{MHz} \pm 100 \mathrm{~Hz}$. Repeat step 3 .
9. If the signals at OUTPUT 1 or OUTPUT 2 disappear or deteriorate, or if phase-lock cannot be maintained, the unit is defective. See paragraph 5.2.3 for troubleshooting information.
10. If Synthesizer is substantially out of tolerance the unit may require alignment. The unit can also lose phase-lock if it is substantially out of alignment. See paragraph 5.2.4. for alignment information.

### 5.2.3 TROUBLE ISOLATION

The technician will frequently detect obvious faults such as cracked or burned resistors, swollen capacitors, or burned insulation by beginning his troubleshooting routine with a visual inspection. Table 5-2 lists the probable causes of phsical damages common to different electronic components.

Follow the visual inspection by measuring the Power Supply voltages at board 1Al (N0917). With a nominal 115 vac or 230 vac input, the dc supply voltages should be as follows:
MEASUREMENT LEVEL
POINT

Pin 4 of $\mathrm{J} 4 \quad+12$ to +13.5 volts with ripple of less than 4 millivolts RMS

Pin 2 of J3 -12 to -13.5 volts with ripple of less than 4 millivolts RMS

Pin 1 of $\mathrm{J} 2 \quad+5$ volts $\pm .5$ volts with ripple of less than 4 millivolts RMS

Table 5-2. General Inspection Procedures

| COMPONENT | CONDITION | CAUSE | CORRECT ION |
| :---: | :---: | :---: | :---: |
| Resistors | Discolored, swollen, or cracked Cracked or broken | Overheated due to overload <br> Improper handling | Locate and correct overload condition. Replace resistor. |
| Capacitors | Leakage, bulging, split case, or broken end seals | Physical damage <br> or dielectric <br> breakdown due to high <br> voltage or improper handling | Check for high voltage condition and repair. Replace capacitor. |
| Transformers | Discolored insulation or windings, leakage | Overheated due to current overload | Locate and correct overload. Replace transformer if destroyed. |
| Connectors and jacks | Bent pins, charred insulation, marred threads, moisture, dirt, or grease | Improper handling | Straighten pins, clean or replace part. |
| Switches and controls | Broken, worn, bent, or dirty | Rough handling or normal wear | Clean, straighten, or replace. |
| Indicator <br> lamps | Broken <br> Burnt out | Rough handling, excessive current, or normal wear | Replace lamp. |
| Wiring and cables | Cut or frayed insulation, broken wires or connections | Improper handling | Repair or replace. |
| Solder connections | Loose or corroded connections, cold solder joints | Improper soldering | Clean and resolder. |

If the visual or voltage checks do not reveal the trouble, proceed with Table 5-3 Trouble Isolation Chart. The Trouble Chart uses a Symptom, Malfunction, Probable Cause approach to isolate a trouble to the possible defective circuits. After the trouble is isolated to a circuit, use the schematic diagrams and an oscilloscope to locate the exact trouble. Use the waveforms shown on the schematics to test the important points in each circuit.

### 5.2.4 ALIGNMENT

The Synthesizer is carefully aligned at the factory with precision test equipment. Realignment will be necessary only if the Synthesizer is tampered with or component parts are replaced. Before attempting to align a malfunctioning Synthesizer always investigate and eliminate all other possible causes for the malfunction. Only qualified technicians should ever align the Synthesizer.

## NOTE

Alignment is a last resort, not a method of troubleshooting.

Figure 5-2 shows the location of the various test and adjustment points. To begin alignment place the Synthesizer in a test location convenient to the required test equipment. Remove top cover from unit. Also remove RF shield from VCO board 1A5 (N0920).

Before attempting to align the Synthesizer, be certain that test equipment and unit have been turned on for at least 1 hour.

NOTE
HP5245L counter must be turned on for at least 72 hours before the Frequency Standard Adjustment can be performed.
5.2.4.1 FREQUENCY STANDARD ADJUSTMENT. Proceed as follows:

1. Connect frequency counter to Jl on the rear panel. Remove cover screw from TCXO module located on FREQ STD board A6 (N0980).
2. Set frequency selector switches to 12.0000 MHz settings. Set mode switch to $1 \mathrm{KHz-100} \mathrm{~Hz}$ position.
3. Adjust TCXO for an output frequency of $21.000 \mathrm{MHz} \pm 1 \mathrm{~Hz}$.
4. Replace cover screw in TCXO and disconnect frequency counter.

Table 5-3 Trouble Isolation Chart

| SYMPTOM | MAL FUNCT I ON | PROBABLE CAUSE |
| :---: | :---: | :---: |
| 1. No signal at OUTPUT 1 (R1 control full clockwise). Normal signal at OUTPUT 2. | Q-phase output circuit defective. | a. Isolation amplifier circuit on NO 920 defective. <br> b. Level potentiometer 1R1 or output connection defective. |
| 2. No signal at OUTPUT 2 (R2 control full clockwise). Normal signal at OUTPUT 1. | P-phase output circuit defective. | a. Isolation amplifier circuit on N0920 defective. <br> b. Level potentiometer 1R2 or output connection defective. |
| 3. No signal at OUTPUT 1 or OUTPUT 2 (R1 and R2 controls full clockwise). | VCO circuit not operating. | a. OPER-SBY switch in SBY. <br> b. VCO circuit on N0920 defective. <br> c. HF phase comparator output from N0921 defective. |
| 4. OUTPUT frequency approximately 10\% higher than selected frequency at all dial settings | Frh reference signal is not sampling phase comparator. | a. Frequency standard board N0980 defective. <br> b. Frh differentiator circuit on phase comparator board N0921 defective. <br> c. Sampling circuit on HF phase comparator board N0921 defective. |

Table 5-3. Trouble Isolation Chart (cont.)

| SYMPTOM | MALFUNCTION | PROBABLE CAUSE |
| :---: | :---: | :---: |
| 5. Output frequency approximately 27 MHz $( \pm 2 \mathrm{MHz}$ and unstable) at all frequency dial settings. | VCO not receiving control voltage from HF pulse phase comparator. | a. Mixer circuit on N0922 defective. <br> b. Divider circuit on N0918 not producing $\mathrm{F}_{\mathrm{th}}$. <br> c. Ramp generator circuit on HF phase comparator board N0921 defective. <br> d. Differential amplifier on HF phase comparator board N0921 defective. |
| 6. Output frequency 20-30 kHz low but stable at all dial settings. VERNIER or $1 \mathrm{KHz}-100 \mathrm{~Hz}$ mode. | Offset oscillator signal is not present at mixers. | a. Offset oscillator circuit on N0922 defective. <br> b. $\div 4$ counter on N0922 defective. |
| 7. One or more dial settings of the $10 \mathrm{MHz}, 1 \mathrm{MHz}$, 100 KHz or 10 KHz switches produces incorrect output frequencies. Other dial settings are normal. | Dividers not operating correctly on defective dial settings. | a. HF divider circuit on N0918 defective. <br> b. Switch connections to dividers on N0918 unsoldered or broken. |

Table 5-3. Trouble Isolation Chart (cont.)

| SYMPTOM | MALFUNCTION | PROBABLE CAUSE |
| :---: | :---: | :---: |
| 8. In $1 \mathrm{KHz-100} \mathrm{~Hz}$ mode only, output frequency 20-30 kHz low but stable at all dial settings. VERNIER mode normal. | Offset oscillator not receiving any phase-lock voltage. | a. Electronic vernier <br> Q1 on N0919 is shorted. <br> b. Phase-lock voltage connection to offset oscillator broken. |
| 9. Output frequency approximately 1 kHz off frequency and unstable at all settings of the 1 KHz and 100 Hz switches. Other switches change output frequency by correct amount. | LF phase-1ock loop not functioning properly. | a. LF divider N0919 not producing $\mathrm{F}_{\mathrm{t}}$ pulses. <br> b. Ramp generator on LF phase comparator N0983 defective. <br> c. Differential amplifier on LF phase comparator N0983 defective. <br> d. Frequency standard signal $\mathrm{F}_{\mathrm{rl}}$ defective. <br> e. Frisampling circuit on LF phase comparator N0983 defective. |
| 10. One or more dial settings of the 1 KHz or 100 Hz switches produces incorrect output frequencies. Other dial settings are normal. | Dividers not operating correctly on defective dial settings. | a. LF divider circuit on N0919 defective. <br> b. Switch connections to dividers on N0919 unsoldered or broken. |

### 5.2.4.2 OFFSET OSCILLATOR ADJUSTMENT. Proceed as follows:

a.Vernier Mode

1. Connect frequency counter to TP1 on MIXER/OSC board 1A3 (N0922). Set mode switch to VERNIER position.
2. Rotate VERNIER dial to setting 10. Adjust CENTER FREQUENCY potentiometer R29 for a frequency of $30,020 \mathrm{~Hz} \pm 10 \mathrm{~Hz}$.
3. Rotate VERNIER dial to setting 00 . Adjust RANGE potentiometer R30 for a frequency of $19,980 \mathrm{~Hz} \pm 10 \mathrm{~Hz}$.
4. Since the two adjustments interact, repeat Steps 2 and 3 until both frequencies are within the stated tolerance.

NOTE
Rotating R29 clockwise increases oscillator center frequency; rotating R30 clockwise decreases the range covered by VERNIER dial and increases oscillator frequency.
b. Digital Mode

1. Connect VOM to J2 pin 1 on LF Programmable Divider board 1A7 (N0919). Set mode switch to $1 \mathrm{KHz-100} \mathrm{~Hz}$ digital position.
2. Set 1 KHz and 100 Hz selector switches to 0 positions.
3. Adjust $R 2$ on board $1 A 7$ for exactly +4.0 vdc on VOM.
5.2.4.3 VCO ADJUSTMENT. Proceed as follows:
4. Connect test equipment as shown in Figure 5-3. Adjust $R 2$ on rear panel to full counterclockwise position.
5. Rotate AGC potentiometer R18 on N09 20 to approximately center position. Rotate WAVEFORM potentiometer R75 on N0920 to full clockwise position.
6. Adjust R75 counterclockwise until LOSS OF LOCK indicator just goes off. Rotate front panel 1 MHz control through positions 0-9 and check that indicator stays off.
7. Tune Synthesizer to $12.0000 \mathrm{MHz}(21,000,000 \mathrm{~Hz}$ output).
8. Adjust R18 for a $1.05 \pm .05$ volt peak-to peak level on oscilloscope. Move dummy load and oscilloscope to Jl and adjust R1 (on rear panel) for a $1.05 \pm .05$ volt peak-to-peak level.
9. Disconnect oscilloscope and dummy load.
5.2.4.4 VCO HARMONIC/SPURIOUS OUTPUT TESTS. Proceed as follows:
10. Connect test equipment as shown in Figure 5-4.
11. Set spectrum analyzer for $0-100 \mathrm{MHz}$ scan width with a scan time of 0.1 seconds or slower. Monitor VCO output with analyzer while changing the 10 MHz and 1 MHz switch settings between 4 to 21 MHz in 1 MHz increments. Observe that the harmonic/spurious outputs are below the primary output by the following amounts:
a. 2nd/3rd harmonics down at least 31 db .
b. 4th and higher harmonics down at least 36 db .
c. Any spurious outputs down at least 55 db .
12. Rotate frequency selector switches and VERNIER control to 12.0000 MHz settings ( $21,000,000 \mathrm{~Hz}$ output).
13. Set analyzer for a 1 kHz bandwidth, a 10 kHz per division scan width, and a 0.2 second per division scan time. Observe that the 20 kHz sidebands are at least 55 db below primary output frequency.
14. Switch spectrum analyzer and counter connections on output connectors and repeat Steps 2 thru 4.

### 5.2.5 REPAIR PROCEDURES

The 1550 A Synthesizer is designed for ease of subassembly removal and installation and will pose no problems for an experienced technician. Replacement of component parts is also routine with the exception of the front panel VERNIER control. The VERNIER control must be removed and replaced as discussed in paragraph 5.2.5.1 to prevent loss of dial calibration.

### 5.2.5.1 REPLACING THE VERNIER CONTROL. Proceed as follows:

1. Rotate VERNIER dial to 0 position. Remove \#4-40 HOLDING SCREW from clip on inside rear of chassis. Using . 050 HEX KNOB WRENCH attached to clip on inside rear of chassis, unscrew either \#4-40 Allen set screw 1 turn. DO NOT rotate set screw more than 1 full turn. Insert holding screw in set screw slot and tighten. If holding screw will not catch, tighten set screw $1 / 2$ turn and insert set screw.
2. Loosen second \#4-40 Allen set screw and remove VERNIER dial. Dial will require light pressure to remove from keyway and shaft.
3. If only VERNIER dial is being replaced, proceed to Step 7. If potentiometer is being replaced, proceed to Step 4.
4. Unsolder and remove wires connected to potentiometer. 1R3. Mark position of each wire as it is removed.
5. Remove nut, washer, and snap-on assembly holding potentiometer to front panel and remove potentiometer. Install new potentiometer and secure to panel. Be certain that lugs on potentiometer are canted to side toward board N0922 in order to clear the top cover.
6. Connect and solder wires removed in Step 4 to new potentiometer. Rotate potentiometer shaft to its counterclockwise stops.
7. Slide VERNIER dial onto potentiometer shaft until it rests lightly against front panel. Apply light pressure and rotate knob COUNTERCLOCKWISE until index seats in keyway.

## CAUTION

## DO NOT ROTATE CLOCKWISE:

8. Press knob into keyway to seat assembly. A slight snap will indicate proper seating.
9. Tighten Allen set screw not containing holding screw. This locks VERNIER dial to the potentiometer shaft. Remove \#4-40 holding screw from dial and tighten \#4-40 Allen set screw.

NOTE
If a new VERNIER dial is installed, \#4-40 set screw must be inserted after holding screw is removed.
10. Replace holding screw and Allen wrench in HOLDING SCREW and HEX KNOB WRENCH clips on inside rear of chassis. If potentiometer was replaced, perform the Vernier Adjustment procedures discussed in paragraph 5.2.4.2.


Figure 5-1. Connections For Minimum Performance Tests


Figure 5-2. Board Locations Ariu Adjustment points


Figure 5-3. Connections For VCO Adjustments


Figure 5-4. Connections For VCO Harmonics/Spurious Output Tests

## SECTION VI

## SCHEMATIC DIAGRAMS


3. UNLESS OTHERWISE NOTED:
inducters arf in microhenties.

4. TRANSISTORS $Q 2$, Q3, QS AND Q6 ARE B1686-1,

AND ARE MARKED WITH BROWN COLOR DOT AND ZN5459.
5. TRANSISTORS Q4 AND Q7 ARE BI686-2 AND
ARE MARKED WITH RED COLOR DOT AND $2 N 5459$.
6. TAANSISTOR Q SYMBOLS, QI AND Q8 NOT USED.

Figure 6-1, Sheet 1. Main Voltage-Controlled Oscillator Schematic Diagram D2172B


Figure 6-1, Sheet 2. Main Voltage-Controlled Oscillator Schematic Diagram D2172B


Figure 6-2. SSB Mixer/Offset Oscillator Schematic Diagram D2171C


Figure 6-3. HF Programmable $\underset{\substack{\text { Divider } \\ \text { D2170 }}}{ }$


Figure 6-4. HF Pu1se Phase Comparator Schematic Diagram D2179C


Figure 6-5. LF Programmable Divider Schematic Diagram


Figure 6-6. LF Pulse Phase Comparator Schematic Diagram D2282


## - NOTES.

1. REF DESIG PREFIX 1 A6.
2. P.C. BOARO REF: NO. 980
3. P.C. BOARD ASS'Y REF: C246O
4. OUTPUT FREQUENCY:

1550A-5kHz
1575-25kHz
5. SEE BIG90 FOR FREQUENCY STANDARD TEMPERATURE STABILITH OPTIONS.


Figure 6-7. Frequency Standard Schematic Diagram C2461


Figure 6-8. Power Supply Schematic Diagram D2169B

NOTES:
I. WIRE LEGEND (A) RGI74/U COAXIAL CABLE (B) NO 24 TWISTED SHIELDED PAIR (C) NO24 STRANDED WITH PVC INSULATION (E) NO18 BUS, TINNED NO 24 TWISTED, SHIELDED, 3 CONDUCTOR 2. ROUTE WIRES \& CABLING AS SHOWN. DO NOT LACE CABLES I\& TOGETHER. UNCABLED (A) WIRES TO BE AS SHORT AS POSSIBLE
3. DENOTES MALE PIN IN PLUG.

O DENOTES FEMALE PIN IN PLUG.
4. AFTER ASSEMBLY SOLDER PINS ON ALL (A) WIRES TO INSURE GOOD RF CONNECTION.


Figure 6-9. Mode1 1550A Chassis Wiring Diagram

## SECTION VII

PART REPLACEMENT DRAWINGS


Figure 7-1. Model 1550A Assembly


Figure 7-1. Parts List


Figure 7-2. Power Supply P.C. Board Assembly 1A1 D2164B


Figure 7-2. Parts List


Figure 7-3. HF Programmable Divider P.C. Board Assembly 1A2 D2165C


Figure 7-3. Parts List

NOTES:


Figure 7-4. SSB Mixer/Offset Oscillator P.C. Board Assembly 1A3 D2166C

| 1 I | 1 | I |  |  | 1 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| I |  |  | I |  | 1 |  |  |
| 11 | I | 1 | 1 |  | 1 |  |  |
| 1 | 1 | 1 | 1 I |  | I |  |  |
| I | I | 1 |  |  | I |  |  |
| 1 | 1 | I | 1 |  | I |  |  |
| I | I | 1 |  |  | 1 |  |  |
| 1 | 1 | I | 1 |  | 1 |  |  |
| 1 | 1 | I | I 1 |  | 1 |  | ) |
| 1 I | I | I | 1 I |  | I |  |  |
| 1 I | 1 | , | 1 |  | I |  |  |
| 1 1 | I | \| |  |  | , |  |  |
| 1 | I |  |  |  | 1 |  |  |
| 1 | 1 | I |  |  | 1 |  |  |
| 1 I | I | I | 1 |  | 1 |  |  |
| I | I |  |  |  | I |  |  |
| I | I |  |  |  | 1 |  |  |
| 1 | \| |  |  |  | I |  | I |
| $42 \mid 31$ | \| DD-3.9 | | I INDUCTOR 3.9 MICROHENRIES \| | \|NYTRONKS $\mid$ |  | 1 |  | \| |
| 41111 | \|RN600 1782F| | \|RESISTOR, $17.8 \mathrm{~K} \quad 1 / 4 \mathrm{~W} / 7.1$ | $\mid$ CGW \| |  | 1 |  |  |
| 40\| 1 1 | \| RN60D 4991 F | | \|RESISTOR, 4.99 K 1/4W $1 \%$ \| | $1 \mathrm{C} ; \mathrm{V}$ |  | 1 |  |  |
| 39111 | \|RN6002432F| | \|RESISTOR1 $24.3 \mathrm{~K} / 4 \mathrm{~W} / \mathrm{C} \mathrm{\%}$ | CGW |  |  |  |  |
| \| 38 |/1/R| | \| 46410 | | 1 GRIPLET | DERE |  | , |  |  |
| 371/5 | \|A62-3-ET | | I STAKE PIN. MALE \| | \|BEAD 2 $^{\text {HA/N] }}$ |  | \| |  | I |
| $361 / 01$ | $\|M 93-102-E T\|$ | I STAKE PIN. FEMALE I | \|OEAD CHAI/N $\mid$ |  | 1 |  | I |
| 35141 | \| $1246-12 \mid$ | I STANDOFF | CTC 1 |  | 1 |  |  |
| $341 / 1$ | 1TD 401 | IINT. CKT. DUAL TRANSISTOR I | \| SPRAGULE | |  |  |  |  |
| $331 / 1$ | \|SN/58093N | | I/NTEGRATED CIRCUIT | INATIONAL |  | I |  |  |
| $321 / 1$ | 166 WR $5 K$ | \|POTENTIOMETER, 5 K | | \|BECKMAN | |  | 1 |  |  |
| 3/1/1 | 166 WR2K | PPOTENTIOMETER. 2 K | [BECKMAN \| |  | 1 |  | 1 |
| 30121 | \|RN6001001F | | \|AESISTOR. $1 \mathrm{~K} .1 / 4 \mathrm{~W}, 1 \%$ \| | 1 CGw |  | 1 |  | 1 |
| 291/ 1 | \|AN600243/F | | $142.43 \mathrm{~K}: 1 / 4 \mathrm{~W}, 1 \%$ \| | 106W |  | 1 |  | \| |
| 28131 | 19COT6F330J 1 |  | $1 A B$ |  | 1 |  | I |
| 27121 | $11103 \mathrm{~J} \mid$ | 110.41 | 4 |  | 1 |  | 1 |
| 2611 | 111 | 1 1 1 1 1 |  |  | I |  | 1 |
| 25111 | 11473.01 | 474 1 |  |  | I |  |  |
| 24141 | \| $14710 \mid$ | $470 \Omega$ |  |  | 1 |  |  |
| 23121 | $1133 / 41$ | 1 1-330 |  |  | 1 |  | I |
| 221/1 | 1122 l | 11.2 K |  |  |  |  |  |
| 21121 | 1168101 | 111 |  |  | 1 |  | I |
| 20141 | 11231 | $112 \pi$ |  |  | 1 |  |  |
| 19121 | $11683 \mathrm{~J} \mid$ | 1158 |  |  |  |  |  |
| $18\|2\|$ | 1 \| 474J| | 470K |  |  |  |  |  |
| 17121 | 11392 l |  | P |  | 1 |  | I |
| $16\|3\|$ | \| AC016F102J | | \|AES/STOR. 1 K. $/ 1 / 4 \mathrm{~W}, 5 \%$ \| | AB |  |  |  | I |
| $151 / 1$ | \|PCR 700:00068 | | \|CAPACITOR, 00068 MF 27.50 V | | \| PAKTRON | |  | 1 |  | 1 |
| $14\|4\|$ | $12 N 5459$ | \| TAANSISTOR, FET, 1 CHAN | | \|motosola I |  |  |  |  |
| $13\|2\|$ | $12 N 5461$ | 1 FET P CHAN 1 | \|nororo: ${ }^{\text {\| }}$ \| |  | 1 |  |  |
| 12141 | \| 2N3904 | | 1 NPN 1 | \| Natloval |  |  |  | 1 |
| $\left.11\right\|^{2} \mid$ | $12 N 3906$ | \|TRANSISTOR, PNP | | \|NATIONAL | |  |  |  |  |
| 10111 | \|5082-2810 | | I DIODE, HOT CARRIER | HP |  |  |  |  |
| $9\|3\|$ | 1/500106190208才 | ICAPACITOR, 10 MFD 20 VI | \|SPRAGUE |  |  |  |  |
| 8191 | 15835 \% 54i03z 1 |  | \| ER/E |  | 1 |  | 1 |
| $71 / 1$ | [CMO6FD82IG03] | 18820.9 F 29500 V | \| ELMENCO 1 |  | I |  |  |
| 6121 | \| 0 M-15-47/J | | 11470 PF, $5 \% .500 \mathrm{VI}$ | \|ELME,VCO| |  | 1 |  | 1 |
| 511 | 1 1 |  | 1 1 |  |  |  |  |
| 4121 | 10M-15-330才 \| | $1 \mathrm{l} 3 \mathrm{pF}, 5 \%, 500 \mathrm{~V}$ | \|ELMENCO | |  | I |  | 1 |
| 3141 | 1/500105 $\times 9015421$ | 1 l 1MFD 15 V \| | $\mid$ SpragiJe \| |  | 1 |  | 1 |
| $2\|3\|$ | 10M-15-680J \| | \|CAPACITOR. 68 PF, $5 \%, 500 \mathrm{~V}$ \| | \|ELIAEIVCO| |  | 1 |  |  |
| 1 1 1 1 | \| NO922A | | I PC. $\triangle$ OARD | FEC |  | \|SCH. $02 / 71$ |  |  |
|  | 1 partno | oescription | MATLOR | MAT ${ }^{\text {SPEEC }}$ SAR CAT PART No. | FiNish | Finish spec | $\mathrm{CKT}^{\text {SYM }}$ |

Figure 7-4. Parts List


DRILL ALL HOLES NO 55 (.052) DR
AND INSTALL GRIPLET NO46410.
ONO52 (.063) DR
(0) No 43 (.089) DR
$\Delta N=\|(.191) D R$

Figure 7-5. HF Pu1se Phase Comparator P.C. Board Assemb1y 1A4


Figure 7-5. Parts List


Figure 7-6. Main Voltage-Controlled Oscillator P.C. Board Assembly 1A5 D2167B


Figure 7-6. Parts List

(- NO 52 (063) 10
(C) $N \because 43(.089) D R$

- $N=40(.098) 00$
- Ne // (./91) DR

4. CLEAN ASS'Y BEFORE INSTALLATION OF ITEM 2
5.).UMPER AS FOLLOWS: 1550A-5kH

1575-25kHz

Figure 7-7. Frequency Standard P.C. Board Assembly 1A6 C2460

## - NOTES.

1. SCHEMATIC REF DIZ87.
2. SHEAR PER BOARDMASTER BIT44.
3. UNLESS OTHERWILSE SPECIFIED DRILL ALL HOLES N: 55 (.O52IDR ANO INSTALL 46410 GRIPLET:

ALL I.C.S-NO 70 (.028) OR
SWITCH SECTIONS-N: 55 (.052) DR
(D) $N \subseteq 52(.063) D R$
(0) $N \cong 43(.089) D R$

- $N=1 /(191) D R$

Figure 7-8. LF Programmable Divider P.C. Board Assembly 1A7


Figure 7-8. Parts List

2. UNLESS OTHERWISE SPECIFIED

DRILL ALL HOLES NO 55 (.O52) OR
ANO INSTALL GRIPLET N: 46410.
NO $52(.063) D R$
O No 43 (.089) DR
$\Delta N O / /(.191) D R$

Figure 7-9. LF Pulse Phase Comparator P.C. Board Assembly 1A8


Figure 7-9. Parts List


TOLERANCE ON TERMINAL PIN LOCATION $\pm .005$

## TERMINAL CONNECTIONS

1. OSC. $B+($ NOM. $+12 V$ )
2. GROUND
3.RF, TTL/DTL COMPATIBLE OUTPUT (FAN OUT OF GT²L GATES)
3. LOGIC $B+(N O M+5 V)$
4. GROUND

## APPLICATION NOTES

1. OSC. B + MUST BE HELD $\pm 2 \%$ OVER TEMPERATURE RANGE.

| -3 | MC 163 $\times 2-0226$ | 4,000.000 | $0^{\circ} \mathrm{TO}+55^{\circ} \mathrm{C}$. | $\pm 0.5 P P M\left(5 \times 10^{-7}\right)$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| -2 | MC 163×2-0216 | 4,000.000 | $+25^{\circ} \mathrm{TO}+55^{\circ} \mathrm{C}$ $0^{\circ} \mathrm{CO}+25^{\circ} \mathrm{C}$ | \#0.5PPM ( $\left.5 \times 10^{-7}\right)$ |  |
| -1 | MC 163 $\times 2-020 \mathrm{G}$ | 4,000.000 | $0^{\circ} \mathrm{TO}+55^{\circ} \mathrm{C}$ | $\pm 1$ PPM ( $1 \times 10^{-6}$ ) |  |
| ITEM | MC COY ELECTRONICS PABT NO | $\begin{gathered} \text { FREQUENCY } \\ \text { KHz } \end{gathered}$ | TEMPERATIRE RANGE | FREQUENCY STABLLTY WITH TEMPERATURE | NOTES | LOAD IS 15 MA MAX

2.LOGIC B + MUST BE HELD WITHIN $\pm 5 \%$ OVER TEMPERATURE RANGE.
LCAD IS 15 MA IMAX.
3.AGING CHARACTERISTIC SPEC TYP.

|  |  | YIRST YEAR |
| :--- | :--- | :--- |
| FIVE YEAR | $4 P P M$ | $0.5 P P M$ |
| EQUENCY TRIMLIFE | 8 YEARS | 10 YPARS |

FREQUENCY TRIMLIFE 8 YEARS 10 YEARS
4. DIMENSIONS SHOWN ARE FOR F.E.C
APPLICATION INFORMATION.

Figure 7-10. TCXO Crystal Oscillator Assembly B1690A

MOTE

1. THESE TRANSISTORS TO BE SELECTED BY FEC FOR PINCH OFF (GATE-SOURCE CUTOFF) VOLTAGE, WITHIN RANGE, INDICATED BY SELECTION FAOM LOT OF TYPE $2 N 5459$. SELECTION PASED ON VALUE OF VGS FOR $10=10$ MAOC WITH VOS $=12 \mathrm{VOC}$. AFTEA SELECTION COLOA CODE WITH DOT OF PAINT FOR IDENTIFICATION: B1686-1: EROWN (VGS = 2.0 TO 3.25)
B1686-2: PED (VGS=4.5 TO 8.0V)


| -2 |  | B1686-2 | FET, HIGH PINCH OFF (4,5-8.0V) | MOTOROLA | $2 N 5459$ | SEE NOTE |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| -1 |  | B1686-1 | FET, LOW PINCH OFF (2.0-3.25V) | MOTOAOLA | $2 N 5459$ | SEE NOTE |  |  |
| ITEM | REQ ${ }^{\prime}$ | PART NO. | DESCPIPTION | MFA | CAT: PAPT NO. | FINISH | FIN. SPEC. | \|ckT. Sim| |

Figure 7-11. 2N5459 Transistor Control Drawing

