SHEET INDEX AND ISSUE CONTROL

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CIRCUIT DESCRIPTION FOR THE 410403 PROGRAMMABLE
INTERVAL/TIMER/STATION IDENTIFICATION DEVICE
CIRCUIT CARD ASSEMBLY

SHEET 1

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CIRCUIT DESCRIPTION FOR THE 410403 PROGRAMMABLE INTERVAL TIMER/STATION IDENTIFICATION DEVICE CIRCUIT CARD ASSEMBLY

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SECTION I - USER INFORMATION

1. Purpose of the Circuit

1.1 The 410403 PIT/SID Logic Card Assembly contains the electronics for the Programmable Interval Timer (PIT) and Station Identification Device (SID). Both are I/O devices for the 40C400 Controller and therefore conform to all 'TELEBUS' input and output signalling standards.

1.2 The purpose of the PIT is to provide a means of generating two independent and program-variable time delays when the device is used as part of a 40C400 based data communications system.

1.3 The purpose of the SID is to provide 8 bytes of field-alterable, non-volatile read only data storage to be addressed by 40C400 operating programs.

2. Functional Description

2.1 Functional Description of the PIT. (Refer to simplified block diagram Figure 1.) - The variable time interval produced by each of the two timers (A and B) is generated by two presettable modulo 256 counting registers. These counters are connected in the count-down mode and, after being preset with a value from the TELEBUS via program control, signify expiration of the time interval when they hit the 'all zeros' state. Expiration of the time interval causes the device 'DONE' flag to be set. This flag generates an interrupt if the corresponding 'INTR ENABLE' flag for that timer has been set by the operating program. Both of these flags are component bits of a 4 bit status register for each timer. Each status register is addressable with the proper device address and may be loaded via the program from the TELEBUS. Clock pulses for the two mod 256 counters are derived by dividing the master system clock (896 KHz) with a frequency divider. This divider consists of 18 binary counting stages with output taps at stages 9, 14, and 18 generating clock signals with periods of 571 ms, 18.28 ms and 293 ms respectively. Three ranges of timing intervals are possible by providing for connection of the mod 256 counters to one of the 3 prescale frequencies. Two 'RANGE SELECT' bits in the status register of each timer are provided to allow selection of the prescale frequency under program control.

2.2 Functional Description of the SID - The 8 bytes of field programmable data storage are provided by 8 dual-in-line 8 position switch packages. Each switch position programs one of the 64 bits of storage. When a SID device address is properly decoded, the contents of 8 switch positions is selected and applied to the TELEBUS drivers to make up a byte of information.

3. User Programming Information

3.1 Device address and interrupt vector programming - A single PIT device constituting two timers is one 40C400 I/O device and shares the same circuit board as one SID. As a result, the devices share common addressing logic and therefore have adjoining device I/O addresses. These addresses and generated interrupt vectors are assigned as follows:

3.1 (Continued)

DEVICE	REGISTER	I/O ADDRESS (binary)	VECTOR (binary)
SID	CELL 1	$A_7A_6A_5$00000	
	CELL 2	00010	
	CELL 3	00100	
	CELL 4	00110	
	CELL 5	01000	
	CELL 6	01010	
	CELL 7	01100	
	CELL 8	01110	
PIT	TIMER A STATUS	10000	$0V_6V_5V_4V_3$000
	TIMER A DATA	10010	
	TIMER B STATUS	10100	$0V_6V_5V_4V_3$010
	TIMER B DATA	10110	

Where A_N represents bit N of the device address, and V_N represents bit N of the generated vector. Decoding of address bits A_7 - A_5 and generation of vector bits V_6 - V_3 is programmed by the switch package located at circuit board position C11 as follows

SPC11 SWITCH POSITION	ADDRESS BIT TO BE PROGRAMMED		VECTOR BIT TO BE PROGRAMMED
POSITION 1			V_3
POSITION 2	A_5	=	V_4
POSITION 3	A_6	=	V_5
POSITION 4	A_7	=	V_6

Switch positions are ordered from top to bottom of the switch package assembly with position 1 being at the top when the card is in the upright position. Closing of the switch (ON) programs a logical '0', whereas opening it programs a logical '1'.

Note that the interrupt vector contains the same 3 bits of information as the assigned device address, but offset by one bit position. An additional programming switch (position 1) is provided to select the value of V_3 for testing (which is normally set to a '1'). I/O address bits 1-3 select one of eight possible registers or data cells within a given device. Note, however, that the PIT has a fixed value for bit 3 ('0') since there are only 4 addressable registers in the device (one status and one data for each of two timers).

3.2 Detailed PIT Usage Information

3.2.1 Status Registers

3.2.1 (Continued)

BIT	DESCRIPTION
00	'DONE' flag (Read Only) - Timing Interval has expired. An Interrupt with the proper vector occurs if the 'INTR ENABLE' flag has been set. This bit is automatically cleared whenever a new status word is written or its interrupt has been granted.
01	'INTR ENABLE' (Read/Write) - Allows the 'DONE' flag to generate an interrupt when set. This bit is automatically cleared upon initialization.
02,03	'TIMER RANGE SELECT' (Read/Write) - Combinations of these bits select the timer ranges as follows:

BIT COMBINATION BIT 3, BIT 2			RANGE (ms)	ACCURACY (ms)
0	0		TIMER IS OFF	
0	1	#1	.571 - 145.6	.571
1	0	#2	18.28 - 4660	18.28
1	1	#3	293 - 74610	293

The timer range select bits are automatically cleared when the interval expires, thus placing it in the 'timer off' state. The timing operation is started as soon as these bits are loaded with a non-zero value.

04-07 Not used, generate zeros when read.

3.2.2 Data Register (Counter Preset)
The Counter Data Register may be preset with an unsigned 8 bit integer value in the range of 1 to 255 (decimal). The value of the time interval generated in each range is then:

RANGE	TIME INTERVAL (ms)
#1	.571*N
#2	18.28*N
#3	293*N

Where 'N' is the 8 bit preset value and is taken to be the multiplier for the clock rate in each range. At the end of the programmed interval the counter data register is automatically recycled back to 255 and ready to generate the largest interval in a given range without being reloaded. The counter register is write-only and will generate all zeros when read.

3.3 Detailed SID usage Information -
The 8 bytes of SID information is programmed by setting 64 switches. The switches are arranged as 8 dual-in-line switch packages each with 8 switch positions. The following table relates the switch positions and the

3.3 (Continued)

switch package locations on the circuit board to the corresponding byte and bit numbers of the SID.

SID BYTE NO.	BIT NO. 0	1	2	3	4	5	6	7
0	SPA 17 Position 1	SPA 15 Position 1	SPA 13 Position 1	SPB 13 Position 1	SPB 15 Position 1	SPB 17 Position 1	SPC 17 Position 1	SPC 15 Position 1
1	SPA 17 Position 2	SPA 15 Position 2	SPA 13 Position 2	SPB 13 Position 2	SPB 15 Position 2	SPB 17 Position 2	SPC 17 Position 2	SPC 15 Position 2
2	SPA 17 Position 3	SPA 15 Position 3	SPA 13 Position 3	SPB 13 Position 3	SPB 15 Position 3	SPB 17 Position 3	SPC 17 Position 3	SPC 15 Position 3
3	SPA 17 Position 4	SPA 15 Position 4	SPA 13 Position 4	SPB 13 Position 4	SPB 15 Position 4	SPB 17 Position 4	SPC 17 Position 4	SPC 15 Position 4
4	SPA 17 Position 5	SPA 15 Position 5	SPA 13 Position 5	SPB 13 Position 5	SPB 15 Position 5	SPB 17 Position 5	SPC 17 Position 5	SPC 15 Position 5
5	SPA 17 Position 6	SPA 15 Position 6	SPA 13 Position 6	SPB 13 Position 6	SPB 15 Position 6	SPB 17 Position 6	SPC 17 Position 6	SPC 15 Position 6
6	SPA 17 Position 7	SPA 15 Position 7	SPA 13 Position 7	SPB 13 Position 7	SPB 15 Position 7	SPB 17 Position 7	SPC 17 Position 7	SPC 15 Position 7
7	SPA 17 Position 8	SPA 15 Position 8	SPA 13 Position 8	SPB 13 Position 8	SPB 15 Position 8	SPB 17 Position 8	SPC 17 Position 8	SPC 15 Position 8

Where the designation 'SPA 17' represents the switch package located at board co-ordinate A17. A given switch is programmed for a logical '0' by closing it (ON) and a logical '1' by opening it (OFF).

SECTION II - DETAILED DESCRIPTION

1. General

1.1 A single +5.0V supply voltage is required by the circuit card assembly. This voltage should have a tolerance of ± 10%.

1.2 The following convention is used in the circuit description to give a unique designation to each circuit in an integrated circuit package.

MLB8 - (4)
ML - Refers to micrologic
B8 - Refers to the package located at board location B8.
(4) - Refers to the pin number of the output of the circuit.

1.3 The terms 'HIGH' and 'LOW' are used in this description to indicate logic voltage levels; where 'HIGH' represents any voltage between 2.4 and 5.5 V and 'LOW' represents any voltage between 0.0 and 0.4 V.

1.4 Signal leads are labeled with a title descriptive of its function. When they are superscribed with a bar (e.g. '$\overline{\text{BUS ENAB}}$') it indicates that the signal is in the LOW state when the state described by the signal is present; otherwise it is in the HIGH state.

2. Circuit Card Operation

2.1 FS-1 - TELEBUS INTERFACE (Refer to 4403SD Sheet 2). All data and address signals received from, and transmitted to the 'TELEBUS' are handled by the two quad bus transceivers MLC4 and MLC5. Data and addresses going into the card are received by the high impedance receiver portion of these devices and transmitted to the local 'IN' bus. Data and interrupt vectors are transmitted from the local 'OUT' bus to the 'TELEBUS' via the gated open - collector driver portion of the transceivers.

The '$\overline{\text{BUS ENABLE}}$' gating signal, which originates on the TELEBUS, provides the proper output timing since all data and address signals must be true while '$\overline{\text{BUS ENABLE}}$' is low. The '$\overline{\text{OUTPUT}}$' gating signal originates in the Read/Write Control Logic section (FS-2) and is issued in response to a TELEBUS read command.

The upper 3 bits of the local 'IN' bus are constantly compared against the device address programming switches SPC11 by the MLC10 address comparator. A fourth input to the comparator is the 'DEV A EN' lead originating on the TELEBUS which selects the devices falling into the A address group. A match between the SPC11 switch settings and the corresponding values on the Local 'IN' bus leads, along with a HIGH on 'DEV A EN', causes a HIGH level on the comparator output MLC10-(6). If such a match occurs during a TELEBUS addressing cycle, the comparator output is latched into one stage of the MLC9 address latch whose output is called the 'UNIT SELECT' lead. A high level on the 'UNIT SELECT' indicates that either the PIT or SID has been addressed for a subsequent read or write operation. Bits 1-4 of the 'IN' bus are latched into the address latch alongside the 'UNIT SELECT' to select the proper register or data cell for reading or writing. The strobe signal for this latching operation is the '$\overline{\text{LD ADDR}}$' lead which originates in the Read/Write control logic FS-2.

The MLC8 address decoder decodes the 4 addresses assigned to the PIT operating registers and generates 4 load pulses '$\overline{LD\emptyset - LD3}$'. The '$\overline{LD\ DATA}$' signal originates in the Read/Write control logic (FS-2) and provides the strobing for the generation of these pulses. All 4 address leads 'A$\emptyset$ - A3' are brought out to provide selection of read data in the Output Selection logic FS-4.

2.2 FS-2 - READ/WRITE CONTROL AND INTERRUPT LOGIC (Refer to 4403SD Sheet 3)

2.2.1 Read/Write Control Logic - All control information from the TELEBUS is received via the MLC3 high impedance hex bus receivers. Control leads '$\overline{C\emptyset}$ - $\overline{C2}$' specify the TELEBUS functions to be performed (e.g. Load Address, Read or Write); while '$\overline{BUS\ ENAB}$' serves as a timing pulse indicating when these control leads contain valid information. Control decoder MLB8 decodes the 5 functions which can be performed by the PIT/SID card. '$\overline{BUS\ ENAB}$' strobes the decoder which generates LOW going pulses at the decoder outputs. The 5 control functions are:

FUNCTION	DEFINITION	$\overline{C2}$	$\overline{C1}$	$\overline{C\emptyset}$
LAD	Load Address	High	Low	Low
LAR	Load Address and Read	High	Low	High
WWI	Write Word	Low	High	High
WBI	Write Byte	Low	High	Low
RDV	Read from Device	High	High	Low

Either '$\overline{LAD}$' or '$\overline{LAR}$' command Lines when LOW together with 'I/O Clock' being HIGH generates a 'LD ADDR' on MLB9-(3) required to clock the address latch as described in Section 2. Similarly '$\overline{WWI}$' or '$\overline{WBI}$' when LOW together with 'UNIT SELECT' and 'I/O Clock' being HIGH generate the '$\overline{LD\ DATA}$' on MLA2-(6) required to strobe the load pulses '$\overline{LD\emptyset}$ - $\overline{LD3}$' in the MLC8 address decoder described in Section 2.1. Both 'LD DATA' and '$\overline{LD\ ADDR}$' are strobed with the 'I/O Clock' signal originating on the TELEBUS because this insures that the trailing (positive going) edge of these signals occurs well before the trailing edge of valid bus information for proper latching of data or addresses. The '$\overline{RDV}$' lead serves to gate read data and interrupt vectors out to the TELEBUS. MLA5-(10) gates '$\overline{UNIT\ SELECT}$' and '$\overline{RDV}$' and generates a HIGH level on the output whenever reading of data is required. This condition is ored with 'VECTOR AB' from the interrupt logic in MLA5-(13) to generate the overall '$\overline{OUTPUT}$' gating pulse required to enable the TELEBUS driver outputs described in Section 2.1.

2.2.2 Interrupt Logic - The interrupt logic consists of two interrupt request flip-flops (MLA4) (one for each timer) and associated gating to generate the control signals required to select and gate the interrupt vectors, propagate the 'GRANT', and generate the TELEBUS '$\overline{INTR}$' signal to the IXL. The interrupt sequence is initiated when timer A or B signals expiration by sending a LOW on the Local '$\overline{REQ\ A}$' or '$\overline{REQ\ B}$'lines. If, at this time, the TELEBUS '$\overline{GRANT\ IN}$' signal is inactive (HIGH); the local request is clocked into the 'J' input of its request flip-flop on the next positive transition of '$\overline{BUS\ ENABLE}$'. This, in turn, conditions several gates at the output of the flip-flops as follows:

2.2.1 (Continued)

a) Gates MLA2-(12) and MLA2-(8) are conditioned to generate an active LOW output on the '$\overline{\text{VECTOR A}}$' or the '$\overline{\text{VECTOR B}}$' leads upon receipt of 'GRANT' and the decoding of control code RDV.

b) If Request A flip-flop is set, MLB9-(11) is conditioned to block the 'GRANT' signal from propagating to the timer B interrupt Logic and other interrupts. If Request B flip-flop is set, MCA1-(3) is conditioned to block the 'GRANT' signal from propagating to other interrupts down the chain.

c) Gates MLA1-(6) or MLA1-(11) pull the TELEBUS '$\overline{\text{INTR}}$' Lead Low to indicate a pending interrupt condition.

2.3 FS-3 PIT LOGIC (Refer to 4403SD - Sheet 4) The Programmable Interval Timer Logic consists of the clock prescaling circuitry, which generates the three clock frequencies (one for each of the three timer ranges), and two identical timer circuits and their required controls. Each of the two timers consists of a clock selector, 8 bit down counter and 4 status flag flip-flops with associated gating.

The 'I/O Clock' provides the master frequency (896 hz) for the prescaler and is received from the TELEBUS with a high impedance receiver MLB1-(2). The 14 stage CMOS binary counter MLC1 accepts the master clock frequency and divides it by 2^9 on pin 12 and 2^{14} on pin 5, generating clocks with periods of .571 ms and 18.28 ms respectively. The third prescale clock frequency (with period of 293 ms) is producted by the 4 bit counter MLC10, which further divides the master clock.

The CMOS low current outputs are converted to TTL current levels by 3 of the remaining receivers in MLB1 which feed the 3 clocks to the two timer circuits. Each timer has a clock selector (MLB2 or MLB7) which selects one of 3 prescale clocks or the 'clock off' condition. The 'clock off' condition produces a steady High level on the clock selector outputs (pin 7). The two range control flags in the status register (MLA9 and MLB10) provide the select code to the clock selector input pins 2 and 14.

The selected clock, appearing on pin 7 of the clock selector, feeds two cascaded 4 bit presettable counters which are connected in the count-down mode of operation. A LOW on the borrow output of the second counter (Pin 13 of MLB4 or MLB6) indicates that both 4 bit counters are in the 'all zeros' state, since the borrow propagates only during a Low Level on the down clock input (pin 4). The borrow output signal primes the $\overline{K}$ input of the status register 'DONE' flag whose $\overline{Q}$ then goes HIGH on the next positive transition of the 'I/O Clock'. At this time two things occur (Refer to timing diagram Fig. 2):

a) Gate MLA6-(4) or MLA6-(13) resets both range control flags which causes the clock selector output to go to a steady HIGH condition. This last transition of the clock shuts off the borrow outputs and recycles the counters to the 'all ones' state.

b) MLA7-(6) or MLA7-(11) go LOW, generating a local interrupt request on '$\overline{\text{REQ A}}$' or '$\overline{\text{REQ B}}$' if the interrupt enable flag had previously been set.

2.3 (Continued)

The 'DONE' flag is reset when the interrupt is granted and the '$\overline{\text{VECTOR A}}$' or '$\overline{\text{VECTOR B}}$' leads go low or when a new PIT status word is written to initiate another timeout ('$\overline{\text{LD}\emptyset}$' or '$\overline{\text{LD2}}$' go LOW). New status information or preset data for the counters is written from the common 8 bit 'IN' bus and loaded into the proper register when the '$\overline{\text{LD}\emptyset}$ - $\overline{\text{LD3}}$' leads are activated. The initialize condition on the TELEBUS is used to preset the range control bits and interrupt enable flag to zero, thus starting the device in the 'timer off' state with no interrupt possible.

All four status flags for each timer are bussed to the Output Selection Logic FS-4.

2.4 FS-4 SID and Data Output Selection Logic (Refer to 4403SD - Sheet 5).

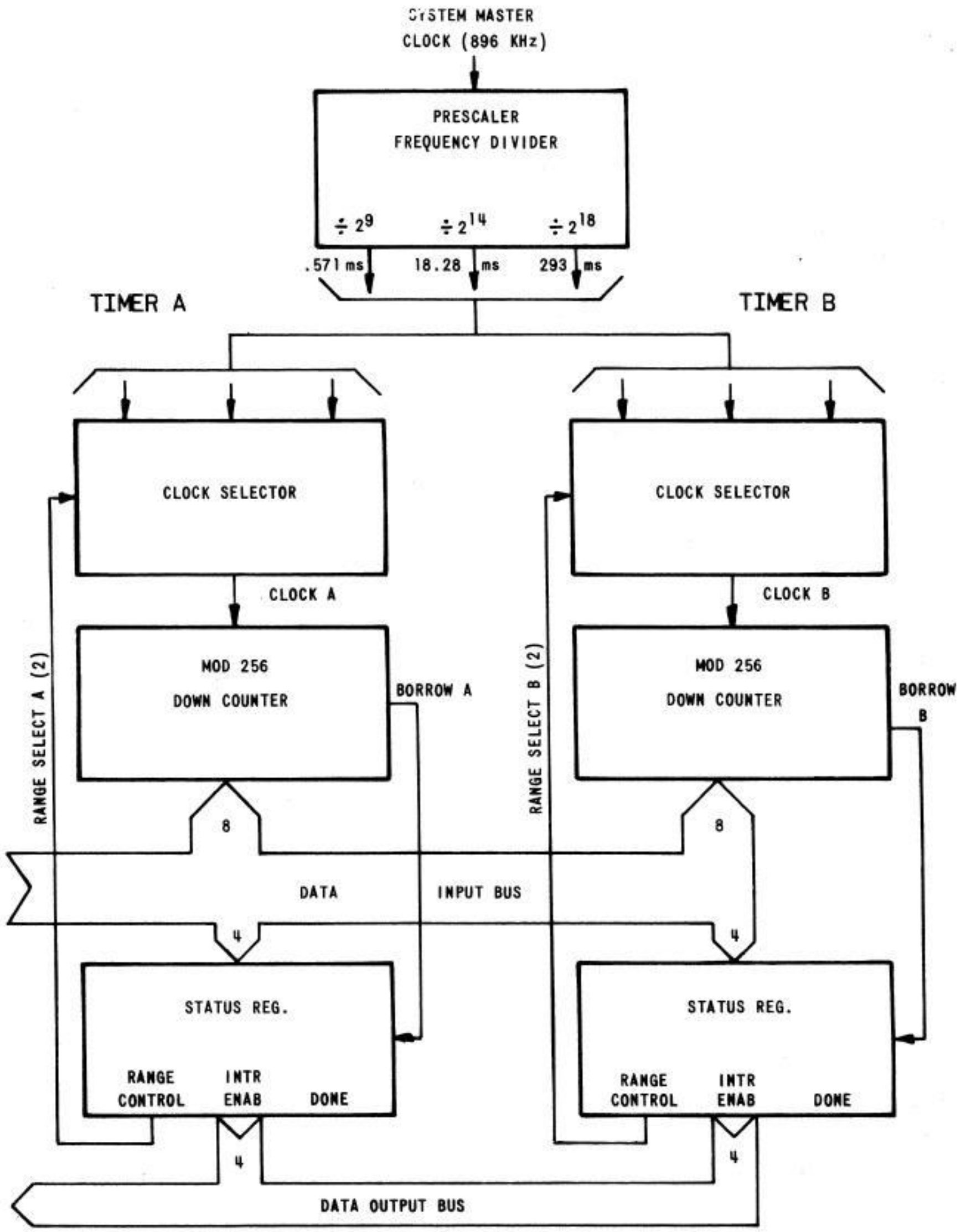
The SID Logic consists of 8 switch assemblies each containing 8 switch positions, and 8-8 input multiplexers. Each switch assembly is connected to the 8 data inputs of the multiplexer package. A switch assembly - multiplexer pair provides one bit of storage for all eight bytes of information.

The three address select leads 'AØ - A2' select the contents of a given switch position to be the output of a multiplexer. Address lead 'A3' disables the outputs of all the SID multiplexers when it is HIGH and instead selects PIT status information in the PIT/SID multiplexer MLA11. Address lead 'A1' selects between the timer A and timer B status in the Timer A/B multiplexer MLB11. Note that address lead 'AØ' serves as a disable and must be LOW when status information is to be read.

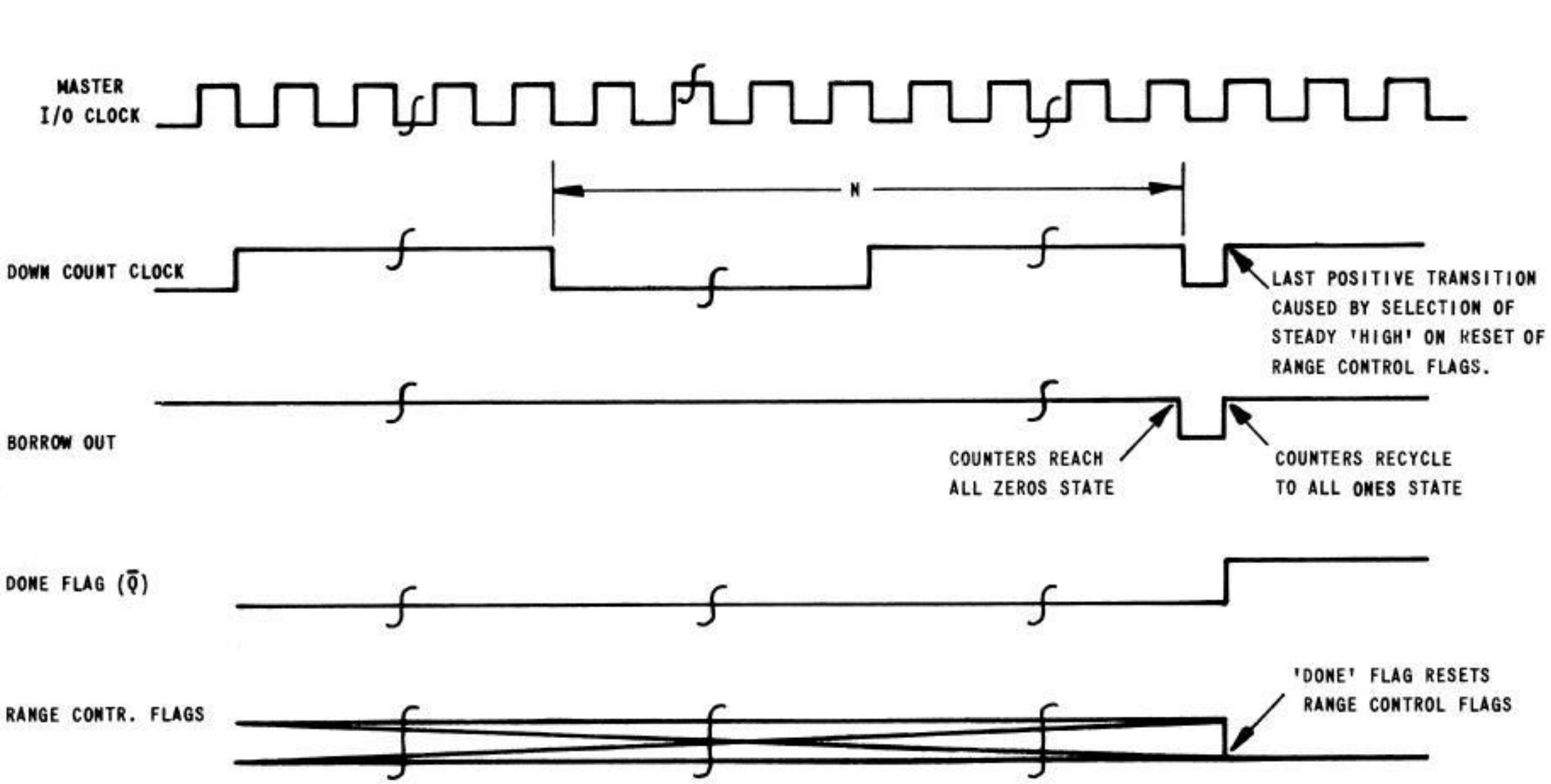
The vector/data multiplexers are controlled by the 'VECTOR AB', lead and select between PIT/SID information or interrupt vector information.

The selected information is presented to the 'OUT' bus and finally gated to the TELEBUS in the interface section of the logic (FS-1).

P.I.T. SIMPLIFIED BLOCK DIAGRAM (FIGURE 1)



PIT TIMING DIAGRAM (FIGURE 2)



WHERE N = 2^9 I/O CLOCKS, FOR RANGE CONTROL = 01

= 2^{14} I/O CLOCKS, FOR RANGE CONTROL = 10

= 2^{18} I/O CLOCKS, FOR RANGE CONTROL = 11

= STEADY HIGH , FOR RANGE CONTROL = 00